DOC112: Hardware Assessed Course Work, October/November 2003

Hand-out date: 23/10/2003
Due Date: 11/11/2003

The coursework is a hardware design exercise, which will result in a circuit that can be built from the integrated circuits types SN7400, SN7406, and SN7408. You are required to submit a wiring list of your design through the normal laboratory submit procedure and hand in a written course work report to the SGO. The report should have a short description of your problem, your design procedures including all the circuits you tried, and your final circuit diagram which should include integrated circuit type assignments and integrated circuit pin numbers (the write up should not exceed four sides of A4). A good grade is given for one working circuit, an excellent one for attempts at minimization of cost by trying more than one circuit. This piece of work counts for 60% of the continuous assessment, the tutorials count 40%.

1. The Problem

Design a four-input, one-output digital circuit which operates as a controlled two-bit Boolean function generator. Two of the inputs are used as control inputs and thus can select one of four different Boolean functions of the other two inputs.

If your name does not appear on the list please send me an email and I will issue you a number. Convert your number to base 4 by looking it up in the table given at the end of this handout. Select **your functions** according to the table below given that the digits of your base four number are **$D_3D_2D_1D_0$.** The operator ⊕ stands for the **XOR (Exclusive OR)** operation.

		C1 C0			
		00	**01**	**10**	**11**
D3 =	**0**	**$A \oplus B$**			
	1	**$(A \oplus B)'$**			
	2	**1**			
	3	**0**			
D2 =	**0**		**A**		
	1		**A’**		
	2		**B’**		
	3		**B**		
D1 =	**0**			**A.B**	
	1			**A.B’**	
	2			**A’.B’**	
	3			**A’.B**	
D0 =	**0**				**A+B**
	1				**A’+B**
	2				**A+B’**
	3				**A’+B’**

For example, if my number is 125, then the base-4 equivalent is equal to 1331, thus D3=1, D2=3, D1=3, and D0=1. Using these digit values and the above table I get my functions:

Digits	**C1**	**C0**	**Output**
D3 = 1	**0**	**0**	**$(A \oplus B)'$**
D2 = 3	**0**	**1**	**B**
D1 = 3	**1**	**0**	**A’•B**
D0 = 1	**1**	**1**	**A’+B**

NB If due to an oversight you have been allocated number 125 please don’t copy out this solution and hand it in but email me and I’ll allocate you a different number!

3. Design Procedure

Once the functions are known, the truth table can be generated and the Karnaugh Map constructed. For the example above this is:

C1	C0	A	B	Result	Function
0	0	0	0	1	(A⊕ B)’
0	0	0	1	0	
0	0	1	0	0	
0	0	1	1	1	
0	1	0	0	0	B
0	1	0	1	1	
0	1	1	0	0	
0	1	1	1	1	
1	0	0	0	0	A’•B
1	0	0	1	1	
1	0	1	0	0	
1	0	1	1	0	
1	1	0	0	1	A’+B
1	1	0	1	1	
1	1	1	0	0	
1	1	1	1	1	

The Karnaugh map can be filled out now (carefully!) and the Boolean expression minimized.

A,B

		00	01	11	10
C1,C0	00	1	0	1	0
	01	0	1	1	0
	11	1	1	1	0
	10	0	1	0	0

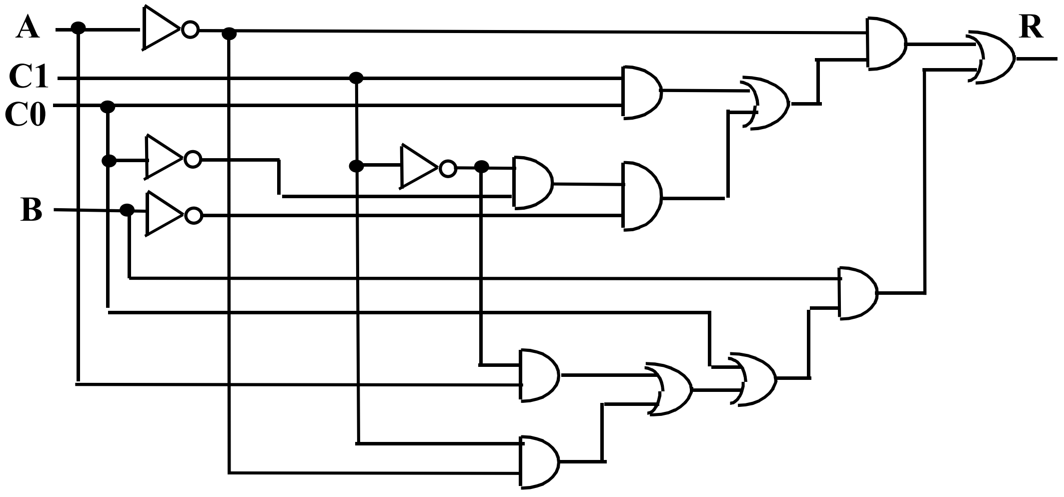
In my case I ended up with a reasonably difficult case. There is one term with four, three terms with three, and one term with two literals. All input signals will have to be inverted. The minimized expression is:

C1’ C0’ A’ B’ + C1’ A B + C1 C0 A’ + C1 A’ B + C0 B

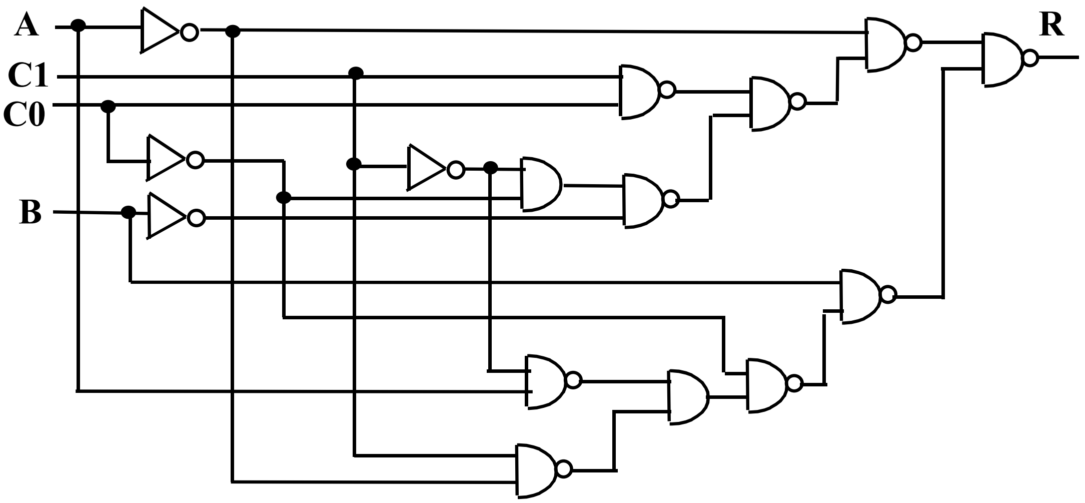
and factoring it one way, I get:

B(C0 + C1’A + C1 A’) + A’(C1’ C0’ B’ + C1 C0)

And the direct circuit implementation is:



Following the design procedures shown in Lecture 4, we transform OR gates to AND or NAND gates and inverters:



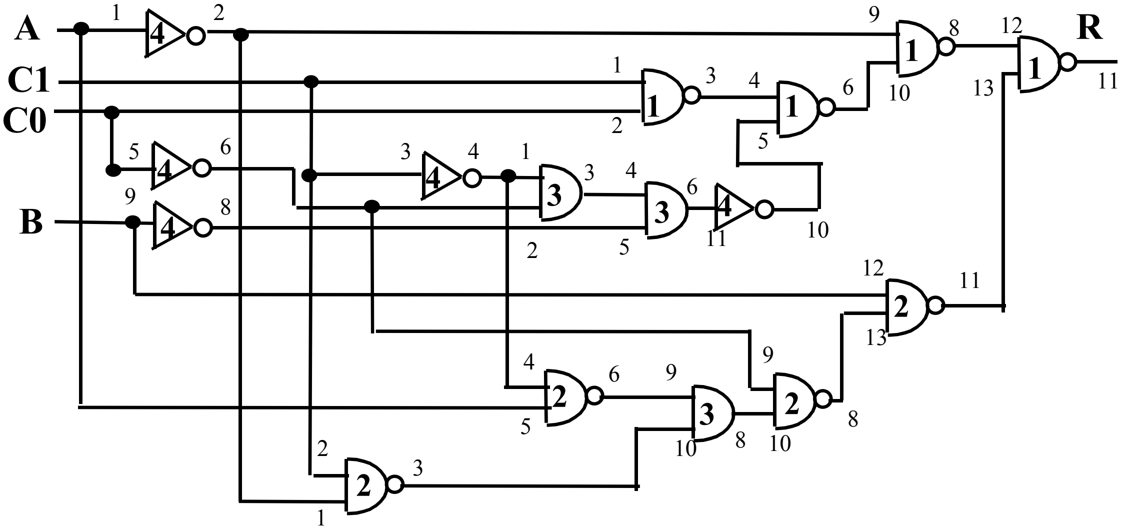
Counting gates, we have to use nine NAND, two AND and four Inverter gates and, accordingly, three type SN7400, one type SN7406 and one type SN7408 ICs. The cost would be:

IC type	U	Cost	
SN7400	1	0.98	
SN7400	1	0.98	
SN7400	1/4	0.62	
SN7406	4/6	0.82	
SN7408	2/4	0.74	Total cost: 4.04

However, we can use one unused AND gate of the SN7408 and one unused inverter gate of the SN7406 ICs to produce one NAND gate and reduce the number of required ICs to four.

IC and pin number assignments.
Since the final product of the design is a wiring list, the gates have to be numbered according to the sequence number of the IC (not it's type number) they belong to. The next step is to indicate the pin number on the wiring diagram for each wire connection. The outputs of the gates can be named consistently with the IC number and pin number; thus, S211 indicates the second IC and pin 11. The first IC being the SN7400, the signals connected to the four NAND gate outputs will be assigned names: S13, S16, S18, and S111. (Obviously, if there were more than ten ICs this method would not be consistent because S111 could also indicate IC 11 pin 1).

The IC and pin numbering of the final circuit are shown below.



From this circuit the wiring list can be constructed.

Testing and debugging your circuit

When you have designed the circuit on paper, given sequence numbers to the required ICs and numbered the connections with the correct pin numbers, you have to generate a wiring list. Each wire in the circuit is given a name which can be any combinations of letters or spaces. I have chosen to name my wires with one of the device pins they are connected to. For example S42 indicates the wire that is connected to device 4 pin 2. (It is also connected to devices 1 and 2 so I could have also called it S21 or S19. There are three special reserved wire names: VCC meaning the 5 volt supply or boolean 1: GND meaning the ground, or boolean 0 and OPEN meaning not connected. The rest of the wiring list format is self -explanatory. You can write comments at the head or in the body of the design, but not between the pairs of matching tags: <number> </number>; < inputs> </inputs>;< outputs> </outputs> or <devices> </devices>. Anything other than a letter or a digit can be used as a white space. My wiring list is:

```
//  My solution to the Hardware Coursework.
//  My number is 125 or 1331 in base 4.
//  My functions are: (00)=(A^B)'   (01)=B   (10)=A'B   (11)=A'+B

<circuit>
<number>   168  </number>
<inputs>  C1 C0 A B  </inputs>
<outputs>   R  </outputs>
<devices>
   SN7400(C1,C0,S13,S13,S410,S16,GND,S18,S42,S16,R,S18,S211,VCC)
   SN7400(S42,C1,S23,S44,A,S26,GND,S28,S46,S38,S211,B,S28,VCC)
   SN7408(S44,S46,S33,S33,S48,S36,GND,S38,S26,S23,OPEN,OPEN,OPEN,VCC)
   SN7406(A,S42,C1,S44,C0,S46,GND,S48,B,S410,S36,OPEN,OPEN,VCC)
</devices>
</circuit>
```

There are two ways in which you can test your design in simulation.

The first is a simple digital circuit simulator written for this exercise. It is called “digisim”. You can download the java code from the course web-page along with my wiring list to check it out. To run it under Windows2000 start Forte (under start/programs/programming), then open your downloaded copy of the file digisim.java and compile and execute it using the build menu options. When digisim is running you can open a circuit wiring list in the above text format. It will either report errors to you or print the truth table and the expected output for your function. When you are satisfied that your circuit is correct, (or you have had enough and want to give up!) use the save report option to generate a text file which you should print and hand in with your report.

NB This version of digisim is newly written this year, so you may find bugs. If you do can you report them to Duncan (dfg) by email asap. Anybody who finds and fixes a bug will get an extra mark for the coursework!

The other system you can use is a comprehensive commercial system called Xilnix. You do not have to use Xilinx this term, however, you may find Xilinx fun, and it will draw the circuit for you.

Once successfully tested you could buy the integrated circuits and build it if necessary. However all you need to do is submit it in the normal manner.

Conversion of Decimal Numbers to Base 4

	0	1	2	3	4	5	6	7	8	9
000	0000	0001	0002	0003	0010	0011	0012	0013	0020	0021
010	0022	0023	0030	0031	0032	0033	0100	0101	0102	0103
020	0110	0111	0112	0113	0120	0121	0122	0123	0130	0131
030	0132	0133	0200	0201	0202	0203	0210	0211	0212	0213
040	0220	0221	0222	0223	0230	0231	0232	0233	0300	0301
050	0302	0303	0310	0311	0312	0313	0320	0321	0322	0323
060	0330	0331	0332	0333	1000	1001	1002	1003	1010	1011
070	1012	1013	1020	1021	1022	1023	1030	1031	1032	1033
080	1100	1101	1102	1103	1110	1111	1112	1113	1120	1121
090	1122	1123	1130	1131	1132	1133	1200	1201	1202	1203
100	1210	1211	1212	1213	1220	1221	1222	1223	1230	1231
110	1232	1233	1300	1301	1302	1303	1310	1311	1312	1313
120	1320	1321	1322	1323	1330	1331	1332	1333	2000	2001
130	2002	2003	2010	2011	2012	2013	2020	2021	2022	2023
140	2030	2031	2032	2033	2100	2101	2102	2103	2110	2111
150	2112	2113	2120	2121	2122	2123	2130	2131	2132	2133
160	2200	2201	2202	2203	2210	2211	2212	2213	2220	2221