HANDBOOK OF SEMICONDUCTOR INTERCONNECTION TECHNOLOGY

Second Edition

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HANDBOOK OF SEMICONDUCTOR INTERCONNECTION TECHNOLOGY

Second Edition

EDITED BY
GERALDINE C. SCHWARTZ
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Preface

Since the first edition of this handbook, semiconductor technology has gone through a continued evolution of new devices and materials like never before. Wafer sizes continue to grow with most of the new fabs equipped for 12-inch wafers. The changes are triggered by many considerations: continued need to provide more functions at lower cost; technology features less than 1000 Å requiring new processes, and exponential increase in the number of device elements. At the device level, the field effect transistor (FET) speed is continually improved by things such as use of insulating substrates, straining the silicon (channel region), and use of dual- and triple-gate (FINFET) structures. The interconnection technology is also going through changes, starting with copper wiring in place of AlCu, low-dielectric insulators in place of silicon dioxide, and use of cobalt and nickel silicide in place of titanium silicide for contacts. In parallel, the decreasing feature size and increasing aspect ratio of lines and studs (vertical vias), along with an increase in the number of wiring levels, have created not only the need for new materials but also unprecedented requirement of reliability per unit interconnect. This again has led to process innovations and improvement in equipment for depositing and patterning conducting and insulating films. *In situ* monitoring of several processes has become routine.

Many of the materials and processes described as likely directions in the first edition of this book have become standard in today's chip fabrication facilities: for example (1) dual damascene processes, including both insulator and metal polished using CMP, (2) use of electroplating of copper, which at one time was considered to be potentially fatal, and (3) fluorine-doped silicon dioxide followed by low-dielectric films containing silicon, carbon, hydrogen, and oxygen, and increasing discussion on the use of porous films. Even more fascinating is the evolution of the fabs which process the 12-inch wafers extensively, using single-wafer equipment that is kept isolated from ambient exposure through most of the process steps, traveling in ambient controlled tunnels from station to station with little human intervention. There has been a huge shift in the traditional focus for cleanrooms with emphasis shifting to particulate generation within tools and during processes from ambient- and operator-generated particulates. This is the main reason why the last chapter in the previous edition on cleanrooms has not been included in this revised edition.

Chapter 1 describes the equipment commonly used in manufacturing for deposition and etching and the principles underlying the design and use of the equipment. In this edition, electrochemical deposition equipment used for plating copper is discussed in detail, in addition to updating previous discussions on equipment used for evaporation, chemical vapor deposition (CVD), and plasma processes. Chapter 2 includes many standard techniques used for characterizing metal and insulator films. The principles of electrochemical deposition are also covered. Measurement of the mechanical and thermal properties of insulators is emphasized in this edition, as is the greater use of electron energy loss spectroscopy (EELS), energy filtering TEM, and atomic force microscopy (AFM). The several recently reported methods for characterizing porous dielectric thin films are also included. Chapter 3 is devoted to contacts and in this edition greater focus has been given to integration issues and properties of titanium, cobalt, and nickel. The need for borderless contacts for gates and source/drain has led to newer process schemes that are also discussed. Use of contact studs with planarized CVD tungsten has become widely established. From all indications this is not likely to change in the future. Based on the need to keep the devices and interconnection safely apart, the use of barrier films for both physical (diffusion barrier) and electrical (barrier heights) requirements is reviewed. Chapter 4 now includes a greater discussion of recently reported choices for low-dielectric insulators. The need for planarization at the macro level has become less, since the use of dual damascene has now become widespread; however, the challenges of managing topography fluctuations at the local level remain. There is extensive coverage of low dielectric constant insulators, particularly the newer ones. The mechanical properties of insulators have become important along with their

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thermal and thermomechanical properties. Chapter 5 covers the deposition and etching of metallic films (tungsten, copper, aluminum) but a greater focus is placed on electroplated copper, with emphasis on the morphology of plated films and their properties. Clearly a big challenge for the next generations of devices is the continuing need to form thin adhesion and barrier layers for copper films in the lines and studs. This has led to the pursuit of atomic layer deposition processes and precursor materials that result in continuous nonporous films covering all sides of trench openings of high aspect ratios (two or more). Chapter 6 deals with two main issues: (1) the problems associated with topography and solutions to these problems, emphasizing the details of CMP and dual damascene processes, (2) process/structure choice conflicts, process compatibility, reliability, manufacturability, and methods for defect-free manufacturing. Chapter 7 is devoted to the reliability of thin metallic and insulating films and this revised edition has an expanded discussion on copper reliability. There is an extensive review of electromigration mechanism and testing procedures as well as other wear-out phenomena for wires and vias. The issue of corrosion is also addressed. The reliability of interlevel insulators is examined, with the impact of migration to low dielectric constant materials and the planned use of pores.

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CHAPTER 1

Methods/Principles of Deposition and Etching of Thin Films

Geraldine Cogin Schwartz

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1.1 INTRODUCTION

This chapter covers many of the methods of depositing and etching both dielectric and conducting films used today in semiconductor manufacturing as well as the basic principles behind them. Some specialized techniques such as beam deposition and chemical mechanical polishing (CMP) are covered in Chapter 6.

A brief overview of deposition techniques can be found in Table 1.1 and of etching in Table 1.2.

1.2 EVAPORATION

Sputtering has almost completely displaced evaporation as a method of deposition because of its superior control of alloy composition, step coverage/hole fill by substrate biasing, ease of integration into cluster tools, etc. Since there are some applications of evaporation, particularly for forming lift-off metal patterns, a brief review of the technique is included.

Evaporation is usually used for metal deposition but has also been used to deposit some nonmetallic compounds (e.g., SiO, MgO). Early reviews of evaporation principles and equipment can be found in Holland (1961) and in Glang (1970); a later one is in Bunshah (1982). A review of some of the basics of high-vacuum technology can be found in Glang et al. (1970).

Glang distinguished the steps of the evaporation process: (1) transition from a condensed phase (solid or liquid) into a gaseous phase, (2) transport of the vapor from source to substrate at reduced

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Table 1.1 Deposition Methods

Method	Materials Deposited	General Comments
Evaporation[a]	Pure metals; alloys; compounds	High-vacuum process; need adequate vapor pressure; various support materials;[b] single/multiple sources for alloys; reactive evaporation
Sublimation	Metals; compounds	Used when very high temperature is needed
Sputtering[c]	Pure metals; alloys; compounds; dielectrics	Can control film properties; control stoichiometry of alloys; use bias, high-density plasma, magnetic enhancement, ICP, IMP; directional deposition using collimation, large source-to-substrate distance
CVD/PECVD/ALD[d]	Pure metals; alloys; dielectrics	Better step coverage/gap fill; film composition and properties by choice of reactants, deposition conditions; commercial cluster systems; operating parameters, bias, temperature
Plating[e]	Pure metals; alloys	Hole fill; film properties through bath control
Spin coat[f]	Soluble, dispersible materials: organic insulators	Planarization; step coverage; curing to remove solvents or promote reactions
Beams[g]	Metals; dielectrics	

[a] Source heating: resistance heaters, RF induction heaters, e-gun.
[b] Crucibles, wires, foils.
[c] Metals: DC or RF; dielectrics: RF; option of DC or RF reactive sputtering.
[d] Includes high-density PECVD systems.
[e] Electroless; electrolytic.
[f] Examples: polyimides, xerogels, FOx, SiLK; one report of Cu spin-on.
[g] Beams covered in Chapter 6.

Table 1.2 Etching for Pattern Definition

Method	Materials Etched	General Comments
Wet chemical	Conductors, insulators, silicon	Almost always isotropic[a]; form a soluble product; need insoluble mask with good adhesion; mask profile not important; usually selective, batch processing
Sputter etch, ion-beam etching	All above	Poor selectivity; faceting, trenching, possible vertical etch; redeposition, possible substrate damage; slow, ion beam (single-wafer mode), sputter etch single or batch mode; used in dep-etch gap fill; angle-dependent etch
Reactive plasma, RIE, RSE, RIBE	Widely used in BEOL	Product needs to be volatile/desorbed by ions; high selectivity possible; profile control: both anisotropic and isotropic;[b] mask profile, erosion; redeposition, trenching, and substrate damage issues; aspect ratio-dependent etch rates; batch, single wafer (cluster); high etch rates attainable

[a] Directionality possible in some cases: e.g., "slow" etched for Si which follow crystal planes; columnar structure resulting in vertical profile (Mo).
[b] Anisotropy vs. isotropy: depends on many factors: reactants, etch parameters, ion energy, sidewall protection, etc.

gas pressure, and (3) condensation of the gas at the substrate. The stages of film growth following condensation of the vapor were outlined by Neugebauer (1970): (1) nucleation and island growth, (2) coalescence of islands, (3) channel formation, and (4) formation of a continuous film.

The source that contains the evaporant must have a negligible vapor pressure at the operating temperature and must not react with the evaporant. There are many types of sources and materials (Holland, 1961; Glang, 1970; Bunshah, 1982), e.g., crucibles of refractory oxides, nitrides,

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carbides, and metals, refractory metal wires, and foils of various designs and shapes (Mathis Co. bulletins). Some materials, such as Cr, Mo, Pd, Si, can be sublimed which relaxes the temperature stability requirements for the source. Vaporization is accomplished by the use of resistance, induction, or electron bombardment heating; several configurations of electron guns (e-guns) are described by Bunshah. Many types are available commercially. E-guns are now used most commonly, except where radiation damage may be a problem, e.g., causing flat-band shifts in FET devices. In properly controlled e-gun evaporation, a shell of solid material shields the molten mass from the crucible, preventing interaction between the evaporant and the hearth. Multiple-pocket crucibles are also available. They may be used for sequential evaporation of different films. Or, using several guns simultaneously, with appropriate control of the source temperatures, multiple component films of a desired composition may be deposited (Glang, 1970). Alloy sources have also been used; the component ratio of the source is adjusted so that the deposited film has the required composition, although the vapor pressures of the constituents are different. The source composition is usually determined empirically. Flash evaporation, in which small quantities of the constituents in the desired ratio are completely evaporated, is another way of depositing alloy films and many kinds of dispensers have been used (Glang, 1970). However, whatever the evaporative technique, the control of the composition is rarely as reliable as that obtained by sputtering an alloy target.

Evaporation is carried out at very low pressures, e.g., 10^{-5} to 10^{-8} torr. At these low pressures, the mean free path is very large compared to the source to substrate distance, so that the transport of the vapor stream is collisionless. The emission pattern of the evaporating species is directional; it is described by a cosine law: $dM/dA = M/\pi r^2(\cos\phi \cos\theta)$ which is illustrated in Figure 1.1. The profile of the emitted flux is shown in Figure 1.2. A comprehensive discussion can be found in Neugebauer (1970).

Since the thickness of the deposited film is greatest directly in line with the source and decreases to either side, uniformity requires the use of planetary (rotating) substrate holders tailored to the particular deposition requirements. Typical of the holders available commercially is the so-called normal-angle-of incidence fixture (Figure 1.3a), which is used for high uniformity and minimum step coverage, suitable for lift-off processes. Another type (Figure 1.3b) has additional planets which rotate at a higher speed and is designed for good step coverage as well as uniformity. Radiant substrate heating, using refractory wires or quartz lamps, is required because the properties

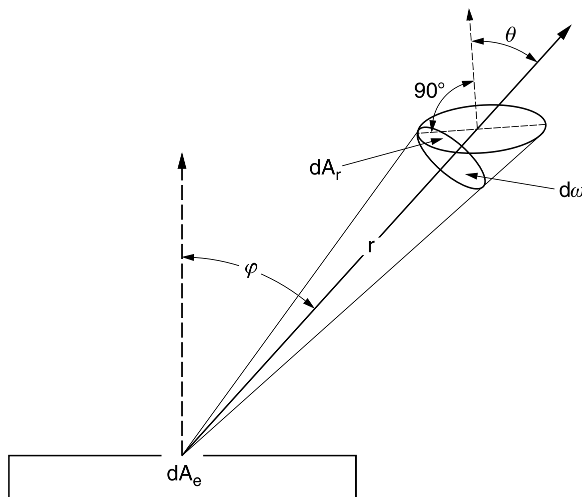

Figure 1.1 Evaporation from a point source dA_e onto a receiving surface element dA_r.

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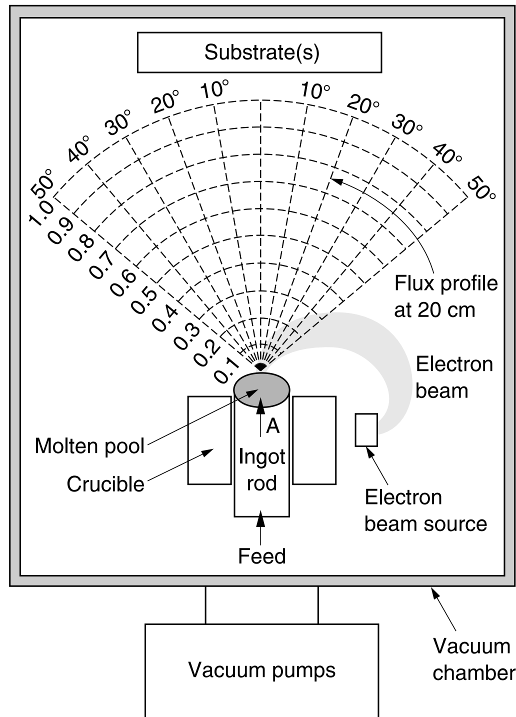

Figure 1.2 Profile of emitted flux. (From Bunshah, R.F., Ed., *Deposition Technologies for Films and Coatings*, Noyes Publications, Park Ridge, NJ, 1982.)

of the deposited thin films are dependent upon the deposition temperature. Temperature monitors and controllers are, therefore, also needed.

There are several kinds of thickness monitors, e.g., ionization gauges and particle impingement rate monitors, for the vapor stream. Crystal oscillators are used most frequently to measure the deposited mass; they utilize the piezoelectric properties of quartz. A thin crystal is part of an oscillator circuit so that the AC field induces thickness-shear oscillations whose frequency is inversely proportional to the crystal thickness; increasing the mass of deposit decreases the frequency. The crystal used has a specific orientation known as the AT cut, because this orientation exhibits the smallest temperature dependence. The thinner the crystal, the greater the sensitivity, if the mass deposited is small with respect to the wafer thickness. For a quartz thickness of 0.28 mm, and an initial frequency of 6 MHz, the change of frequency/thickness is 81.5 Hz/μg/cm (Wagendristel and Wang, 1994). The availability and simplicity of use makes the crystal oscillator preferable to microbalances. Interferometry is used for transparent films. For metals, optical techniques such as light absorption, transmittance and reflectance techniques, as well as resistance monitoring have also been used, but with less success. Thickness control is achieved by simply following the thickness monitor and stopping the process when the desired thickness is reached. Rate control is more complex; it requires adjustment of the source temperature, which means that a measurement and feedback mechanism is required.

The brochures supplied by equipment manufacturers are an excellent source of detailed information about the currently available evaporation systems and their operation. *In situ* sputter cleaning prior to evaporation of a metal film into a via hole is used to remove a contaminant film which causes high interfacial resistance (Bauer, 1994). When the lower surface is aluminum, the native oxide can be regrown quickly after sputter cleaning, due to the presence of residual water vapor.

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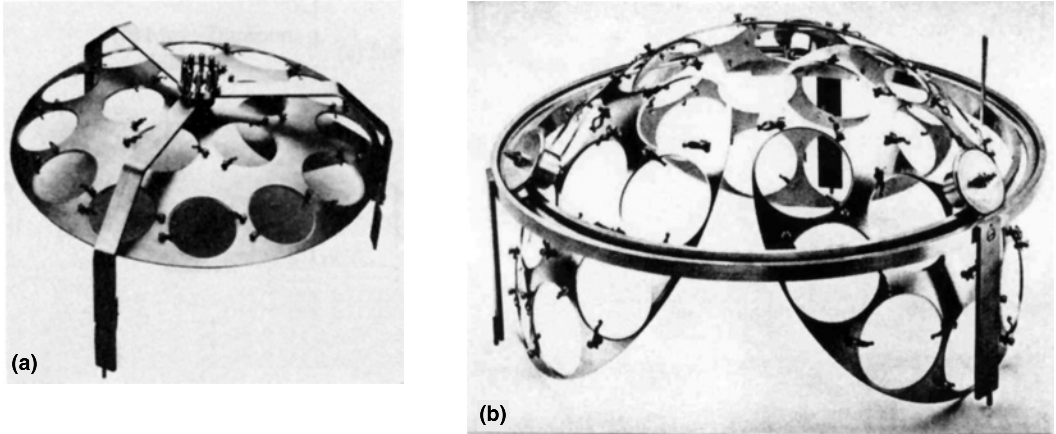

Figure 1.3 Substrate holders for evaporators: (a) normal angle of incidence fixture; (b) planetary fixture. (From Temescal Co., Airco coating technology bulletins. With permission.)

Sputtering of an aluminum electrode, before exposing the wafers to the plasma, is an efficient way of reducing the partial pressure of water vapor, thereby eliminating the need for prolonged sputter cleaning.

1.3 CHEMICAL VAPOR DEPOSITION

1.3.1 Introduction

The term chemical vapor deposition, CVD, used without modifiers, refers to a thermally activated reaction. Plasma and photon activation have also been used; these processes are called plasma-enhanced CVD (PECVD) and photon-enhanced CVD (sometimes referred to as LACVD, for laser-activated CVD) and are discussed elsewhere in this chapter. The term MOCVD refers to the use of an organometallic compound as a source gas in CVD. CVD processes have been used in the preparation of both metallic and insulating thin films as well as for depositing semiconductors. There are a number of reviews that contain more detailed information than can be covered here: Kern and Ban (1978), Sherman, (1987), Mitchener and Mahawili (1987), and Jensen (1989). There is also a book by Kodas and Hampden-Smith (1994). In addition, there are individual papers collected in CVD symposia proceedings volumes of the Electrochemical Society.

Because of temperature restraints imposed by interconnnection metallization, high-temperature CVD processes cannot be used for interlevel dielectrics but have been used for (usually) doped oxides to smooth the topography beneath the first interconnection level. CVD is being used to deposit metals (e.g., W, Al, Cu, Ti), nitrides of, for example, Ti and Ta, and various silicides. Currently, important uses of CVD of metals are the deposition of (1) thin conformal metal films to line trenches (barriers and seed layers) and (2) thicker films to fill vertical via holes (the vertical interconnections are termed “plugs” or “studs”) and to fill vertical vias and trenches of damascene structures.

A more recent development is atomic layer deposition (ALD) used to prepare *very* thin, continuous, conformal metal films for barriers and as seed layers in the electrodeposition of Cu. Discussions of specific CVD processes are postponed to the chapters covering the particular flms.

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1.3.2 Principles

Film formation by chemical vapor deposition is a heterogeneous chemical reaction in which volatile reactants produce a solid film upon reaction at a hot surface. The sequential kinetic steps have been summarized by Jensen (1989) as follows:

"(1) mass transport in the bulk gas flow region from the reactor inlet to the deposition zone, (2) gas-phase reactions leading to the formation of film precursors, (3) mass transport of film precursors to the growth surface, (4) adsorption of film precursors on the growth surface, (5) surface diffusion of film precursors to growth sites, (6) incorporation of film constituents into growing film, (7) desorption of volatile byproducts of the surface reaction, (8) mass transport of byproducts in the bulk gas flow region away from the deposition zone toward the reactor exit."

Homogeneous gas-phase reactions must be suppressed since they are responsible for the formation of dust particles which become incorporated into the growing film, making it hazy and defective. In a thermally activated reaction, the dependence of rate on the temperature is given by the Arrhenius equation:

$$\ln\text{(rate)} = -E/RT + \text{constant}$$

where E is the energy of activation. However, if the deposition rate is controlled by the transport of the reactant, the rate will be approximately independent of temperature. In many CVD reactions, two regions are observed: (1) the surface rate-limited reaction (temperature controlled) and (2) the mass transport-limited reaction (temperature independent), as illustrated in Figure 1.4. In the latter, the surface reaction is fast relative to the transport of reactants. Temperature uniformity is critical for film uniformity for the first type of reactions. For the second type flow across the wafer surface is critical.

1.3.3 Reactors

1.3.3.1 Classification

One way of classifying CVD reactors is by the relative temperatures of the parts of the system: there is the hot-wall system in which the substrate and reactor walls are at the same temperature, and the cold-wall system in which the substrate is at a higher temperature than the walls so that deposition occurs only on the substrate. There is the possibility of contamination by

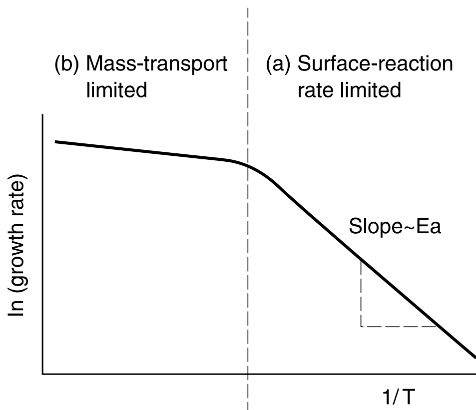

Figure 1.4 Deposition rate vs. temperature for CVD processes.

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deposition on and subsequent flaking off the heated chamber walls. As pointed out by Kern and Ban (1978), the deposit is dense and adherent, and if not permitted to become too thick the problem of flaking may not be severe, particularly since there is no thermal cycling. Also, since the wafers are stacked vertically, any flakes would not be likely to fall on them. In the cold-wall reactor, this source of contamination is negligible, but convection due to temperature differentials can arise (Carlsson, 1985).

Another classification scheme is in terms of the pressure at which a reactor is operated. The earlier classifications were atmospheric pressure (APCVD) and low pressure (LPCVD) which covers a pressure range of about 0.05 torr to several torr. More recently, particularly for the deposition of SiO_2 films, both sub-atmospheric (SACVD; ~600 torr) and intermediate pressure (no acronym; ~60 torr) have been used. At higher pressures, the rates of mass transfer of the volatile reactants and byproducts and of reaction at the surface are about the same order of magnitude. Reducing the pressure increases the mass transfer rate so that reaction at the surface becomes the rate-limiting step. Reactor configuration greatly influences mass transport and thus is a critical factor for APCVD, but not for LPCVD. Uniform deposition is more easily achieved in LPCVD but the deposition rates are much lower than in APCVD.

Another way of classifying a reactor is by the deposition temperature: high temperature (HTCVD; ~750 to 950°C) and low temperature (LTCVD; below ~500°C). It can be seen that there are many possible combinations for CVD reactor and process design.

1.3.3.2 Examples of Reactors

Winkle and Nelson (1981) described a cold-wall low-temperature (LT) APCVD reactor, made by Watkins-Johnson. It is used for depositing undoped and P-doped SiO_2 and is shown in Figure 1.5. At temperatures of ~350 to 450°C, deposition rates as high as ~1 μm/min were achieved using mixtures of O_2 and the appropriate hydrides. A feature of this reactor is the gas injector design which improves surface reaction uniformity and coating efficiency and prevents homogeneous gas phase reactions.

An example of a hot-wall LPCVD system is shown in Figure 1.6; this is typical of reactors used to deposit insulators and metals. Two versions of an experimental single-wafer, LP cold-wall reactor, designed for selective W deposition from WF_6 and H_2, are shown in Figure 1.7 (Stoll and Wilson, 1986). In the system in Figure 1.7a, the substrate is heated radiantly by means of quartz lamps; in

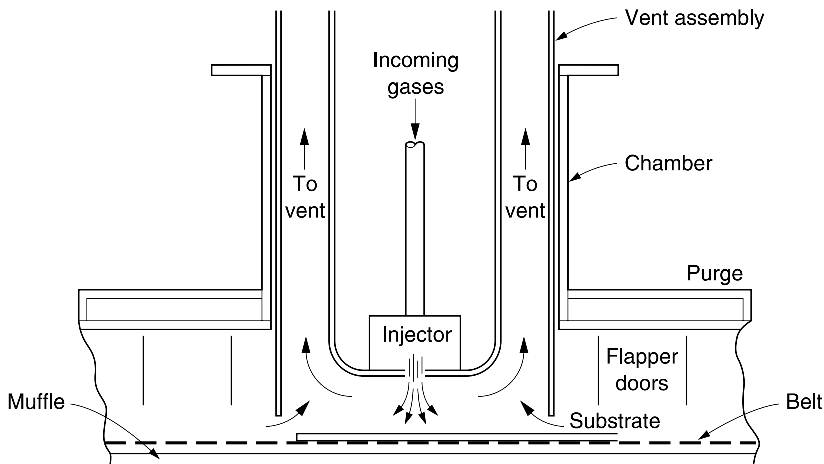

Figure 1.5 Schematic of an APCVD reactor. (Watkins-Johnson.)

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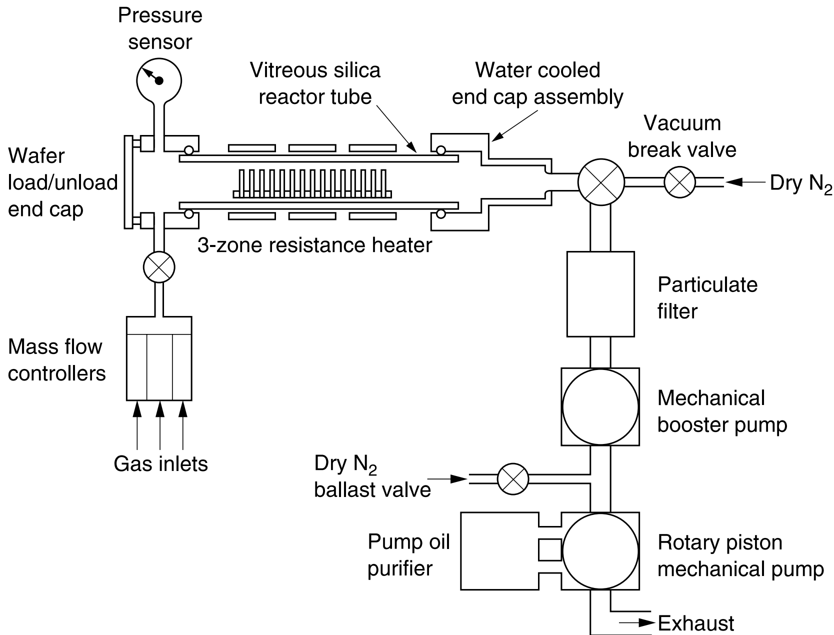

Figure 1.6 Schematic of an LPCVD reactor. (Reproduced from Kern, W. and G.L. Schnable, IEEE *Trans. Electron Dev.*, ED-26, 647, 1979. With permission of the Electrochemical Society, Inc.)

that in Figure 1.7b the wafer is heated on a hot plate. Another system (Heiber and Stolz, 1987) was an adaptation of a sputtering module and was equipped with a load lock, as shown in Figure 1.7c

A commercially available, single-wafer, cluster-compatible, cold-wall LPCVD chamber is the Watkins-Johnson SELECT™ reactor shown in Figure 1.8, in which the wafer rests on a quartz cover and is heated by an encapsulated three-zone graphite heater. The system pressure is about 1 torr, and has been used to deposit SiO_2 doped with both P and B (BPSG) from SiH_4 and O_2.

Another commercially available, load-locked, single-wafer, cold-wall reactor is the Applied Materials Precision 5000 system shown in Figure 1.9a; it has been integrated into a "cluster tool" (Figure 1.9b). This reactor has been used for blanket W deposition from WF_6 and H_2 at 10 to 80 torr (Clark et al., 1991) and for SiO_2 (doped and undoped) from TEOS + O_3 (plus dopants) at 60 torr or at 600 torr (SACVD) (Lee et al., 1992). For these applications, the radio-frequency (RF) feed-through shown in the diagram is not used. This thermal CVD/PECVD reactor is covered by patents (Wang et al., 1989, 1991).

1.3.4 Film Properties

The composition and purity of a film, its electrical and mechanical properties, the deposition rate, and its uniformity are controlled by the many variables involved and the interaction among them is complex and difficult to categorize. The reviews cited above contain more detailed information. Some discussion of specific films can be found in Chapter 4 and Chapter 5.

1.4 PHOTOENHANCED CVD

True photochemical processes depend on the fragmentation/activation of the reactant molecules, in the gas phase or on the surface, by photons. The advantage of photoinduced reactions is

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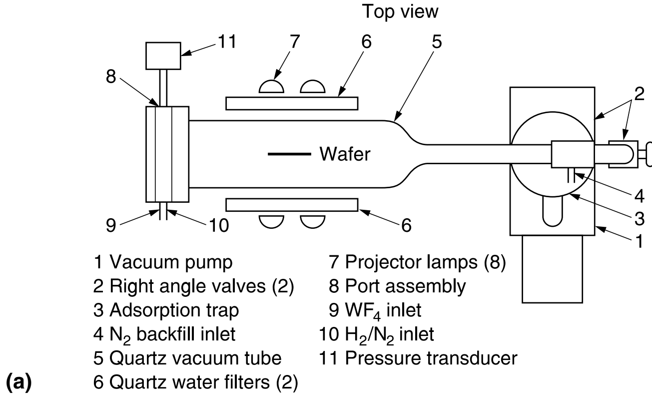

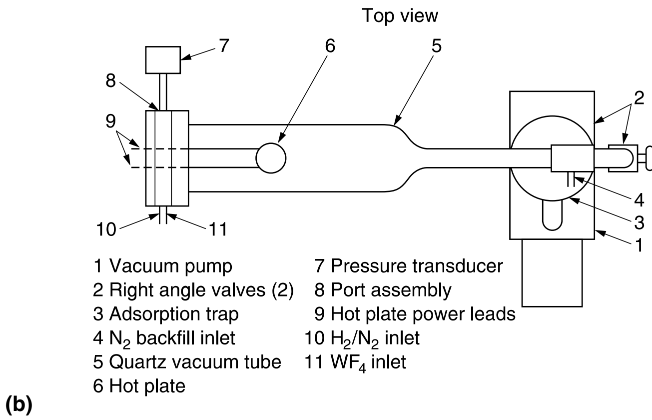

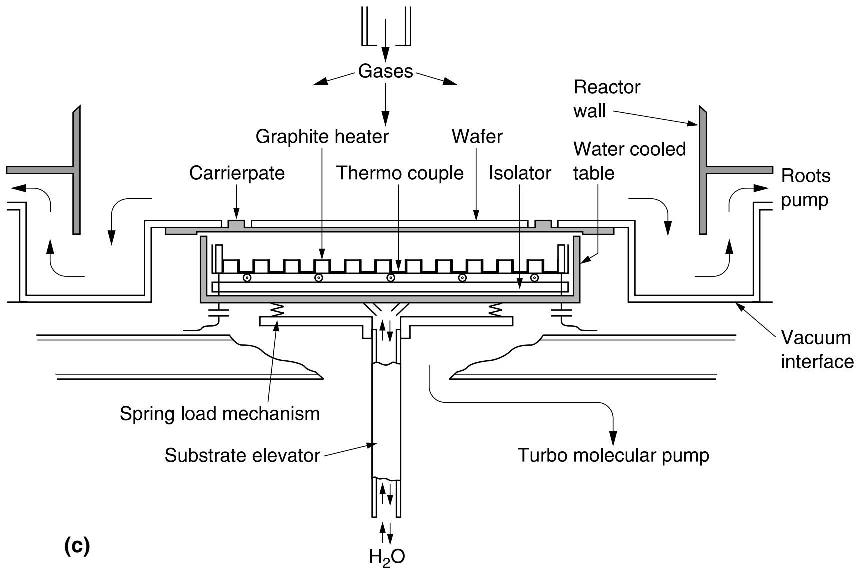

Figure 1.7 Experimental cold-wall CVD reactors. (a) Tungsten filament lamp heating; (b) hot plate heating. (From Stoll and Wilson (1986). With permission of the Electrochemical Society, Inc.) (c) Single-wafer cold-wall system with load lock. (From Hieber, K. and M. Stolz, 1987 VMIC, 1987, p. 216. With permission.)

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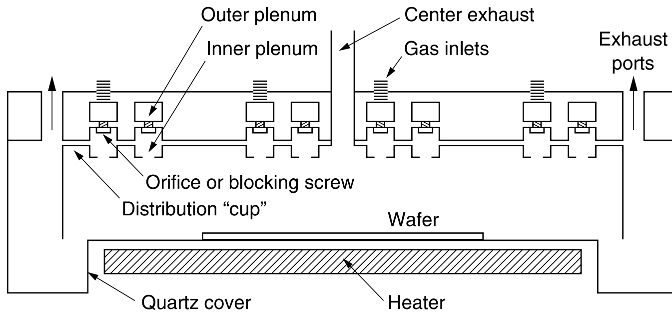

Figure 1.8 Schematic of a single-wafer CVD system: Watkins-Johnson Select™.

Figure 1.9 Schematic of an Applied Materials Precision 5000™ single-wafer CVD reactor: (a) side view of an individual chamber; (b) top view of the cluster system configuration.

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the absence of electromagnetic radiation and charged species which can induce damage in dielectric films. To quote Eden (1991):

> Optical radiation can induce specific chemical reactions in the gas phase or at a surface. The selective production of atoms, radicals or other excited species in the vicinity of a surface independently of the substrate temperature, effectively decouples temperature from the number density of the species of interest. The introduction of photons allows one to drive the chemical environment far from equilibrium by selectively producing species not normally present in conventional CVD reactors.

In some cases, radiation merely heats the surface and the process is, in reality, thermally activated LPCVD, although the process may be localized to some degree if the light source is very narrow. If the light source simply heats the source gases, thermal fragmentation occurs as in conventional CVD processes. Ultraviolet (UV) and vacuum ultraviolet (VUV) lamps and lasers are used as energy sources. Photo-CVD has not, at least up to now, been used in production because the deposition rates are low and therefore the process is expensive.

1.5 PLASMA PROCESSING

1.5.1 Introduction

Plasma processing has become essential for depositing and etching the materials used in building semiconductor devices. The low-plasma-density capacitively coupled discharge was used exclusively in fabrication until recently, when high-plasma-density reactors became available commercially. Specific applications are discussed in Chapter 4 to Chapter 6. The reliability issues associated with plasma processing, e.g., contamination, electrical damage, surface modification, are covered in the chapters on reliability and contamination.

1.5.2 Capacitively Coupled RF Glow Discharge

When an increasing RF voltage is applied between electrodes in a low-pressure (~10 to 1000 mtorr) gas, ultimately the gas breaks down, i.e., it ionizes and current flows. A glow is observed. Adjacent to the electrodes are dark spaces, the sheaths, and a voltage drop occurs across the sheath regions. The glow region is virtually field-free; there are approximately equal numbers of positive and negative charges. Electron impact dissociation produces not only ions but also photons, free radicals, and metastables (the neutral species). The potential in this plasma region is the most positive potential in the system. Thus all electrodes (which may include the chamber walls) have a negative potential with respect to the plasma and are all bombarded by positive ions. Sputtering of the surfaces is a source of contamination making the choice of reactor materials an important issue (Vossen, 1979; Oehrlein, 1989). The relative potential (bias) developed at each electrode determines the ion bombardment energy; this is a function of their areas. If the electrodes have equal areas (symmetrical reactors), the voltage, i.e., the DC bias, is the same on both so that both are bombarded by ions of equal energy (Vossen, 1979) and the plasma potential is relatively high; the point of attachment of the power is irrelevant.

When the electrodes are unequal in area, the DC voltage is higher on the smaller one (Koenig and Maissel, 1970); if the area of one electrode is very much smaller than the other (called asymmetric systems), the bias on the small electrode is approximately one half the peak-to-peak applied voltage. The high-bias electrode is usually called the cathode. The plasma potential is low; the potential of the plasma and that of the larger electrode are approximately equal. Thus the ion bombardment energy at the very large electrode is low, but not zero. For convenience and safety, the smaller electrode is powered and the chamber (counter-electrode) is grounded. However, the

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ion bombardment on a specific electrode does not depend on which electrode is powered (Coburn and Kohler, 1987), although the plasma potential is higher when the larger electrode is powered.

In addition to the electrode potentials there is the floating potential which exists on all surfaces, neither externally biased nor grounded. This is a function of the electron mass and temperature and of the ion mass and charge.

The plasma in these reactors is a nonequilibrium plasma in which the temperature of the electrons is much higher than the temperature of the gas. The plasma density is low ~10^9 to 10^{11} cm^{-3} and the fractional ion density (i.e., the ratio of ion to neutral species) is low (~10^{-6} to 10^{-3}).

1.5.2.1 Frequencies

A range of frequencies has been used, from 50 kHz to 2.54 GHz (microwave); 13.56 MHz (or multiples) is the most commonly used frequency (no interference with communications). However, Goto et al. (1992) preferred to treat the frequency as a process parameter and have investigated the 10 to 215 MHz range. Martinu et al. (1989) used microwave (2.54 GHz) excitation. Colgan et al. (1994) suggested the use of very high-frequency capacitive discharges to obtain high plasma densities at low ion energy. An ultrahigh-frequency (UHF) 500 MHz discharge has been used in conjunction with a new antenna. In the low-frequency range, electrons and ions follow the electric field and the ions experience the full amplitude of the RF voltage resulting in higher bombardment energy of the electrode. Above ~3 MHz ions can no longer follow the field, as do the electrons. The ions interact only with the time-averaged field since it takes several RF cycles to cross the sheath. Therefore, the average energy is reduced and the electrode is bombarded with lower energy ions. However, at higher frequencies, energy coupling is more efficient so that, for a given power, the plasma densities are greater than at lower frequencies. At low frequencies the peak energy of the ions is greater than at high frequencies but the energy distribution is broader (Bruce, 1981; Coburn and Kohler, 1987; Hey et al., 1990; Meyers et al., 1994). At low frequencies the angular distribution of the ions is more directional than at higher frequencies (Meyers et al., 1994).

A two-frequency or dual-excitation mode in which both frequencies are applied simultaneously is now used frequently for independent control of the substrate bias in both reactive plasma-enhanced etching and deposition. The excitation electrode may be powered using the higher frequency and the substrate electrode powered with the lower (using appropriate filter networks). A variety of combinations have been used, e.g., 13.56 MHz/200 kHz (Tsukune et al., 1986), 13.56 MHz/450 kHz (van de Ven et al., 1988, 1990), 2.54 GHz/13.56 MHz (Martinu et al., 1989), 100 MHz/30 MHz (Goto et al., 1992). In an electrically equivalent mode of operation, *both* frequencies are fed to one electrode, e.g., 13.56 MHz/450 kHz, (Hey et al., 1990), 13.56 MHz/350 kHz (Matsuda et al., 1996).

1.5.2.2 Reactor Requirements

Whatever the electrical configuration of the reactors, whether inert or reactive gases are used, and whether used for etching or for deposition, the reactors have many features in common. Some of these are (1) the reaction chamber with the associated vacuum apparatus, e.g., pumps, pressure controllers/monitors, and the gas distribution systems with the appropriate control and monitoring equipment and (2) the glow discharge generation equipment consisting of power source(s) and, where required, an impedance matching network for efficient power transfer. It should be noted that the power to the glow discharge may be significantly less than the input power due to (undetermined) losses in the matching network (Logan, 1990) There is optional equipment for following the processes: rate monitors, e.g., interferometers, grating patterns, etc., which can act as end-point detectors in some cases. Particularly in reactive plasma etching processes, there are several other kinds of end-point detectors, e.g., optical emission spectroscopy (OES), discharge impedance and pressure monitoring systems, etc., as well as plasma diagnostic equipment, e.g., OES, mass

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spectrometry, and laser-induced fluorescence spectrometry. Unfortunately much of this equipment is often not compatible with the configuration of reactors used for manufacturing.

Many of the newer reactors used in manufacturing are integrated into multichamber processing systems (cluster tools) in which each chamber processes a single wafer (Singer, 1993, 1995). These provide not only load-locked entry into the first chamber and exit from the last but also vacuum transfer between chambers. *In situ* plasma-cleaning capability is often a feature of such systems. The chambers in the system shown in Figure 1.12b, into which a CVD reactor was incorporated, have been configured for plasma processing (PECVD and inert or reactive plasma etching) as well.

1.5.2.3 Capacitively Coupled Reactors

The earliest reactors for the commercial production of chips are what have been called planar or parallel plate diode reactors with an internal electrode capacitively coupled to an RF source. In symmetrical systems, used frequently in reactive plasma-assisted processing, there are actually two flat electrodes inside a dielectric chamber; one is powered and the other, on which the wafers are placed, is grounded. These systems are based on the radial flow reactor patented by Reinberg (1973) and are usually operated at relatively high pressures (several hundred millitorr). A schematic representation of the reactor is shown in Figure 1.10.

Asymmetrical reactors were developed for sputter deposition and etching. In these reactors there may be a counter-electrode connected to the grounded chamber enclosure (Figure 1.11a), or the grounded enclosure itself acts as the counter-electrode, as shown in Figure 1.11b. Both are called planar diodes and are operated at relatively lower pressures (tens of millitorr). An axial configuration, the so-called hexode reactor, patented by Maydan (1981) is electrically equivalent to an asymmetric planar diode system. A schematic representation of the hexode is shown in Figure 1.11c, and a sketch of the reactor, taken from the patent, is shown in Figure 1.11d.

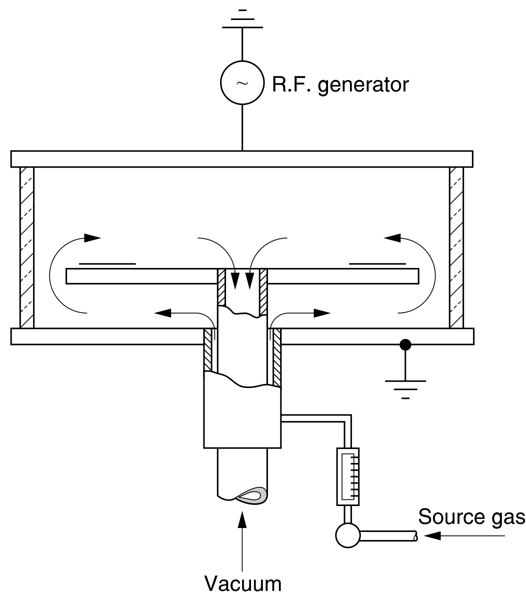

Figure 1.10 Reinberg's radial flow reactor. (From Reinberg, A.R., U.S. Patent 3,757,733, 1973.)

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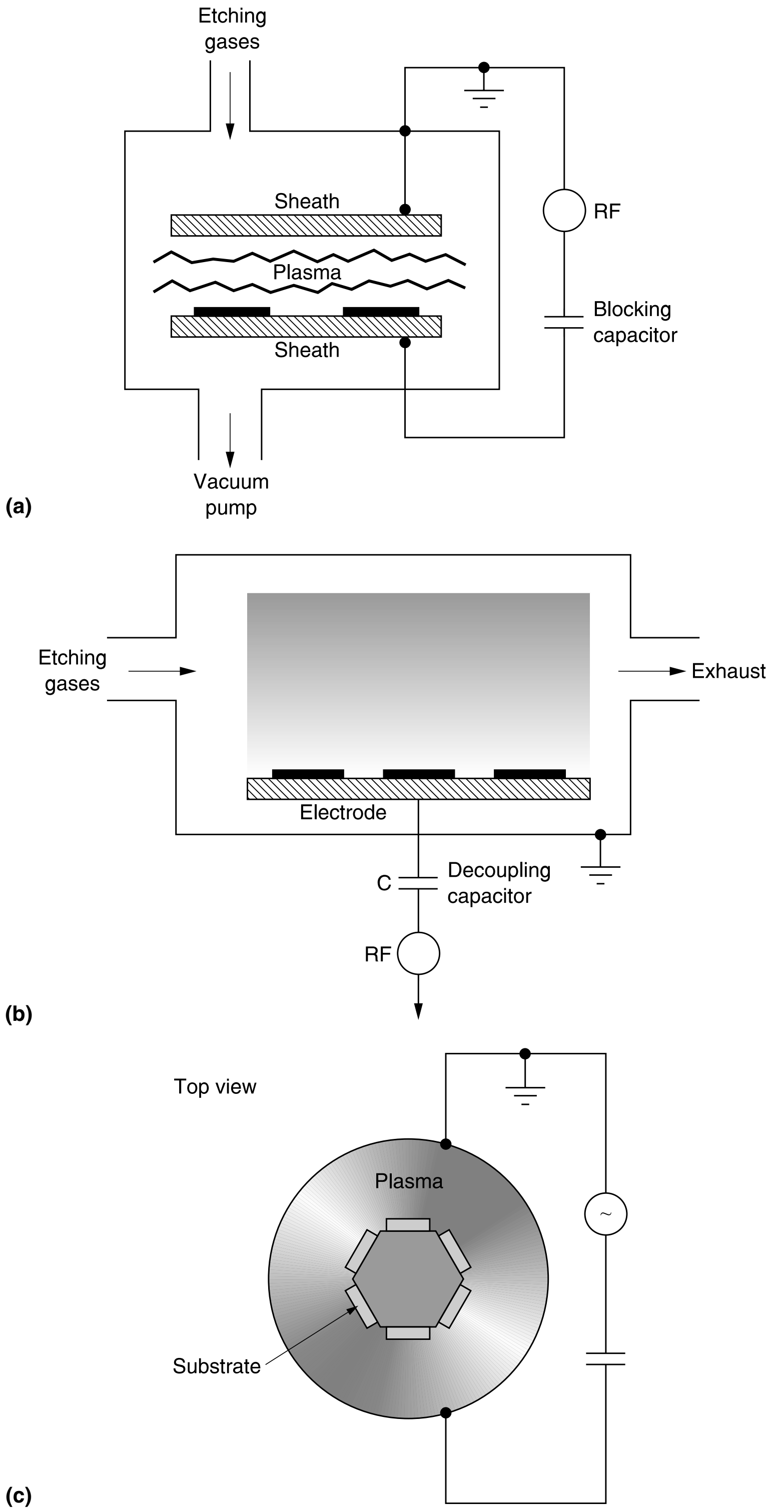

Figure 1.11 (a) Capacitively coupled asymmetric reactor. (b) Capacitively coupled reactor used for RIE. (c) Schematic of a hexode reactor. (d) Sketch of an actual hexode reactor.

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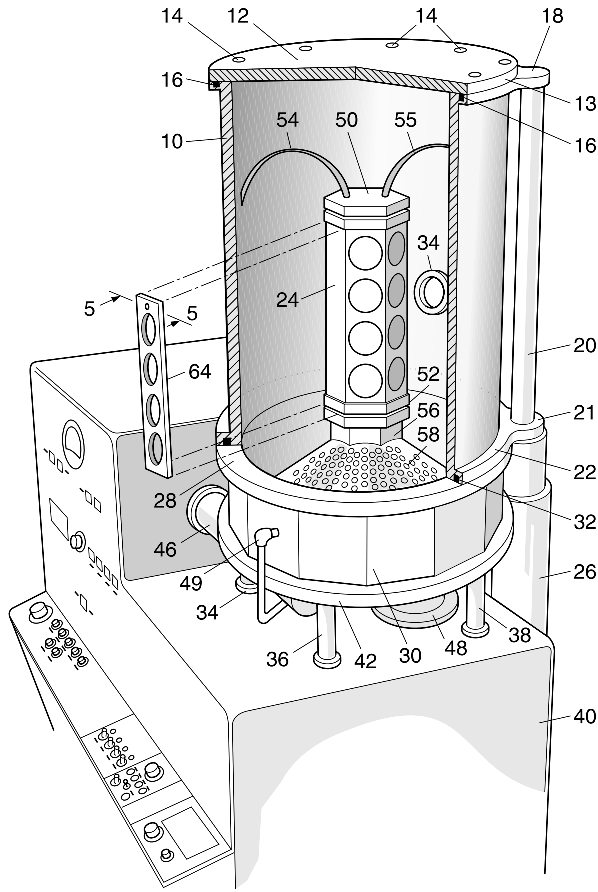

Figure 1.11 (Continued)

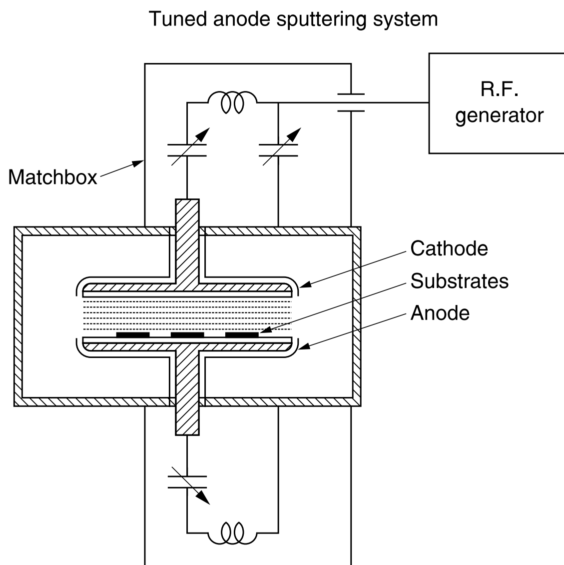

Figure 1.12 (a) Schematic of a tuned anode sputtering system. (b) Schematic of a driven anode sputtering system with two generators. (c) Power-splitting RF drive for driven anode system.

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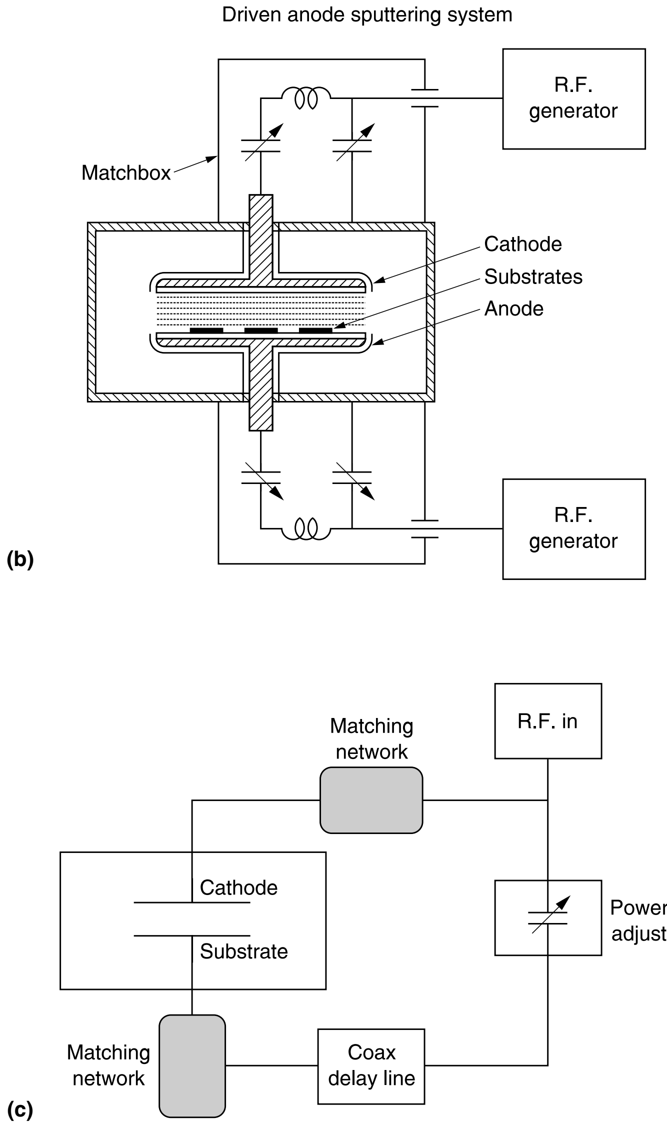

Figure 1.12 (Continued)

The dual-frequency mode of operation is described above. The triode system is an extension of the diode reactor; a third electrode is added so that the substrate bias can be controlled essentially independently of the excitation energy, using the same or a different frequency. Reactors of this kind have been called substrate-biased reactors. Substrate biasing is used to improve the properties of the deposited material. The chamber walls are grounded and the target and substrate are isolated. Two versions of a triode have been used for bias-sputtered oxide deposition: the tuned-substrate in which the bias at the substrate is controlled by a tuning network (Figure 1.12a); and the driven system in which both electrodes are powered using two RF generators (Figure 1.12b) or a single power supply and a power-splitting network (Figure 1.12c). One version, the flexible diode, shown in Figure 1.13, is a planar reactor used for etching (Ephrath, 1981a).

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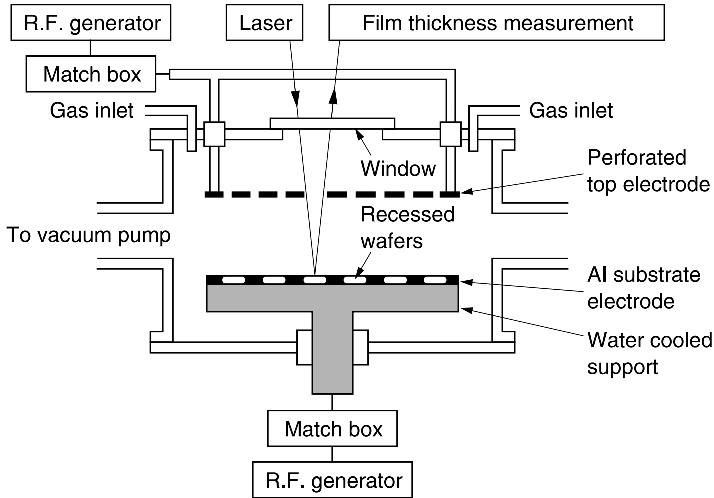

Figure 1.13 Schematic of a flexible diode RIE reactor (From Ephrath, L.M., IEEE *Trans. Electron Dev.*, ED-28, 1315, 1981.)

1.5.2.4 Magnetic Confinement

Magnetic confinement is used to obtain a high plasma density, higher ion/neutral ratio at relatively low voltages and at lower pressure than in an unconfined system. The magnetic field confines the electrons in the discharge.

1.5.2.4.1 Magnetrons

Axial magnetic fields used with a planar diode increase the path length of the electrons and keep them away from the chamber walls. In magnetron sputtering systems, the object is to trap electrons near the target to increase their ionizing effect, thus increasing the deposition rate. The electric and magnetic fields are usually perpendicular (Chapman, 1980).

The many magnetron configurations, cylindrical, circular (sputter-gun and S-gun), and planar, used for sputtering, are described extensively in Kern and Ban (1978) and in Chapman (1980). A high-vacuum planar magnetron discharge, operating at pressures at or below 1 mtorr, but with reasonable deposition rates, has been described by Asamaki et al. (1992, 1993).

Magnetron reactors in which the magnetic field lines are parallel to the cathode surface are used for reactive ion etching (RIE); these systems have been called magnetically enhanced RIE (MERIE) and magnetron ion etcher (MIE) systems. Among the various magnet configurations are the planar (Hinson et al., 1983), band, quadrupole (Hill and Hinson, 1985), and annular (Kinoshita et al., 1986).

An example of a single-wafer magnetron RIE system (Schultheis, 1985) is shown in Figure 1.14.

1.5.2.4.2 Multipoles

Multipolar confinement or surface magnetic field confinement is one in which the chamber walls and sometimes an end wall are lined with strong permanent magnets arranged in an alternating N–S arrangement, used with several kinds of reactors.

The magnets produce a series of magnetic cusps around the wall, in effect forming a magnetic bottle (Mantei and Wicker, 1983; Mantei et al., 1985; Wicker and Mantei, 1985; Kuypers et al., 1988).

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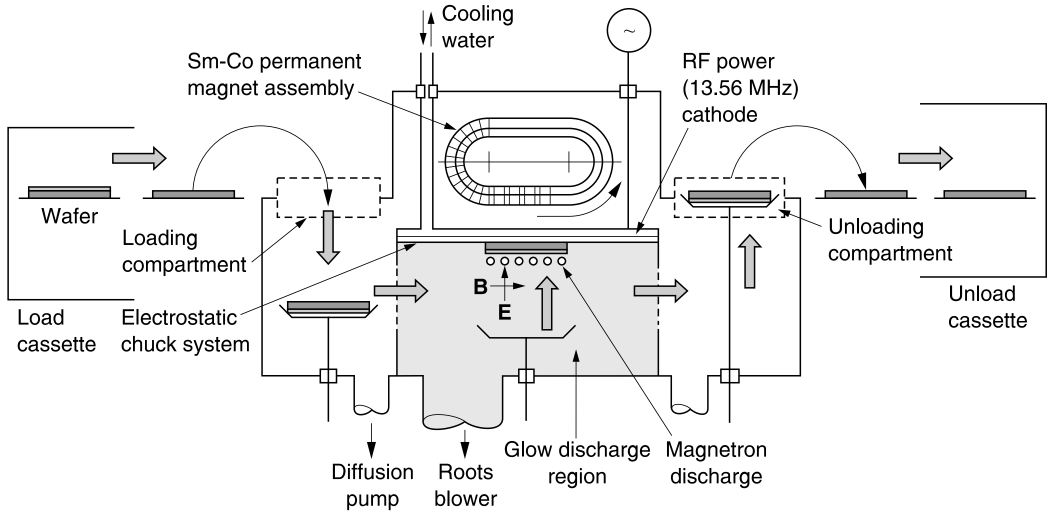

Figure 1.14 Schematic of a single-wafer magnetron RIE system. (From Schultheis, S., *Solid State Technol.*, 4/85, 233, 1985.)

The charged species are reflected by the magnetic mirror into the plasma away from the walls. In one of the multipolar reactors using a hot filament discharge, there is an increase in the plasma density of a factor of about 100 and a reduction of operating pressure to about 1 mtorr. Figure 1.15 shows a multipolar microwave reactor.

Another use of multipoles is in the magnetically confined reactor (MCR). This is a triode etcher, 13.56 MHz applied to the annular electrode and 100 kHz applied to the wafer holder and the common top electrode is grounded. The multipoles are arranged around the chamber walls and embedded in the top electrode (Engelhardt et al., 1990; Engelhardt, 1991). A similar arrangement of a grounded cylindrical multipolar bucket, but using the same frequency at both electrodes, in a triode reactor was described by Singh et al. (1992a).

Multipolar confinement has also been used with high-density discharges, which are discussed below.

1.5.2.5 Hollow Cathode

A modification of the capacitively coupled reactor is the hollow cathode (HC) configuration (Horwitz, 1989a,b; Gross and Horwitz, 1993). Plasma confinement is provided by opposing RF-powered electrodes, which increases the utilization of the ions in the discharge and provides an electron mirror by which secondary electrons are trapped. This configuration makes it possible to operate a high-plasma-density, low-voltage discharge at low pressure. This kind of system has not been developed commercially.

1.5.3 Temperature Effects

1.5.3.1 Heating

Bombardment by energetic ions heats a surface. In low-pressure environments, the heat transfer between the wafer and its holder is poor, unless a heat-conducting medium (e.g., thermal grease, a moderate pressure of He) is interposed between. The temperature rise is proportional to the ion

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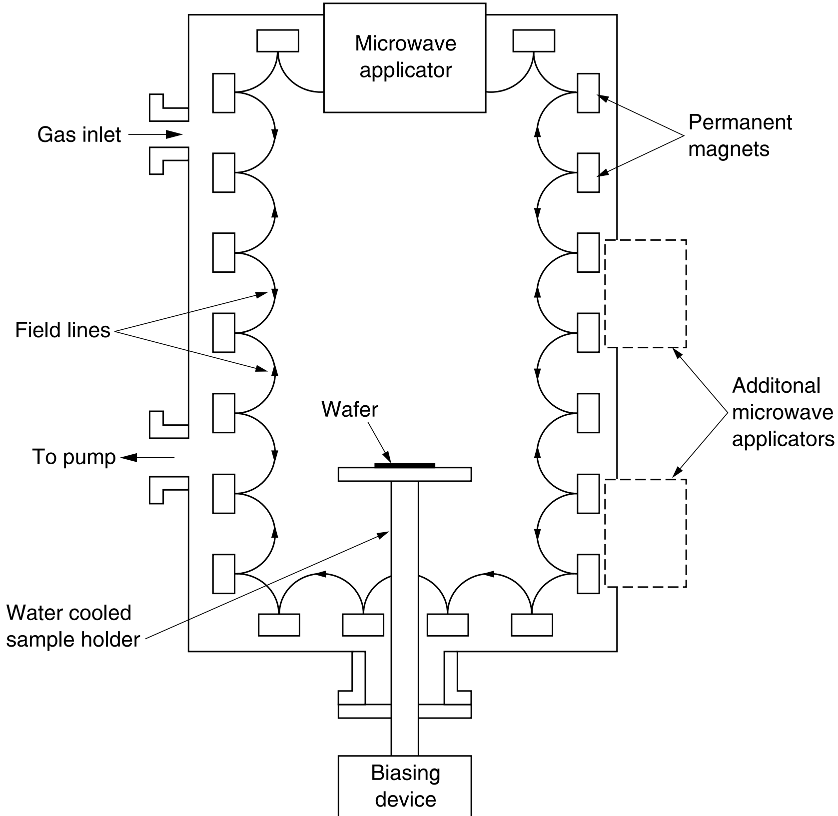

Figure 1.15 Schematic of a multipolar microwave plasma processing chamber. (From Asmussen, J., in *Handbook of Plasma Processing Technology*, Rossnagel, S.M., Cuomo, J.J., and Westwood, W.D., Eds., Noyes Publications, Park Ridge, NJ, 1989, chap. 11.)

energy, e.g., the input RF power in sputter etching (Schwartz and Schaible, 1981) or the sheath voltage in ion-driven reactive etch processes (Fortuno, 1986). If the wafers are exposed at the same time to a plasma, and one is bombarded with the full ion energy and the other is shielded, the temperature of the first wafer is significantly higher.

1.5.3.2 Temperature Control

Since many of the recently developed processes require either cooling the wafer or keeping it at a constant, uniform, and reproducible temperature, wafer clamps have been used in many reactors. At first the wafers were mechanically clamped by a ring on the topside of the wafer to the temperature-controlled wafer holder (Hinson et al., 1983; Katetomo et al., 1992), but the purely mechanical contact was often found to be inadequate. The next advance was the use of several torr of a heat-transfer gas (Wright et al., 1992), often helium, forced across the backside of the mechanically clamped wafer, as shown in Figure 1.16. However, the topside ring covers a portion of the edge of the wafer; in addition the ring may be responsible for increased contamination and nonuniformity.

Electrostatic wafer clamping is now the usual choice. This technique, which had been used earlier for, for example, holding a wafer during transport (Lewin, 1985; Kumagai, 1988; Nakasuji and Shimizu, 1992) and during lithographic processing (Clemens and Hong, 1991), uses the attractive

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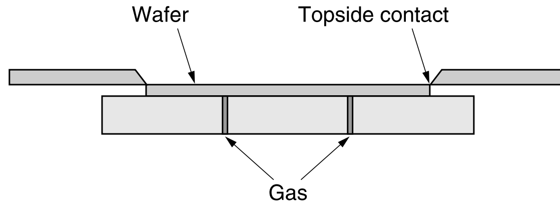

Figure 1.16 Schematic of a mechanical clamp with helium backside cooling. (From Field, J., *Solid State Technol.*, 9/94, 21, 1994. With permission.)

force between the charged plates of a capacitor to hold the wafer in place. This chuck can be installed in a plasma reactor, eliminating the need for a topside clamp, while maintaining the flow of gas across its back. There are several configurations, described by Field (1994). The configurations and equivalent circuits are shown in Figure 1.17. For each type, Field has also discussed the advantages and disadvantages, such as declamping time and device damage. There are numerous patents describing the materials used for fabricating electrostatic chucks, their structures, as well as the methods of applying the voltage. Several do not state a particular application (Lewin and Plummer, 1985a; Lewin, 1985; Ward and Lewin, 1987; Suzuki, 1987; Logan et al., 1991; Horwitz and Boronkay, 1992; Watanabe and Kitabayashi, 1992; Liporace and Seirmarco, 1992; Hongoh and Kondo, 1993; Logan et al., 1993; Barnes et al., 1993; Collins and Gritters, 1994). Others are specifically for use in a plasma reactor (Nozawa et al., 1993; Arami and Ito, 1994; Su et al., 1994).

1.5.4 Sputtering

1.5.4.1 Introduction

Sputtering is a physical process (Wehner and Anderson, 1970; Maissel, 1970; Vossen and Cuomo, 1978; Chapman, 1980; Logan, 1990; Wasa and Hayakawa, 1992) in which the positive ions in a glow discharge strike a surface and eject atoms from it by momentum transfer. About 1% of the incident energy goes into particle ejection, about 75% into heating the bombarded surface, and the rest is dissipated by secondary electrons which heat the substrate (Vossen and Cuomo, 1978). Ejection occurs when the kinetic energy of the incoming ions exceeds the binding energy of the surface atoms of a solid. Sputtering is the result of a collision cascade, a sequence of independent binary collisions; it is not a simple interaction between an incoming ion and a surface atom.

1.5.4.2 Sputter Deposition

Sputter deposition has almost always been carried out in a capacitively coupled reactor, often with magnetic enhancement and independent substrate bias control. Recently, high-density plasma reactors have supplanted these systems for some applications.

1.5.4.2.1 Sputtering Target

The solid from which the atoms are ejected is termed the "target." When used as a sputtering target for film deposition, a dense target is preferred, to eliminate the possibility of contamination, although for some materials only sintered, hot-pressed, or powder targets may be available. Since the target is heated by the bombarding ions, the backing electrode to which the target is bonded must be cooled, and the bonding material must be a good heat-transfer medium that will not be a source of contamination. Shields, often called ground shields or dark space shields, surround the back of the

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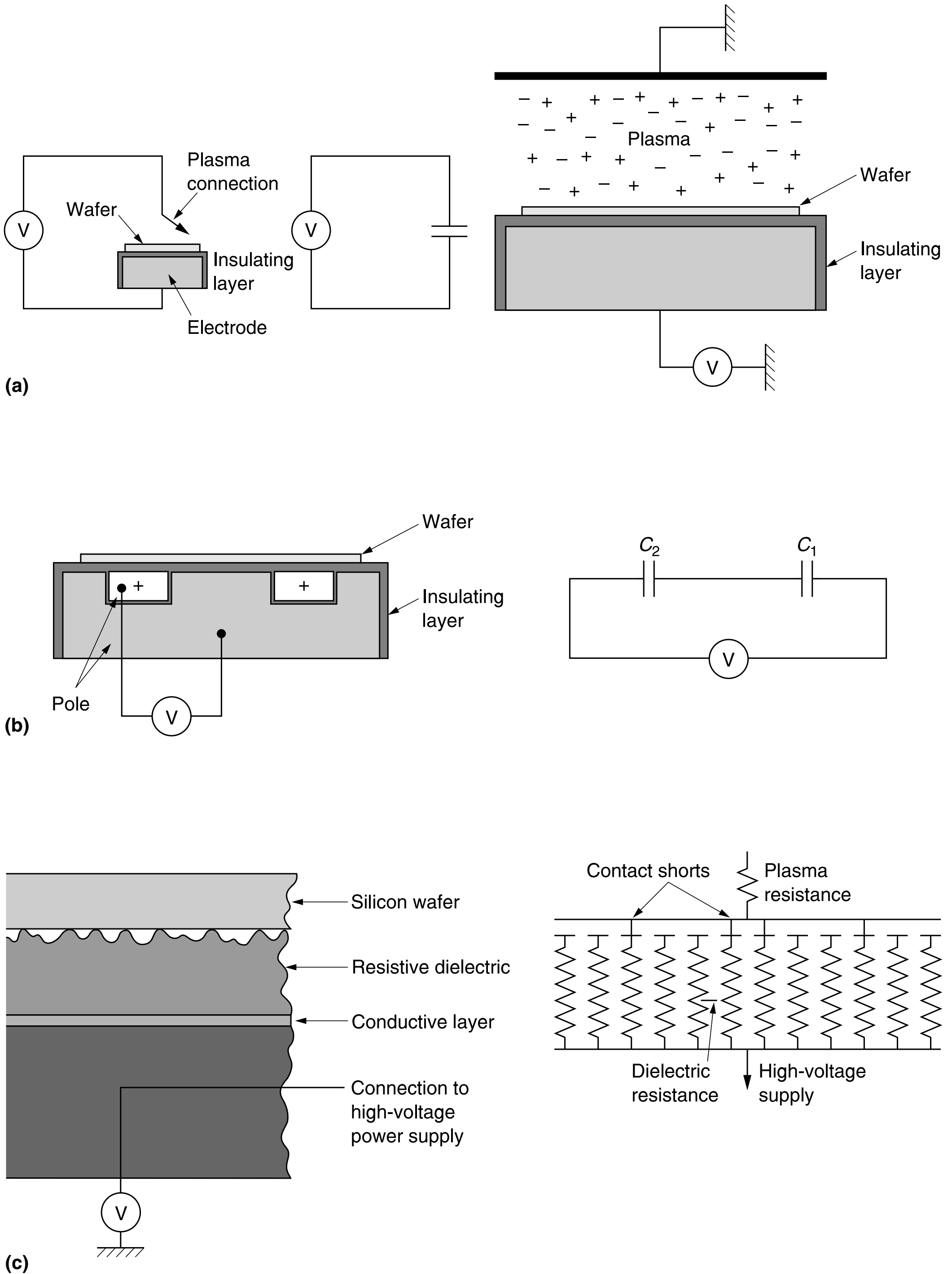

Figure 1.17 Schematic of electrostatic wafer clamps with equivalent circuits: (a) unipolar; (b) bipolar; (c) Johnsen–Rahbek configuration.

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target (placed at such a distance that no discharge will be initiated in that space) to suppress sputtering of the backing material; some shield configurations are illustrated in Chapman (1980).

1.5.4.2.2 Threshold Energy

The minimum ion energy required for sputtering is called the threshold energy which depends on the heat of sublimation of the target material; it is relatively insensitive to the nature of the bombarding ions. The sputtered material is usually monatomic, although diatomic species (e.g., SiO from an SiO_2 target (Coburn et al., 1974)) have been detected. In most sputtering processes, the ion source is solely an inert gas, most often argon, but in reactive sputtering (discussed more completely below) O_2 or N_2 is added, depending on the material to be deposited.

1.5.4.2.3 Yield

The sputtering yield is the number of atoms ejected for each incoming ion; it increases with ion energy, exponentially at lower energies and then linearly, reaching a plateau and finally decreasing at very high energy. In the low energy range of exponential increase, the yields are very low, reaching ~0.1 in the energy range used in practical sputtering. Although it is often the case that the sputtering yield increases with increasing mass of the bombarding ion, as the oft-quoted results of Almen and Bruce (1961) for inert gas ion sputtering of copper indicate, this does not appear to be true for all substrates, as perusal of sputtering yield tables reveals (Vossen and Cuomo, 1978). Molecular ions dissociate into energetic atoms upon impact with the target surface and behave as though the individual atoms arrived separately. That is, an ion X_i^+ at an energy E has the same sputtering effect as i X^+ ions at energy E/i (Steinbruchel, 1984). The sputtering yield of neutral species is the same as the corresponding ion. The effect of the angle of incidence is discussed in a separate section.

1.5.4.2.4 Film Composition

The composition of the deposited film is usually the same as that of a homogeneous target. In the case of an alloy target, composed of atoms of different sputtering yields, an altered layer forms at the surface of the target. Initially, the component with the highest sputtering yield is preferentially removed, leaving the surface enriched with the lower sputtering yield component. At steady state, the composition of the material sputtered from the altered layer onto the substrate is the same as that of the bulk target. However, if there is significant preferential resputtering from the substrate surface and/or diffusion at the target surface, the composition of the deposited film will differ from that of the source. If one of the components of the target is volatile, ion heating of the target may result in a difference in stoichiometry between the target and deposit; addition of the volatile component to the sputtering gas can compensate for this.

1.5.4.2.5 Effect of Operating Conditions

Raising the gas pressure increases the number of ions (ion current) for sputtering and, although the energy of the ions decreases, the net result is an increase in deposition rate, because the yield decreases slowly with decreasing energy in the energy range used for sputtering. At some pressure, however, backscattering in the gas will result in a rate decrease.

The flow rate of the gas does not directly affect the deposition rate, but some contaminants (from the vacuum chamber or desorbed/sputtered from the target), which would be swept out in a high flow, do affect the rate: e.g., a small partial pressure of O_2 reduces the deposition rate of SiO_2 significantly (Jones et al., 1968). And removing the contaminants also reduces the probability of incorporating them into the growing film and degrading its properties.

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Increasing the source-to-substrate distance reduces the accumulation rate but improves uniformity. The net accumulation rate decreases with increasing substrate temperature. The use of the term accumulation rate takes into account the fact that, in some instances, not all of the material sputtered from the target and arriving at the substrate remains on the surface; some of it may be resputtered or reemitted thermally.

Metals may be sputtered in a DC glow discharge, but when insulators are exposed to a DC plasma a positive charge accumulates on the surface preventing further positive ion bombardment. The use of RF sputtering, in which an RF potential is applied to a cooled metal electrode to which the insulating target is bonded, circumvents this problem. A grounded metal shield prevents sputtering from the edges of the metal electrode. In sputtering, the use of frequencies higher than 13.56 MHz can be advantageous. At higher frequencies, the ion current increases but the ion energy decreases, resulting in higher deposition rates at lower target voltages. Lowering the target voltage reduces the energy of the secondary electrons produced at the target, and substrate heating due to secondary electrons is also reduced.

1.5.4.2.6 Advantages of Sputter Deposition

There are a number of advantages to sputtering: (1) controlled stoichiometry of the deposit, (2) easy sputter cleaning of the substrates, (3) improved adhesion, (4) better control of film thickness, and (5) use of bias sputtering for improving the physical properties of the films and for step coverage/gap-fill. The improvement in film properties by the use of substrate bias can be related to the removal by the impinging ions of atoms trapped in nonoptimal surface sites and that of gap-fill/step coverage to the angle dependence of the sputtering yield and perhaps by the elevated temperature resulting from ion bombardment heating.

1.5.4.2.7 Temperature Effects

Since many film properties are influenced by the deposition temperature, temperature control is desirable. Substrate holders may be cooled or heated by various techniques, but it must emphasized that, since the substrates are heated by ion bombardment and secondary electrons, their temperatures may be different from that of the holder, unless a heat transfer medium is interposed between them. The review by Lamont (1979) contains a more extended discussion of the thermal history of substrates during sputter deposition and etching. Accurate measurement of the surface temperature is possible using fluoroptic probes, but they are difficult to implement in a system used in manufacturing, so their use in feedback controls may not be possible. Monitoring and controlling the holder temperature is more feasible, but is only meaningful when there is excellent thermal contact between it and the wafer.

1.5.4.2.8 Reactive Sputtering

Reactive sputter deposition is one way of depositing an insulator in a DC sputtering system, although RF reactive sputtering is more common. In reactive sputtering, a metal target is sputtered in a mixture of an inert gas and the appropriate reactive constituent. One reason for preferring reactive sputtering is that metal targets are usually denser and more easily fabricated than compound targets. In addition, by changing the sputtering gas mixture, several compounds can be deposited using the same target. The reaction to form the required compound may occur on the target surface, in the gas phase (unlikely), or at the substrate. Since sputtering rates of metals are higher than those of oxides, it is best to adjust conditions so that reaction occurs at the substrate; this occurs at low reactive gas partial pressure and high target sputtering rates. This effect was utilized for high-rate deposition of Al_2O_3, which has a particularly low sputter yield (Jones and Logan, 1989). The stoichiometry of the film is a function of the relative arrival rates at the substrate.

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1.5.4.2.9 Collimated Sputtering

In sputter deposition, a large fraction of the particles impinging on the substrate do not arrive at normal incidence because the atoms are emitted from the sputtering target in a cosine distribution and pressures are such that gas scattering is significant. To reduce the angular distribution of the impinging species, so that high-aspect-ratio (AR) features can be filled adequately, a collimator (an array of directional filters) can be placed between the sputtering target and the substrate in a magnetron system (Rossnagel et al., 1991; Cheng et al., 1995). A schematic of such a reactor is shown in Figure 1.18. Increasing the AR of the collimator increases the directionality of the deposit. In a modification called "dual collimation" (Kools et al., 1999) the target-to-substrate distance was similar to the target dimension and the collimator placed relatively close to the wafer (out of the plasma). It was stated that this configuration reduced the build-up, since fewer of the atoms emitted at off-normal angles reach it. In addition, the position out of the plasma reduced thermal cycling (particle generation).

Further discussion of the use of collimated sputtering for enhanced edge and bottom coverage of etched features is found in Chapter 6.

1.5.4.2.10 Long Target-to-Substrate Distance Sputtering

An alternative to collimated sputtering is sputtering using a wide separation between the target and substrate, a low pressure (~1 mtorr), a smaller target (to mimic a point source), and, possibly, a light sputtering gas. These modifications result in a narrow angular distribution of the sputtered species. The application of this technique, called long target-to-substrate (T/S) distance sputtering or long-throw distance sputtering, is discussed in Chapter 6.

Rossnagel (1998) has written a comprehensive review of physical vapor deposition, including both collimated and T/S distance sputtering.

1.5.4.2.11 Self-Sputtering

In this technique, used for depositing metals, ions of the same element are used in the absence of an inert gas. Further discussion is contained in Chapter 6.

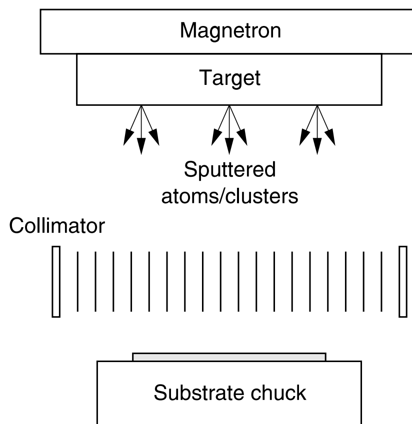

Figure 1.18 Cross-section of magnetron sputtering system with (grounded) collimators. (From Rossnagel S.M., D. Mikalsen, H. Kinoshite, J.J. Cuoma, *J. Vac. Sci. Technol.*, A9, 261 1991.)

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1.5.4.2.12 Conclusions

Although insulator films of excellent quality can be deposited by sputtering at low temperatures, defined as temperatures compatible with aluminum alloy metallization, there are a number of disadvantages to sputter deposition as practiced traditionally. One is high cost. Batch systems were used, and although such systems can be very large, the throughput is quite low. Load locks are difficult to implement in such systems so that flaking from the chamber walls during wafer load/unload becomes a major reliability problem when the flakes become incorporated into the film. The wafer temperature is a function of the input power. In order to increase the deposition rate to meet the demands of higher throughput, the power must be increased; this often results in an excessive rise in wafer temperature. Helium backside temperature control of wafer temperature is impossible to implement in batch systems. Step coverage and gap-filling capabilities are limited (although they are superior to single-pass PECVD and early low-temperature CVD) and even marginal improvement requires much extended processing time. This last is probably responsible for the lack of interest in further development of advanced reactors and in the use of sputtering for insulator deposition.

Also, there have been major improvements in alternative insulator deposition methods with, apparently, costs lower than traditional sputtering. Better low-temperature CVD and PECVD reactors and processes have been developed. The dielectric and physical properties of the films have been improved significantly, although the properties of some of them are still inferior to sputtered films. Reasonable throughput multistep processes for gap fill have been developed. In addition there has been great activity in the commercial development of high-density plasma reactors for gap-fill capability. Understanding of the interactions of reactor, process, and film properties is progressing. These factors, plus the integration of many of the processes into high-throughput, single-wafer, often integrated-chamber reactors, have essentially eliminated sputtering for insulator deposition.

Sputter deposition of metals has almost completely superceded the previously ubiquitous process of evaporation, despite the greater complexity of sputtering systems (the need for the networks in addition to the vacuum apparatus). For the most part, deposition is carried out in integrated systems, in which the individual chambers have been configured to meet the objectives of high film quality and gap-fill, e.g., bias, magnetron, high temperature, collimated, and long target-to-substrate sputtering, with vacuum transport among the various deposition chambers (if several metals are to be deposited sequentially) and to etching and annealing chambers where needed; in addition there are entrance and exit load locks.

1.5.4.3 Sputter Etching; Ion Milling

1.5.4.3.1 Introduction

Etching by means of inert ion bombardment is usually performed in a capacitively coupled diode system, which is essentially an RF sputtering system in which the wafers are placed on a holder that takes the place of the target in a deposition system. In some systems, the wafers are held against the upper electrode (cathode) facing the anode. A more convenient arrangement is one in which the wafers are placed on the lower electrode (cathode) and the chamber itself is the counter-electrode.

Another method of bombarding a substrate with ions is in an ion milling or ion beam etching system. There are several types of ion sources, among which are the Kaufman, Penning, duoplasmatron, hollow anode, and glow discharge, all of which have been described by Harper (1978).

1.5.4.3.2 Applications Other Than Pattern Transfer

Sputter etching in an inert plasma can be used for patterning, but is also used to clean surfaces before subsequent processing, e.g., *in situ* sputter cleaning, which minimizes interface resistance by

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removing an insulating surface layer from a metal before deposition of a second metal. It has also been used to roughen a surface to enhance adhesion of a second layer.

Ion milling is used in depth profiling for Auger and x-ray photoelectron spectroscopy surface analysis and as part of the process in secondary ion mass spectrometry. Other uses of sputter etching are in a process called PECVD/sputter etch and in bias sputtering and biased high-density-plasma deposition. These take advantage of the angle-dependent sputter yield in increasing the acceptance angle for incoming species. This is discussed in detail in a later section.

1.5.4.3.3 Pattern Transfer

In this section, pattern transfer by sputter etching in a glow discharge or by ion milling is treated. Patterning by sputter etching is carried out in an RF discharge by bombarding the masked substrates with positive ions formed by excitation of an inert gas (Davidse, 1971).

One of the theoretical advantages of sputter etching or ion milling is that, because of the directionality of the ions and the absence of chemical (isotropic) components, it is possible to etch without undercutting the mask and to form vertical edges. Undercutting is not observed, but often the end results are not vertical profiles due to faceting of the mask (discussed in Section 1.5.5). Masking by lithographic techniques is the first step. However, since sputter etching is a physical process, there is not the same degree of selectivity that exists when using chemical reagents, such as solutions or reactive plasmas, since all materials can be etched by ion bombardment techniques. Thus mask erosion can be a significant problem, particularly since some resists are among those materials with the highest sputtering yields. However, thick resists degrade lithographic performance. Therefore it may be necessary to add to the complexity of the process by using a thinner resist layer to form a secondary mask in a material of somewhat lower sputter yield, such as an oxide.

In addition, the resist mask can flow and change shape because of the temperature rise due to ion bombardment.

Another problem is redeposition of sputtered material. Material deposited on the sidewalls of the masking pattern will alter the profile; grooves will be narrower and lines will be wider than the original mask (Lehmann et al., 1977). Redeposition on the sidewalls can be seen in scanning electron microscopes (Gloersen, 1975) and is shown schematically in Figure 1.19.

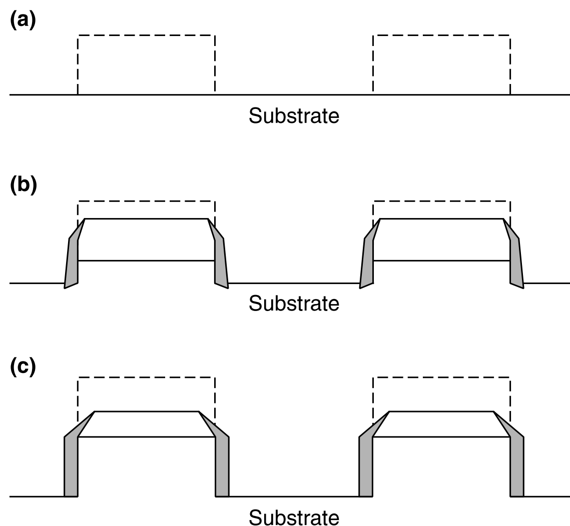

Figure 1.19 Redeposition during ion bombardment of a resist layer.

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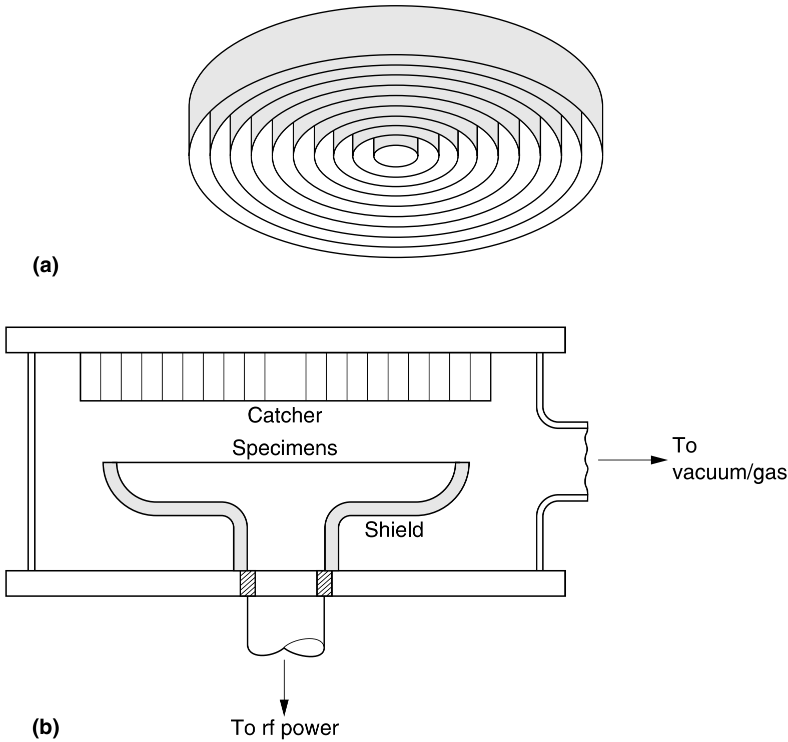

Figure 1.20 (a) Catcher plate; (b) catcher plate installed in a sputtering system. (From Maissel, L.I., C.L. Standley, and I.V. Gregor, *IBM J. Res. Develop.* 16, 67, 1972.)

Backscattered impurities can mask areas on the surface and, due to the angular dependence of the sputtering yield (see Section 1.5.5), cones can develop on the surface during sputter etching. The use of a catcher plate, a series of concentric rings with deep aspect ratios bonded to the anode of a sputter etching system, reduces redeposition (Maissel et al., 1972). A catcher plate is shown in Figure 1.20a and as installed in an etcher in Figure 1.20b.

Finally there is trenching, enhanced etching at the sidewalls of an etched feature. This is a result of increased ion flux at the sidewall (forward reflection) due to differential charging (a consequence of the difference in the angular distribution for ions and electrons) (Arnold and Sawin, 1991). Another factor in trenching is redeposition. The region close to the step will see a reduced solid angle (θ) for redeposition from above, while further out a larger angle (θ') is apparent so that more redeposition (slower net etch rate) will occur (Melliar-Smith, 1976).

The problem of faceting the mask is covered in Section 1.5.5. In ion milling there is an extra degree of freedom since the substrate (or the ion gun) can be rotated. This offers additional control of linewidths and profiles (Somekh, 1976). Etching for pattern transfer in inert plasmas has, for the most part, given way to reactive plasma-assisted etching processes, although some of the problems described above are also problems in reactive plasma etching.

1.5.5 Angular Dependence of Sputtering Yield

Many processes for step smoothing, planarization, and gap-fill depend on the fact that the sputter etch rate (ion milling yield) usually depends on the angle of incidence of the ions. When such a dependency exists, as the angle of incidence increases the rate increases, reaches a maximum, and then decreases to zero at 90°. This is illustrated in Figure 1.21. The change in rate with angle of

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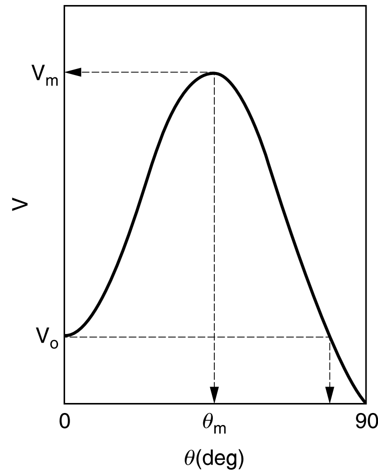

Figure 1.21 Etch rate vs. ion angle of incidence.

incidence, the angle at which the maximum etch rate occurs, and the sharpness of the maximum differ for different materials (targets) and for ions of different atomic numbers (Oechsner, 1973; Somekh, 1976; Rangelow, 1983).

Ducommun et al. (1975) gave the relationship between the angular dependences of the etch rate $V(\theta)$ (μm/min) and the sputter yield $S(\theta)$ (atoms/ion) as

$$S(\theta) = n/\phi[V(\theta)/\cos\theta]$$

where n = atomic density of target, ϕ = ion flux normal to surface ($\theta = 0$), and $\cos\theta$ accounts for the reduced current density at angles off normal. The relationship was illustrated in the paper of Ducommun et al. (1975) on ion etching of Si. It was found that $V(\theta)$ reached a maximum at ~50°, at which point $V_{max} \sim 2.3V_0$ (the value at normal incidence), whereas $S(\theta)$ reached a maximum at 65° and $S_{max} \sim 4S_0$.

The initial increase in rate from its value at normal incidence, V_0, as the angle of incidence is increased, is due to the fact that the probability of a collision resulting in an atom acquiring a component of momentum directed away from the surface increases with increasing angle of incidence, i.e., less of a directional change in momentum is required to eject an atom in the forward direction. Oblique incidence, particularly at higher energy, confines the action closer to the target surface, enhancing sputtering.

At very high angles of incidence, the rate decreases because the incoming ion flux is spread over a larger surface area and the probability of purely elastic reflection of the incoming ions is increased at large angles. Stewart and Thompson (1969), Wehner and Anderson (1970), and Lee (1979) stress the latter point. They state that at the angle at which the rate is a maximum (θ_M), reflection of the ions from the potential barrier associated with the surface plane of atoms prevents penetration. θ_M, which has also been called the critical angle, is a function of ion energy, the atomic density in the target material, and the atomic numbers of both the incoming ion and the atom being sputtered.

Increasing the atomic numbers of either ion or atom decreases θ_M, since both parameters increase the surface potential (Oeshsner, 1973).

Increasing the ion energy increases θ_M, since a more energetic ion can more easily penetrate the surface potential barrier. At the glancing angle ($\theta = 90°$) the etch rate is essentially zero. S_M/S_0 was shown to decrease with increasing ion energy for Cu (Oechsner, 1973) but to increase for Si (Dimigen et al., 1976).

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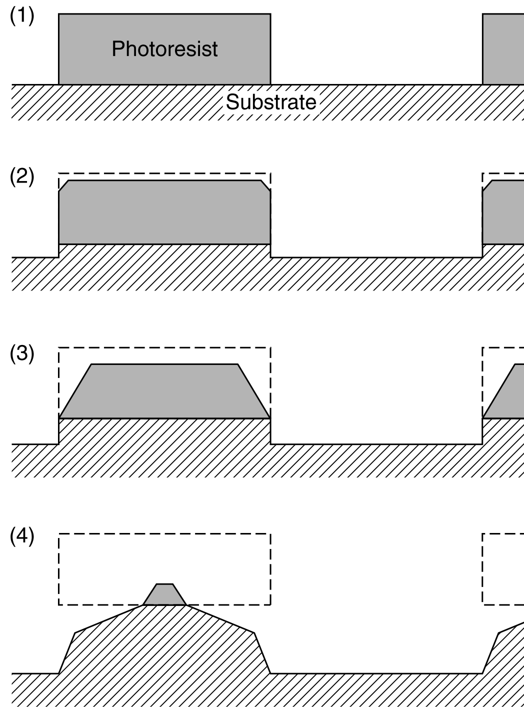

Figure 1.22 Facet formation during ion bombardment of a resist layer. (From Smith, H.I., *Proc.* IEEE, 62, 1361, 1974. With permission. Copyright 2004, IEEE.)

Thus it has been demonstrated that angled surfaces etch at a higher rate than horizontal ones when ions impinge normal to the horizontal surface; therefore sputter etching results in local planarization. The value of θ_M is important. When the angle of the edge of a structure being bombarded with ions is steeper than θ_M, a stable facet angle is formed, corresponding to θ_M; however, if the angle is less steep, there will be no change in angle. A rounded step can be eroded and thus transformed into a linear step with abrupt corners under the influence of ion bombardment (Stewart and Thompson, 1969).

The angular dependence of the sputter yield is responsible for the increased gap-filling capability in substrate-biased deposition processes, since the edges at the top of the gap become tapered which increases the acceptance angle of the incoming species.

However, the angular dependence can have an undesirable effect: it causes faceting of the edges of a resist mask, so that the edges pull back during etching. The final dimensions of the mask, therefore, will differ from those initially printed in the mask. Also, as the mask pulls back, the walls of the etched features will become tapered. The facet propagates and makes contact with the substrate surface; the two facets are propagated, as shown in Figure 1.22. The angle of the upper facet depends on the etch rate of the substrate and the rate at which the substrate is exposed. The lower facet angle is determined by the maximum angle in the rate vs. angle curve of the substrate material (Smith, 1974).

1.5.6 High-Density Plasmas

1.5.6.1 Introduction

The limitations of standard capacitively coupled plasma reactors for high-rate anisotropic etching and deposition (gap-fill) have encouraged development of high-density, low-pressure

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systems which are now available commercially. These include electron cyclotron resonance (ECR) and helicon plasma reactors, both of which are magnetically assisted. The ECR reactor is powered at a microwave frequency; the helicon reactor uses an RF source. In addition is the nonmagnetic inductive discharge using an RF power source, which is known by several names: ICP (inductively coupled plasma), RFI (RF inductive) plasma, and TCP (transformer coupled plasma).

1.5.6.2 Electron Cyclotron Resonance

This was one of the earliest of the high-density plasmas to be developed commercially for etching and deposition. It can produce a high-density plasma ($\geq 10^{13}$ cm^{-3}) at low pressure. The use of an ECR reactor for RIE was first reported by Suzuki et al. (1977) and its use for PECVD was introduced by Matsuo and Kiouchi (1983). An ECR reactor can also be used as a high-rate sputtering system (Matsuoka and Ono, 1989).

1.5.6.2.1 Principles of ECR

An electron in motion in a uniform magnetic field undergoes circular motion transverse to the magnetic field direction; the frequency of motion is called the cyclotron frequency, $W_c = eB/m_e$ (e = electron charge, B = magnetic field strength, m_e = electron mass). The magnetic energy is coupled to the natural resonant frequency of an electron gas in the presence of a static magnetic field. The resonance condition for energy transfer, i.e., for efficient transfer from the electromagnetic field to an electron, exists when the electron undergoes precisely one circular orbit in one period of the applied field. For a microwave frequency of 2.54 GHz (a frequency in common use for many applications), ECR occurs at a magnetic field of 875 Gauss. The very energetic electrons ionize the gas species creating a plasma. To obtain the highest plasma density, the microwave is launched into the resonance region from the direction in which the magnetic field is greater than the resonance field. The plasma densities obtainable in an ECR plasma are about 10 to 100 times those in an RF capacitively coupled plasma, the ion/neutral ratio is much higher (~0.1), and the operating pressure is significantly lower (~0.1 to 1 mtorr). At higher pressures (~10 mtorr) the resonance cannot be established. Due to the low pressure of operation, there are fewer collisions in the plasma and in the sheath, resulting in greater directionality of the ions. Thus, impingement of active species is more normal to the surface than in the extended source systems, the capacitively coupled sputtering, PECVD, and RIE systems. Thus, there was an inference that the process was intrinsically directional (Machida and Oikawa, 1986). However, it was realized quite quickly that substrate bias was needed for good gap filling and directional etching. Therefore, for most applications an external bias (400 kHz to 13.56 MHz) is applied to the substrate. In etching, the etch rate increases with increasing bias (Jin and Kao, 1992), and in deposition the film properties (Andosca et al., 1992) as well as good gap-fill are a function of the applied bias. The ability to fill a gap depends on the proper balance between deposition and etching (e.g., Virmani et al., 1996). This subject is discussed more fully in Chapter 6.

In an ECR system, the ion energies are low, so it was assumed that there would be no substrate damage. And, since the wafer holder was cooled, it was assumed that good films were being deposited at a very low temperature. It was neglect of the effect of substrate bias that led to these misconceptions. As mentioned previously, energetic ion bombardment of a wafer raises its temperature. A low-pressure gas is a poor heat conductor; therefore, unless additional heat transfer mechanisms are supplied, the wafer temperature must increase. In some of the early systems, in which there was no helium backside cooling, a temperature of about 500°C was reached during ECR PECVD deposition of SiO_2 (Schwartz, 1989). Ion bombardment damage is also a possibility. A schematic representation of an ECR source is shown in Figure 1.23.

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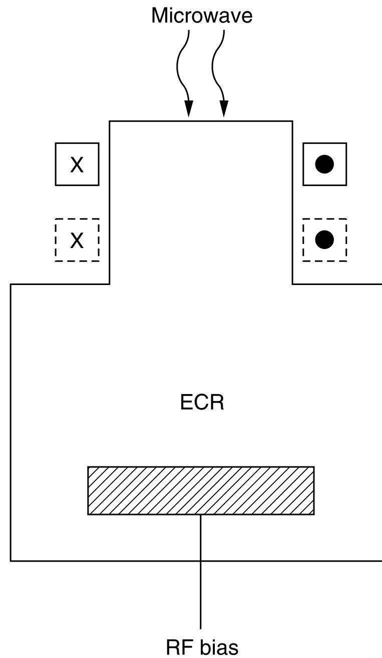

Figure 1.23 Schematic of an ECR reactor with substrate bias.

1.5.6.2.2 Divergent Field ECR

The configuration used most widely is the divergent field system; one commercially available version is shown in Figure 1.24. The microwave power is introduced into the evacuated plasma source chamber through a dielectric window. Usually solenoid coils surround the source chamber, although the use of permanent magnets has been described by Mantei and Dhole (1991) who used blocks of Nd–Fe–B, by Shida et al. (1993) who placed concentric circles of Nd–Fe–B with successive opposite polarities on the ceiling of the reactor, and by Getty and Geddes (1994) who used an array of permanent magnets arranged over the surface of the dielectric waveguide window.

The ECR position, the position at which resonance occurs, is most often within the source chamber, although advantages of locating it closer to the wafer surface have been reported (Fukuda et al., 1988). The plasma is extracted from the source chamber along divergent magnetic field lines; the magnetic flux density decays and approaches zero in the neighborhood of the wafer. As the electrons are extracted, an electrostatic potential is created which pulls the ions in the same direction toward the wafer.

1.5.6.2.3 Uniformity in a Divergent Field ECR Reactor

Multipolar magnets have been placed around the reaction chamber to confine the plasma (Mantei and Ryle, 1991; Nihei et al., 1992). Another approach was to place a pair of solenoid coils beneath the substrate holder. The inner coil (current flowing in direction opposite to main coil current) generates a cusp magnetic field to make the plasma distribution at the wafer more uniform; the outer coil (current in same direction as main coil) generates a mirror magnetic field which confines the plasma, resulting in a narrow ion energy distribution (Matsuoka and Ono, 1987; Araki et al., 1990).

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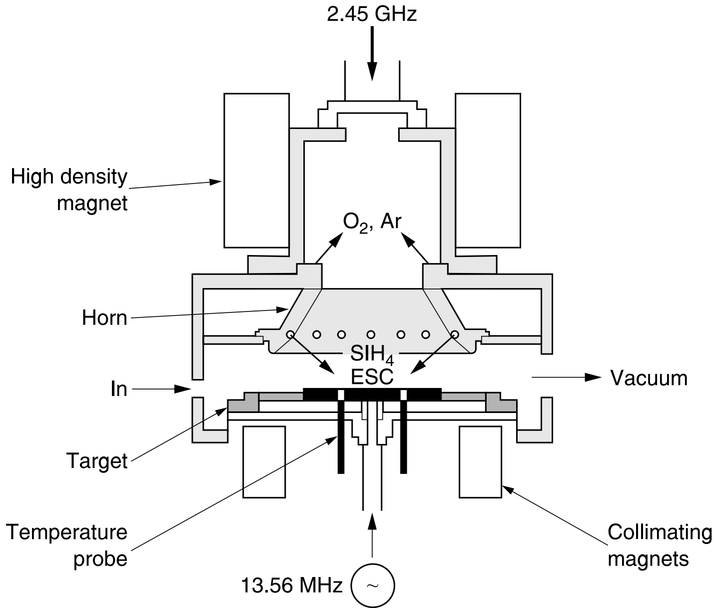

Figure 1.24 Commercial ECR reactor with substrate bias and solenoid coils. (From Denison, D. and W.R. Harshbarger, DUMIC, 1995, p. 318.)

1.5.6.2.4 Other ECR Reactors

The other configurations are the microwave multipolar plasma (MMP) and the distributed (DECR) reactor (Burke and Pomot, 1988, 1989). These are other examples of the use of multipolar confinement with ECR microwave excitation. MMP is the term used for surface wave excitation. In this system, a silica tube is inserted into an opening of a waveguide to create localized excitation and subsequent diffusion into a multipolar magnetic structure, as illustrated in Figure 1.25a.

In DECR, the ferrite multipole magnets create the resonant field for ECR excitation within the reactor chamber a few millimeters from each pole face. The microwave energy is applied by a set of tubular conductors placed around the chamber to distribute the plasma excitation around the chamber walls; one of these is shown in Figure 1.25b. Figure 1.25c shows the principal plasma zones: the ECR cusps, the lobes, and the diffusion plasma. The lobes, developed by the alternating polarity of the multipoles and trap electrons, contribute additional ionizing regions.

Although DECR systems have been developed commercially, they do not appear to be used to any great extent in device fabrication. Reports about the use of microwave plasmas using multipolar confinement are concerned with etching (Arnal et al., 1984; Pichot, 1985; Pomot et al., 1989; Cooke and Pelletier, 1989) and deposition (Cooke and Sharrock, 1990; Plais et al., 1990, 1992).

1.5.6.3 Radio-Frequency Induction (RFI)

1.5.6.3.1 Introduction

Some of the earliest examples of glow discharges were those produced in tubes wound with coils (later used as barrel ashers and neutral-species-dominated reactive plasma-assisted etchers). These were operated at high pressures. It was a matter of controversy whether these discharges

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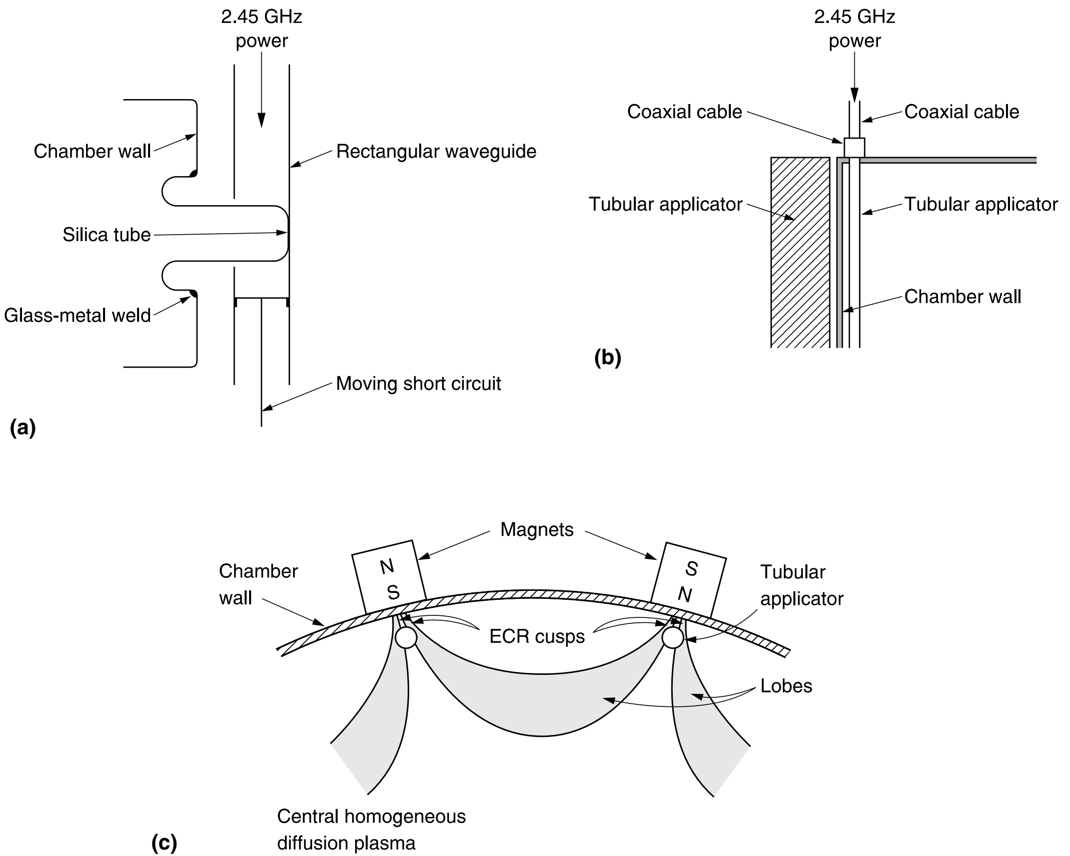

Figure 1.25 Microwave multipolar plasma configurations: (a) hybrid surfaguide excitation source; (b) tubular applicator of microwave energy; (c) tubular applicators surrounding a chamber showing cusps and diffusion plasma. (From Burke, R.R. and C. Pomot, *Solid State Technol.*, 2/88, 67, 1988. With permission.)

were capacitive (plasma coupling to the ends of the coil) or inductive (induced electric field inside the coil). It was finally concluded that at low plasma densities (low power, high pressure) the discharge is capacitive (electrostatic origin, E discharge, faint glow); as the power is increased there is a transition to the inductive mode (electromagnetic origin, H discharge) (Amorin et al., 1991).

1.5.6.3.2 Principles

The low-pressure, high-density inductive discharges are those of interest since they meet the requirements for processing advanced devices. To quote Keller (1996):

> In an RF induction system, power is coupled from the RF coil to the plasma which acts as a single turn secondary of a transformer.

These plasmas are known by various names: RFI (radio-frequency inductive (plasma)), ICP (inductively coupled plasma), and TCP (transformer-coupled plasma). A review by Keller (1996) gives details about the features of these systems.

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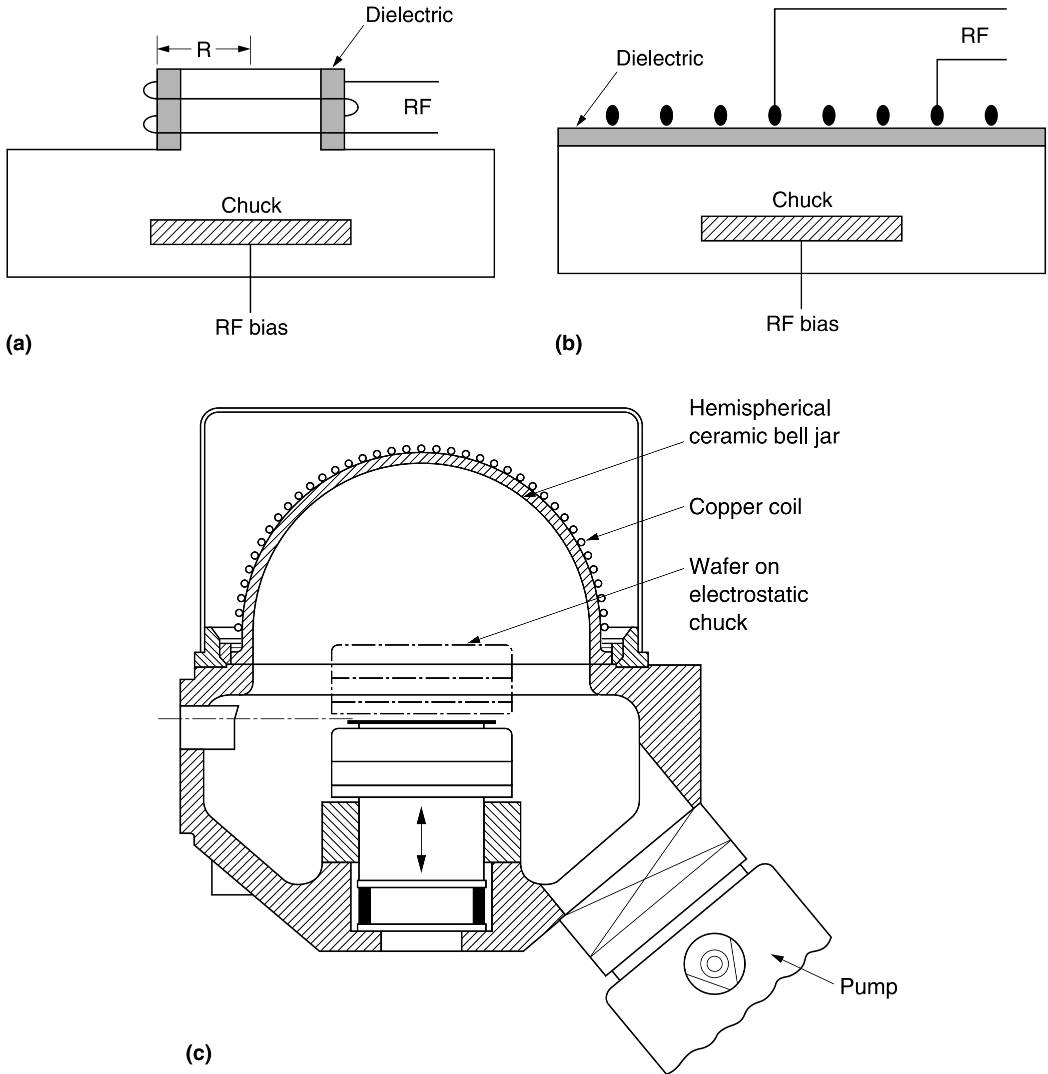

Figure 1.26 Schematics of inductively driven sources: (a) cylindrical; (b) planar; (c) hemispherical. (From Mountsier, T.W., A.M. Schoepp, and E. van de Ven, *Electrochem. Soc. Ext. Abstr.* 485, PV 94-2, 770, 1994. With permission of the Electrochemical Society, Inc.)

Two coil configurations are used: cylindrical (wrapped around the source chamber) (e.g., Cook et al., 1990) and planar (electric stove coil) (Ogle, 1990; Keller et al., 1993). These coils can also be fashioned to give hemispherical coil shapes, as disclosed in a patent by Benzing et al. (1995) and first described in the literature by Mountsier et al. (1994). These reactor configurations are shown schematically in Figure 1.26.

Keller (1996) used a 13.56 MHz power supply to drive a flat coil placed over a thick dielectric window; this reduces capacitive coupling. The length of the reaction chamber is small so that the plasma diffuses only a few mean-free paths from source to substrate; this contributes to high plasma production efficiency by reducing loss to the walls. It also minimizes the ion density loss characteristic of divergent systems. Multipolar confinement improved the uniformity. The wafer was held by a He-backed electrostatic clamp and was independently biased using a 40.68 MHz capacitively

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coupled source. The plama potentials are low: densities of ~10^{12} cm^{-3} can be achieved at an operating pressure as low as 1 mtorr.

There are capacitive as well as inductive components to the energy coupling in this kind of system. At low power (low degree of ionization) the capacitive mode dominates; therefore, these reactors are not operated in this regime. Even in the best operating range, there still exists some degree of capacitive coupling to the plasma; thus the dielectric window can be etched. This is not a problem when using reactive gases producing volatile Si compounds. However, in etching polymers in an O_2-based plasma, the window is sputtered and the involatile particles act as micromasks. Faraday shielding between the coil and the window reduces sputtering of the window significantly, but this makes starting and sustaining the plasma at low pressures more difficult and may reduce the efficiency of power transfer to the plasma. The capacitive coupling may be reduced by electrically grounding the turn of the inductor adjacent to the vacuum window (Forgotson et al., 1996) and by the application of a weak axial magnetic field (Kim et al., 1997).

Inductively coupled reactors are now used in chip fabrication; they are available from, among others, Lam and Applied Materials. The use of a very high frequency, 100 MHz, instead of the usual 13.56 MHz, was found to result in a higher degree of dissociation of C_4F_8 but there is less dissociation of high-order radicals so that F radical generation was suppressed (Nakagawa et al., 2002).

A lower frequency, 0.46 MHz, was used in a hemispherical ICP source (Benzing et al., 1995; Tuszewski and Tobin, 1996) which was operated at 5 mtorr. Up to 2 kW of RF power was efficiently coupled to the plasma. The radial uniformity of the plasma was excellent.

1.5.6.3.3 Ionized Metal Plasma (IMP) Deposition

In this modification of an RFI system (Figure 1.27), the metal atoms from a DC magnetron cathode are ionized in an RFI discharge on their travel to the biased substrate (e.g., Rossnagel and Hopwood, 1992; Rossnagel, 1998). This technique is more efficient (lower cost) than collimated or long T/S sputtering and has largely replaced them. Uses for IMP include deposition of seed layers for electrochemical deposition of Cu (Section 1.6.2 and Chapter 5) and of liners/diffusion

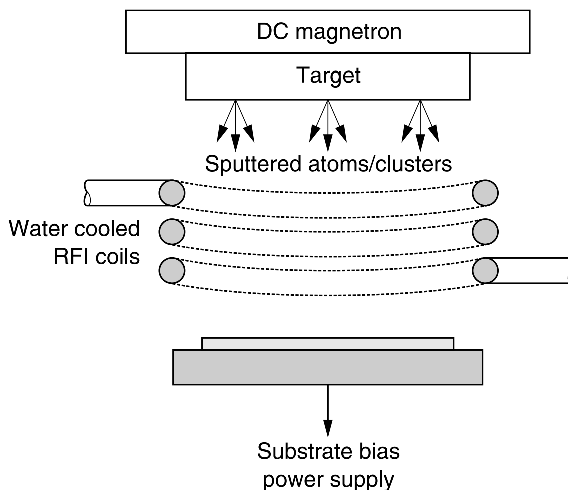

Figure 1.27 Essentials of the reactor used for magnetron sputter deposition using an RF inductively coupled plasma (ionized metal plasma, IMP). (Adapted from Cheng, P.F., S.M. Rossnagel, and D.N. Ruzic, *J. Vac. Sci. Technol.*, B13, 203, 1995.)

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barriers used for Cu interconnections (Chapter 5). The system itself is explored in greater detail in Chapter 6.

1.5.6.3.4 Magnetic Neutral Loop Discharge (NLD) Plasma

This system is shown schematically in Figure 1.28. There are coils around the chamber to produce a 13.5 MHz inductive discharge and three 4.8 Gauss magnets to produce the neutral loop. The direction of the field of the middle magnet is opposite to that of the upper and lower ones and thus the loop is established in the neighborhood of the middle magnet (Chen et al., 1998, 1999; Nakagawa et al., 2002). Electrons are accelerated every half cycle by the RF electric field. The motion induced by the field around the neutral loop thermalizes the accelerated electrons without collisions. The result is a high-density plasma and low electron temperature. The plasma can be generated at pressures well below 1 Pa. An RF bias is applied to the electrode holding the sample. Uniform etching is obtained by moving the magnetic neutral loop radially and vertically (Chen et al., 1998, 1999).

1.5.6.4 Helicon Sources

These reactors, used for plasma processing, were first described by Perry and Boswell (1989) and Perry et al. (1991). A schematic representation of a reactor using a helicon wave source is shown in Figure 1.29.

A high-density plasma is generated in the source chamber by coupling a 13.56 MHz RF source to an antenna which surrounds the chamber. The source solenoid is required for coupling the RF source into a helicon mode in the plasma for efficient transfer of energy into the center of the plasma (Boswell, 1989). In this system, the plasma potential is low, and the substrate bias is controlled independently of the plasma excitation voltage. The plasma diffuses from the source to the

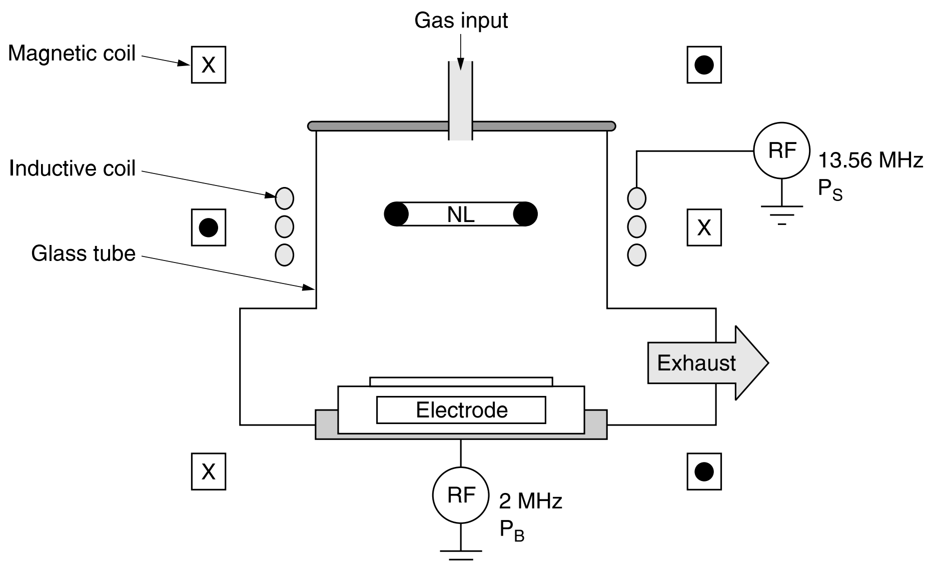

Figure 1.28 Schematic cross-section of a magnetic neutral loop discharge (NLD) plasma etching system. (Adapted from Chen, W., M. Itoh, T. Hayashi, and T. Uchida, *Jpn. J. Appl. Phys.*, 37, 332, 1998; Nakagawa, H., Y. Morikawa, M. Takano, E. Tamaoka, and T. Hayashi, *Jpn. J. Appl. Phys.*, 41, 5775, 2002.)

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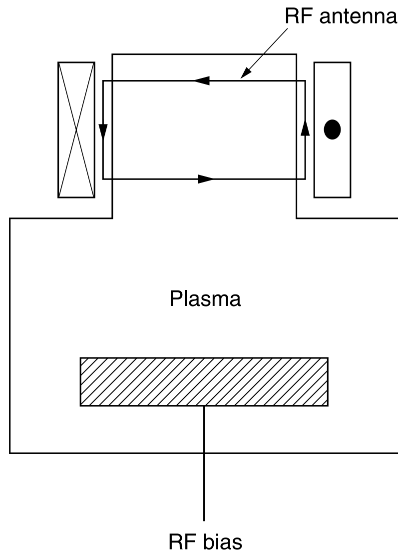

Figure 1.29 Schematic of a helicon reactor.

reaction chamber, where it is confined by the axial field produced by the chamber solenoid or by multipoles (Boswell et al., 1989). Another option is to combine the source and process chambers or to place the wafer very near the source exit in order to increase the ion and neutral fluxes and reduce the spread in ion energy. At a pressure of 3 mtorr, average densities of 3×10^{11} to 5×10^{11} cm^{-3} were obtained in the reaction chamber for an input power of 500 W. Densities above 3×10^{13} cm^{-3} have been achieved in a small helical discharge reactor using 2 kW RF power (Chen and Chevalier, 1992). Plasma-assisted etching in a helicon reactor has been called "resonant inductive plasma etching" or RIPE (Henry et al., 1992).

A commercially available helicon plasma reactor offered by Trikon Technologies, Inc. is called the MORI (magnetic zero resonant induction) plasma system. It differs from the scheme discussed above by the addition of a second electromagnet to control plasma uniformity. The lower chamber is made of aluminum, surrounded by permanent magnets to minimize electron losses to the wall. It can be operated in the helicon, RIE, and downstream modes (Thomas et al., 2001).

1.5.6.5 Concluding Remarks about High-Density Reactors

As noted above, the high-density plasma systems use an RF-biased wafer holder so that the flux of ionic and neutral species (determined by the microwave power in the ECR system or RF power fed to the inductive coil in an RFI (ICP, TCP) system) and the ion energy (determined by the bias voltage at the wafer) can be varied independently, a very useful flexibility.

ECR, RF inductively coupled, and helicon reactors are similar in their ability to achieve high plasma densities at low pressure, so that deposition and etching results are also similar. All can be configured with multipolar confinement. It is said that the inductive and helicon systems are less complex, easier to maintain, and less susceptible to failure than the ECR systems. ECR reactors, although the first to be in commercial production, appear to have been almost completely displaced by the RF systems.

A more complete discussion of the physics and design of high-density plasma sources can be found in Lieberman and Lichtenberg (1994) and Lieberman and Gottscho (1994).

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1.5.6.6 Ultrahigh-Frequency (UHF) Source

In this reactor, a spokewise antenna is located on a quartz plate separating it from the vacuum chamber. The UHF (500 MHz) power propagating between the spokes is efficiently coupled into the plasma both inductively and capacitively. The plasma is very uniform, has a high density (without the need for a magnetic field), has a low ion and neutral temperature, and can be operated at higher pressures than can ECR plasmas, but collisional broadening is negligible (Samukawa et al., 1995; Samukawa and Nakano, 1996).

1.5.7 Plasma-Enhanced CVD

1.5.7.1 Introduction

PECVD is carried out in a nonequilibrium glow discharge. Impact dissociation by high-energy electrons results in the formation of highly reactive species (largely free radicals) that normally are formed at high temperatures. It is possible to form materials with unique chemical, physical, and electrical properties in the highly reactive plasma (Hess, 1984). Among these are materials of importance to the semiconductor industry such as the oxides and nitrides of Si, Ti, Ta, etc., BN, SiBN, SiOBN, amorphous and polycrystalline Si, amorphous C, some metals, silicides, etc., and a variety of other materials used for applications not considered here (e.g., Nguyen, 1986).

Because of the complex mix of potential precursors (which makes possible the variety of PECVD films) and the large number of independent and interdependent operating parameters, control and reproducibility of films and processes are often difficult. Despite difficulties, the ability to form high-quality insulating films at substrate temperatures ($\leq$450°C) compatible with aluminum alloy-based metallization has led to the extensive use of PECVD in semiconductor manufacturing. PECVD has been used predominantly for depositing interlevel dielectric films; oxides have been the chief product but more recently low ε films such as SiOCH and α-SiC:H have been formed by this technique. Nitrides for passivation and moisture/Na^+ barriers and polish stops are another application. A variety of materials have been deposited to be used as diffusion-barriers, seed layers for electrodeposition, barrier layers for multilevel masks, in addition to metals as interconnections.

1.5.7.2 Mechanisms

The kinetic reactions are the same as those for CVD, except that plasma-initiated radical formation replaces thermally activated precursor formation (Hess and Graves, 1989). The growing film is subjected to bombardment by energetic species in the plasma; this influences film properties and deposition characteristics (e.g., gap-fill, described in a later section). Ion bombardment has been cited as largely responsible for the excellence of the films deposited at a relatively low temperature at a relatively high rate (Hess, 1984; Claasen, 1987; Hey et al, 1990). However, there is the possibility of radiation damage to sensitive devices and methods for eliminating, or at least minimizing, it are discussed elsewhere in this book.

The mechanisms of the reaction(s) occurring on the surface and in the gas phase prior to adsorption have been studied but are not discussed in detail in this book. More information can be found in a review by Hess and Graves (1989). Some of the models that may help in understanding the process or film properties are discussed in the sections dealing with specific films. However, at times experiments have been performed, for the sake of simplicity and ease of interpretation, using system configurations and/or operating conditions very different from those used in deposition for device applications, making universal application of the results and models somewhat questionable.

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1.5.7.3 Reactors

PECVD reactors use capacitively coupled or high-density discharges; the basic properties and attributes of these plasmas are described earlier in this chapter.

1.5.7.3.1 Capacitively Coupled Discharges

One of the earliest mentions of the deposition of silicon oxide films in an RF glow discharge was by Alt et al. (1963), but details of the system, beyond the use of a fused quartz reaction chamber, were omitted. Ing and Davern (1965) and Sterling and Swann (1965) described tubular (barrel) reactors, powered by external RF coils or plates. These were found to be unsuitable for commercial application.

The use of PECVD films in semiconductor manufacturing can probably be dated from the introduction of the radial-flow capacitively coupled parallel-plate diode reactor with internal electrodes, to which an RF source was connected, patented by Reinberg (1973). This basic design, used for batch processing, had been used in many commercially available systems; some of the differences among them include gas-flow pattern, gas introduction method, electrode design, and RF frequency. One of these batch reactors is shown in Figure 1.30 in which the flow pattern of the gases, from center to edge, is in the direction opposite to that in the Reinberg reactor (Figure 1.10).

Reactors using magnetic enhancement of the discharge have been described (Kaganowicz et al., 1984). A departure from the conventional design for batch processing is a hot-wall tubular

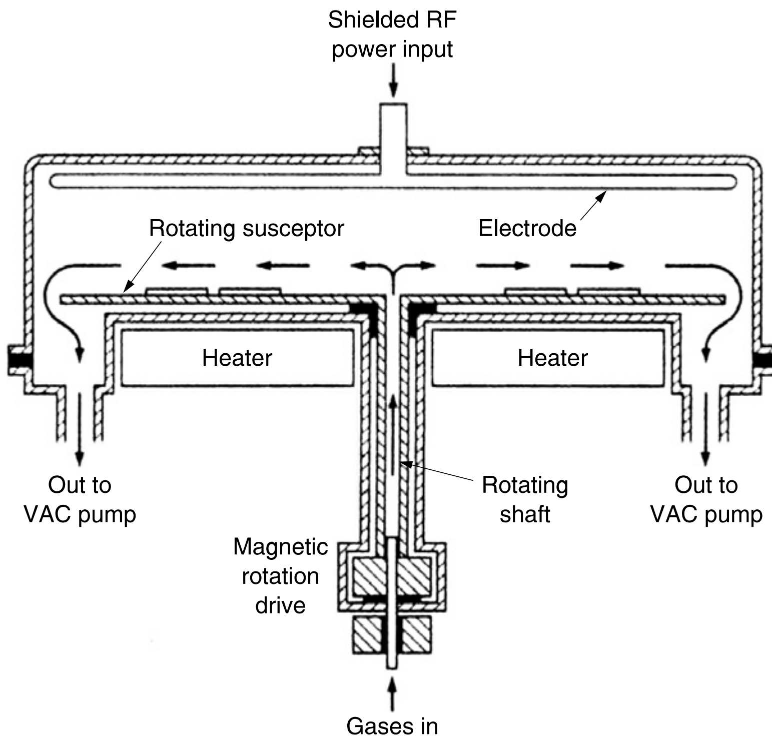

Figure 1.30 Applied Materials batch PECVD reactor.

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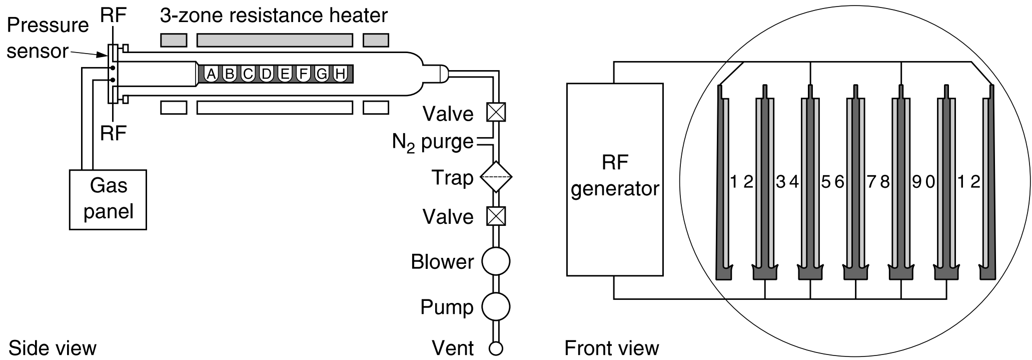

Figure 1.31 ASM/PWS batch PECVD reactor. (From Rosler, R.S. and G.M. Engle, *Solid State Technol.*, 12/79, 88, 1979. With permission.)

system (resembling a hot-wall LPCVD reactor) with internal graphite electrodes, illustrated in Figure 1.31. It is also available commercially from ASM/PWS (Rosler and Engle, 1979).

Another variation was a stepped batch process reactor: a cassette-to-cassette linear multiple-station reactor in which one fifth of the total film thickness was deposited at each station, using a vibrating track transfer mechanism. The mechanism was not reliable and, in addition, was responsible for particulate contamination. It had a short commercial life (Rosler, 1991).

The early reactors were batch systems. The deposition rates were low, but the throughput was adequate because many wafers were processed simultaneously. However, defect levels were relatively high because deposits would form on all surfaces and could flake when they became too thick or were exposed to the atmosphere. Thus system cleaning was a major problem. The introduction of load locks reduced the severity of the latter problem.

Among the next advances, using a parallel-plate reactor, is the Applied Materials 5000, shown in Figure 1.9, used with RF activation of the incoming gases. Processes in this system have been discussed by Law et al. (1987), Spindler and Neureither (1989), and Bader et al. (1990). In this integrated system are the PECVD module, etch chambers with inert and reactive gases, and a low-temperature CVD reactor.

At about the same time there was a more successful reintroduction of the continuous or multiple-station system (van de Ven et al., 1987). Here, the configuration was circular, with cassette-to-cassette load/unload in a vacuum load lock. In the first version, one seventh of the total thickness was deposited at each of seven stations, heated resitively; each station had its own showerhead for gas and RF distribution. An improved wafer transport mechanism reduced contamination. The system is shown in Figure 1.32. As the wafer size increased, fewer wafers could be accommodated and so a larger fraction of the total film was deposited at each station. This was among the first commercially available PECVD systems to use a two-frequency mode of operation (Martin et al., 1988; van de Ven et al., 1990).

These systems used *in situ* cleaning as well as load locks. Deposition rates are high, so that the throughput is comparable to batch systems.

1.5.7.3.2 High-Density Plasmas

High-density systems, described in Section 1.5.6, are available commercially and have been used successfully for PECVD; they have largely replaced the older systems. Their use for depositing PECVD SiO_2 is discussed in Chapter 4.

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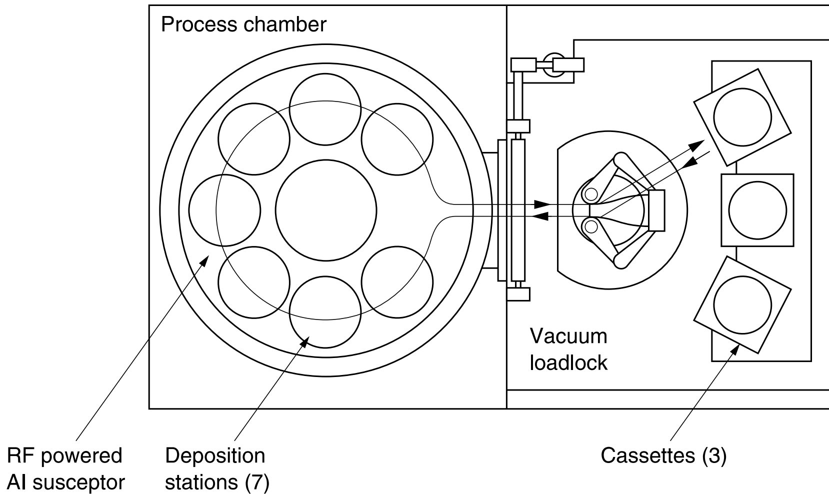

Figure 1.32 Novellus multiple-station chamber for PECVD.

1.5.7.3.3 Other Reactors

There are other systems that have not been used to any great extent in device fabrication but are mentioned here for the sake of completeness. One is called remote PECVD (RPECVD), often used for basic studies of the mechanism of film formation. In these reactors, N- or O-containing species are excited by an RF plasma, then transported out of the glow to react in the vicinity of the substrate with unexcited silane to form a nitride or an oxide (Helix et al., 1978; Meiners, 1982; Richard et al., 1985; Lucovsky et al., 1989, 1991). There are also the downstream or afterglow systems that operate on similar principles but use microwave excitation to produce the active species (Robinson et al., 1987; Spencer et al., 1987).

1.5.8 Reactive Plasma-Enhanced Etching

1.5.8.1 Introduction

The use of substrate-biased reactive plasma-assisted etching processes has replaced wet etching and sputter etching. Although sputter etching shares many of the substrate-biased reactive techniques, such as directionality of etching, compatibility with automation and vacuum processing, and relative cleanliness, the selectivity, enhanced rates, and versatility of the reactive process has made it the process of choice for pattern transfer in semiconductor fabrication.

One of the major advantages of these processes is the ability to achieve anisotropic etching, i.e., etching without undercutting the mask, so that small features can be etched with fidelity, or as it is sometime phrased, the "critical dimensions" defined by the mask can be maintained. However, anisotropy does not *always* mean a vertical profile. If the mask does not have vertical edges or if the mask edges shift during etching, due to temperature effects or lateral etching, then the resulting profile will be tapered.

The directionality of etching, which is a key advantage of these processes, does present a problem when the film to be etched has been deposited over a steep step, as shown in Figure 1.33. Since the thickness of the film to be etched is much greater at the sidewall, long overetches are required to clear the step, making great demands on the masking layer and requiring large film/substrate etch rate ratios.

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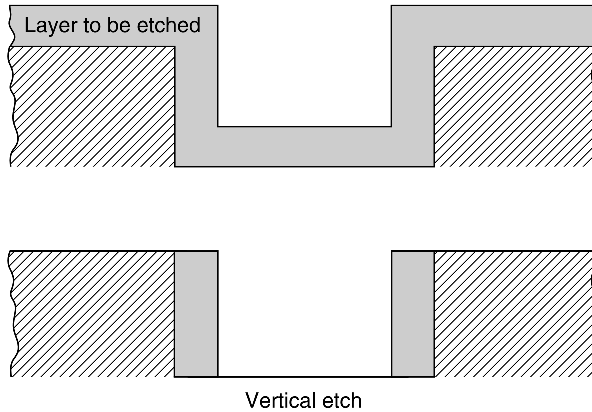

Figure 1.33 Schematic representation of anisotropic etching of a film deposited over a vertical step.

These processes are carried out in nonequilibrium glow discharges of reactive gases, and in the same kinds of reactors as PECVD, e.g., capacitively coupled diodes, with and without magnetic enhancement, triodes, and high-density plasmas (ECR, RFI, and helicons). The basic steps are similar to those in PECVD: species generation, transport, adsorption, reaction, desorption of volatile species, and finally pump-out. The basic requirement of plasma-assisted etching is the production of a reaction product that is volatile or can be desorbed readily under the influence of ion bombardment. The chemical reactivity of the radicals produced in the discharge results in higher etch rates and greater selectivity between the film to be etched and the substrate and mask than that obtained by physical sputter etching in inert (nonreactive) plasmas. Chemical etching is isotropic. However, if an adequate bias is applied to the substrate, the ion bombardment responsible for the directionality of sputter etching contributes an anisotropic component which, in a sense, competes with or complements the isotropy of chemical etching in determining the shape of the etched feature. Both the adsorption of a reactive species on the surface and the desorption of a product from the surface may be enhanced by ion bombardment (Oehrlein, 1989). Thus ion bombardment which is responsible for anisotropy also contributes to rate enhancement above that obtained by exposure to reactive gases only (Coburn and Winters, 1979).

1.5.8.2 Mechanisms

Several mechanisms have been proposed to account for the rate enhancement: (1) the reacted surface sputters with a higher yield than the unreacted surface (chemically enhanced physical sputtering; Mauer et al., 1978; Dieleman, 1978; Haring et al., 1982; Dieleman et al., 1985), (2) ion bombardment damages the surface thereby increasing the reaction rate (Flamm and Donnelly, 1981; Greene et al., 1988; Oehrlein, 1993), (3) ion bombardment supplies additional energy to the reaction layer enhancing volatile compound formation and desorption (chemical sputtering; Tu et al., 1981), and (4) energetic reactive ions dissociate upon impact into atoms which react with the substrate (direct reactive ion etching; Steinbruchel et al., 1986). As pointed out by, for example, Tu et al. (1981) and Vugts et al. (1996), several mechanisms may contribute to the overall reaction. A shift in the mechanism of etching has been shown to occur by, for example, changing the composition of the feed gas (Dulak et al., 1991) or the ion energy (Mayer et al., 1981).

There are detailed reviews of mechanistic studies and models, which include spontaneous etching and the sometimes contradictory effects of ion bombardment: e.g., Winters et al. (1983), Coburn

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and Winters (1985), and Coburn (1988). The applicability of each model appears to depend on the specific etchant/substrate system. In addition, some of the results obtained by reacting clean surfaces in a vacuum (as done in some mechanistic studies) may be different from those obtained in practical etching systems.

1.5.8.3 Etching Systems

The first commercially available plasma etchers were barrel reactors in which ion bombardment was minimal and etching was purely chemical (i.e., isotropic) (Irving, 1971; Abe et al., 1973). The advantage over etching in solution was the integrity of the mask/substrate interface. In wet etching, the liquid, driven by capillary forces, often penetrated beneath the resist, lifting it and exposing regions of the substrate protected during the lithographic procedures. This does not occur in a plasma so that any undercut beyond that dictated by isotropy was a function only of the overetch time. The use of this configuration outlasted the pattern transfer application; it has been used extensively for resist ashing, i.e., oxidation in an O-radical plasma, although downstream etching may be replacing it (Boitnott, 1994).

1.5.8.4 Reactive Ion Etching (RIE) or Reactive Sputter Etching (RSE)

RIE combines the chemical activity of the reactive species with the ion bombardment of physical sputtering. Among the first RIE reactors were the capacitively coupled sputter etchers (asymmetric systems) retrofitted with reactive gases. These were low-pressure systems; the low pressure and high ion energy bombardment of the wafers (placed on the smaller electrode) favored anisotropy. Muto (1976) was one of the first to patent this process. He claimed vertical etching of masked surfaces placed on the cathode of a two-electrode planar reactor, into which chemically reactive F- or Cl-containing gases were introduced for the purpose of rapid etching of thin-film circuits or semiconductor chips. Matsuzaki and Hosakawa (1976) called it a method for sputter-etching silicon or its compounds, using a planar electrode and employing fluorohalogenhydrocarbon gases (including bromine and O_2, N_2, Ar, or air as diluents) for the manufacture of integrated circuits.

Symmetrical systems (based on the radial flow reactor) were also popular; they were labeled plasma etchers because the wafers were placed on the grounded electrode. However, since the system was symmetrical, the potential on each electrode was the same. The tendency toward isotropy was due not to the grounding of the substrate electrode but in part to the pressure regime in which they were operated: several hundred millitorr as compared with tens of millitorr in the RIE systems. In addition, the plasma potential was high due to the symmetry and plasma confinement between the closely spaced electrodes, so that the ion energy was lower than in RIE. The use of the so-called anisotropic etching gases, in which lateral attack (isotropic etching) was inhibited, extended the usefulness of these reactors (Ephrath, 1981b). Their action was due to the formation in the plasma of species that (1) inactivated the etchant species (recombinants) or (2) formed a protective film on the sidewall (passivants). These systems were eventually abandoned in favor of the low-pressure, high-bias RIE systems, in which there was a greater latitude in the choice of etchants.

The distinction between RIE (cathode coupled or diode etching) and what was known as plasma etching (anode coupled) in what may appear to be a symmetrical reactor, because the internal electrodes are of equal area, was stated clearly by Mathad and Patnaik (1979): “In the diode mode, the power is applied to the wafer-carrying electrode while the rest of the system is grounded”; the ion energies at the wafer surface are high. “In the anode mode the power is applied to the upper electrode; the wafer-carrying electrode and the reactor chamber are grounded and there is negligible ion bombardment of the wafer surface.” These concepts were also illustrated by Toyoda et al. (1980).

The capacitively coupled RIE systems are being replaced, in turn, by the lower pressure, independently biased, high-plasma-density RIE reactors which are discussed later.

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1.5.8.5 Choice of Etchants

The choice of etchants (and inert species) depends not only on the ability to form a volatilizable product in its reaction with the substrate but also on its potential for enhancing anisotropy and selectivity to mask and substrate (Coburn and Kay, 1979; Flamm and Donnelly, 1981). Mixtures of gases may be required to achieve the desired results. Inert additives are often used as diluents, but they may have other functions, such as plasma stabilization, cooling, alteration of the electron energy distribution, enhanced ion bombardment, and formation of metastable states for efficient energy transfer (Oehrlein, 1989). In metal etching, N_2 plays an active role (Ohno et al., 1989; Sato and Nakamura, 1982; Howard and Steinbruchel, 1991). H_2 (Heinecke, 1976) and O_2 (e.g., Flamm and Donnelly, 1981) are often used to interact with the etch-specific gases to modify the etch results. The nature and relative concentrations of the reactive species formed in the plasma from the source gases depend not only on the chemical composition of the gases but also on the electron energy and energy distribution in the plasma which, in turn, are a function of the system (e.g., low-density vs. high-density plasma) and the system parameters. A more detailed examination of some of these systems is made in later chapters when some of the specific substrate/etchant interactions are discussed.

Another issue, more recently addressed, is the effect of some of these etchants on the environment and the efforts made to reduce their global warming potential. This is discussed in detail in Chapter 4.

1.5.8.6 System Parameters

The physical parameters, such as power, pressure, gas flow rate/pumping speed, and reactor configuration in parallel-plate reactors (e.g., chamber size and shape, relative electrode sizes and electrode spacing, number and location of ports, etc.) affect the electrical properties of the glow discharge and thus the interaction with the source gases. Their influence on etching, individually and in concert, are important but beyond the scope of this book. Several recent reviews cover some of this material (Oehrlein, 1989; Manos and Flamm, 1989; Oerhlein and Rembetski, 1992).

Since, as pointed out by Oehrlein and Rembetski, there is no simple relationship between the process objectives and the physical variables, process optimization requires systematic investigation of the parameter space.

1.5.8.7 Profile Control

There are several aspects to profile control; one is suppression of undercut. Others are the prevention of (1) bowing (outward curvature of the sidewalls) and (2) trenching or dovetailing (overetching into the substrate at the bottom corners of a feature). Still another is deliberate shaping of the profile of via holes to form sloped sides (edge tapering) to ensure better step coverage during subsequent deposition of overlying films if vertical studs (plugs) are not used; this is discussed in Chapter 4. Advances in step coverage and hole filling (discussed in Chapter 6) reduced the need for tapering. Processes for etching space-saving vertical profiles (particularly in low-ε films) are in constant development.

The influence on the shape of the etched feature of both the shape and etch rate of the mask relative to that of substrate is covered in the next section. The extremes in profile, purely directional and purely isotropic, are illustrated in Figure 1.34.

An isotropic profile results when the dominant etchants are neutral (chemical) species and there is no inhibition of this lateral component. Lateral etching may be minimized or even eliminated by what has been called sidewall passivation, in which a chemically unetchable film is formed on all surfaces (Oehrlein and Rembetski, 1992). Only the horizontal surfaces are exposed to energetic ion

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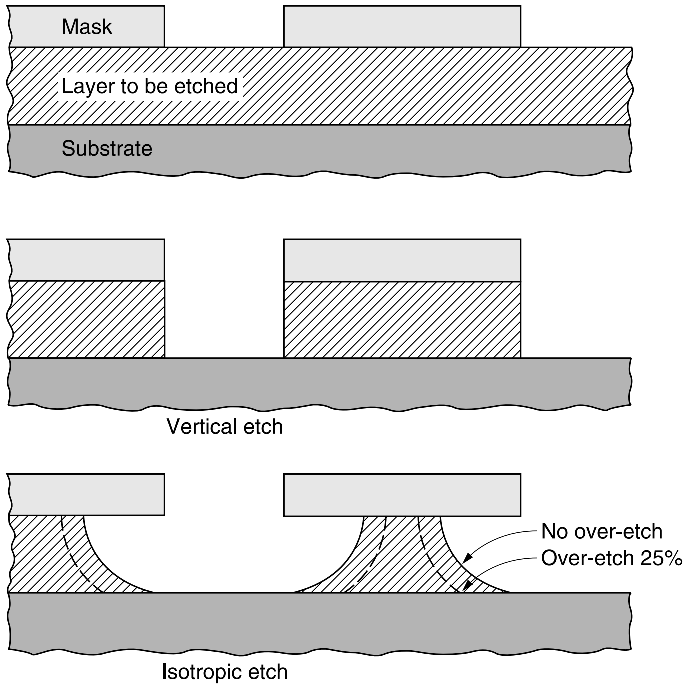

Figure 1.34 Schematic showing the contrast between vertical and isotropic etch profiles.

bombardment which removes the film, exposing fresh surfaces to the etchant. There is essentially no ion bombardment on the vertical walls, so the film remains there. Therefore, vertical, but not horizontal, etching proceeds. Passivating films have been observed in most material/etchant systems currently used. The inhibiting film may be formed from precursors created in the discharge by fragmentation of the source gas (Schaible and Schwartz, 1979), by redeposition from an eroded mask, or by both (Kawamoto et al., 1994). Another source of protection is the formation of a film, in the absence of ion bombardment, by a side reaction between an additive and a reaction product. Hirobe et al. (1987) found that a sidewall film was formed by materials sputtered from the cathode plate. A sidewall film, flaking off the edges, is seen clearly in Figure 1.35, which shows a scanning electron microscopy (SEM) image of an Al film etched in CCl_4/Ar.

Redeposition on the sidewalls of a marginally volatile etch product can also provide some protection. The competing processes of etching and deposition not only provide protection but also result in a slight inward tapering of the edges, i.e., the sidewall film decreases in thickness with depth.

The shape of the etched feature can also be influenced by off-axis ions (Lii and Jorne, 1990; Nguyen et al., 1991) and by ions scattered from the edges of a mask (Ohki et al., 1987). Arnold and Sawin (1991) proposed that localized surface charging could cause surface potentials capable of skewing the directionality of the incoming ions, resulting in ion fluxes to the walls of an etched feature which would contribute to bowing and trenching. Murakawa et al. (1992) invoked this same phenomenon to account for profile distortion, i.e., tilted edges.

Pulse-time modulation of the plasma in several high-density reactors has been used for profile control of Si. For example, Boswell and Henry (1985) and Boswell and Porteous (1987) found that pulsing the plasma in a substrate-biased helicon plasma reactor changed the profiles of Si etched in SF_6; the longer the duration of the pulse (e.g., 1000 msec at 20% duty cycle) the straighter the walls (and the lower the ER).

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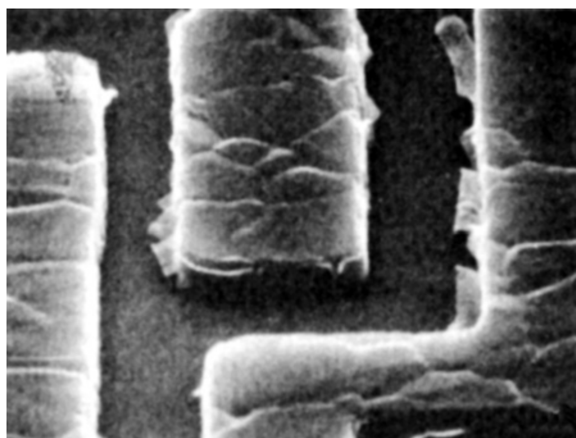

Figure 1.35 SEM image of a sidewall film formed during RIE of AlCu in CCl_4/Ar. (From Schwartz, G.C. and P.M. Schaible, *J. Electrochem. Soc.*, 130, 1777, 1983. With permission of the Electrochemical Society, Inc.)

Modulation of chlorinated plasmas has been used in high-density reactors to achieve vertical and notch-free profiles as well as highly selective and charge-free etching (e.g., Samukawa and Terada, 1994; Fujiwara et al., 1996; Samukawa and Mieno, 1996). The improvements due to pulsing were attributed to the change of the flow of ions through the sheath region to the substrate surface (Mieno and Samukawa, 1995).

Tungsten was etched in pulsed SF_6 helicon plasmas (Petri et al., 1994). Two etching regimes were shown to exist. For short discharge-off periods, etching was limited by F adsorption on the surface (neutral-limited); for long discharge-off periods, etching was limited by the desorption rate (ion-limited).

A model was developed to interpret the results of a pulsed high-density plasma on metal etch. It dealt with pulsing the source power to control the ion and radical densities and pulsing the bias power to control the ion energy. It showed that higher selectivity to resist and minimized AR-dependent etching can be achieved at high etch rates. It also showed the same directionality and charge-up effects (Xie and Kava, 1996).

A time-modulated ECR plasma was used to control polymerization in etching SiO_2 to achieve high selectivity (Samukawa, 1993). In contact/via etching a time- or power-modulated high-density plasma can be used to increase the selectivity of SiO_2 to Si by controlling the generation ratio between polymer precursor and etching species (Xie and Kava, 1996).

Other reports are available on pulsed plasmas: e.g., Economou and Park (1990), Verdeyen et al. (1990), Ashida et al. (1995), Holland et al. (1996), Ahn et al. (1996), and Sugai et al. (1996).

A different approach was used by Tsujimoto et al. (1986) who proposed a chopping method to prevent lateral etching in ECR etching. The sample was sequentially and independently exposed to a film forming gas and an etching gas, so that the side wall is covered as the bottom of the feature is etched. Shibata and Oda (1986) used a multistep process for etching Si by alternating RIE in a chlorinated plasma with surface oxidation. Another hole taper-etching procedure involved using an oxygen ion plasma in a biased ECR reactor; it was based on the incident angle dependence of the etch rate and the etch selectivity of SiO_2 with respect to the metal in an O_2 plasma (Hashimoto et al., 1990).

Profile evolution is not discussed in detail in this book. It has been the subject of many models and simulations and just a few references, in addition to those cited above, are given as examples: Smith et al. (1987), Arikado et al. (1988), Glowacki and Tkaczyk (1988), Cottler et al. (1988), Economou and Alkire (1988), Gross and Horwitz (1989), Jackson and Dalton (1989), Giffen et al. (1989), Shaqfeh and Jurgensen (1989), Pelka et al. (1989), Lii and Jorne (1990), Cottler and

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Elta (1990), Fujinaga et al. (1990), Fichelscher et al. (1990), McVittie et al. (1992), Singh et al. (1992b), Shan et al. (1994), and Hamaguchi and Dalvie (1994). Some models consider the two components of RIE, the chemical and the ion assisted, their interactions, the competing roles of etching and deposition, and changes in mask shape. Others concentrate on the effects of ion scattering in the sheath and reflection off the sidewalls of the etched feature or due to local surface charging which affects not only ion deflection but ion flux and energy distribution.

1.5.8.8 Masking

In wet chemical etching, the shape and thickness of the mask is not important. The principal requirement is good adhesion, particularly at the edges of the mask, to prevent seepage of the etchant beneath the mask and increase the lateral extent of the isotropic profile. In RIE, however, masks usually etch at a significant rate due both to ion bombardment and chemical reaction. Thus the choice of the mask material (its etch rate) and its shape are very important; adhesion is a concern only if wet chemical steps precede RIE. The interaction between mask shape and the etch rate ratio of mask to substrate is shown in Figure 1.36a for vertical and Figure 1.36b for tapered masks, assuming only vertical etching. It is clear that, if the erosion of the tapered mask is prevented, i.e., if the bottom edge does not move laterally, the result will be a vertical profile. Additional changes in the mask profile, due to lateral chemical etching and faceting of the edges by ion bombardment, will be reflected in further (and possibly more complex) changes in the shape and dimensions of the etched feature. Deposition of a film on the surfaces of the mask, when using polymerizing etchants, may protect them from erosion.

Another requirement is thermal stability since sample heating may occur due to ion bombardment and exothermic etching reactions. Heating can cause flow or reticulation of a resist mask, distorting it so that changes in its shape and dimensions result. Resist stabilization procedures

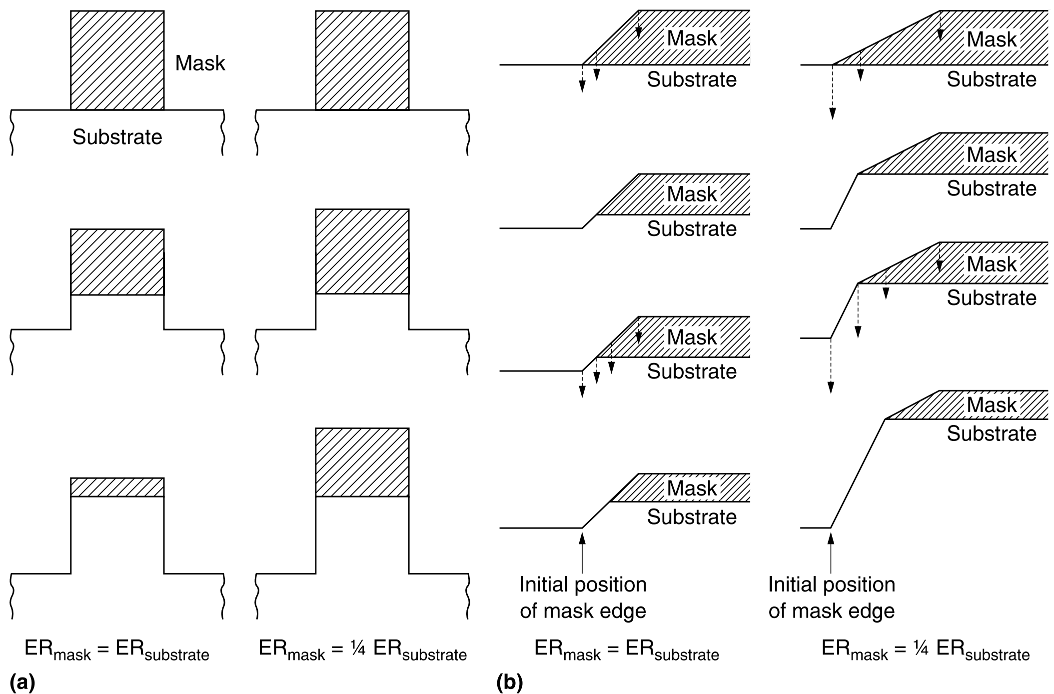

Figure 1.36 Effect of mask shape and etch rate ratio of mask to substrate on the profile etched into the substrate assuming only vertical etching: (a) vertical mask; (b) tapered mask.

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have been developed to minimize these effects (Iida et al., 1977; Ma, 1980; Moran and Taylor, 1981; Hiraoka and Pacansky, 1982).

Hard (unflowable) masks, such as SiO_2, Al_2O_3, MgO, have the additional advantage of negligible etch rates in the processes for which they are used but require additional processing. Unetchable masks have been used to study the basic interaction between plasma and substrate by eliminating any contribution of mask erosion to the shape of the feature.

The limitations of single-layer resist masks and the advantages and drawbacks of multilevel masks for RIE (described in Chapter 6) have been discussed by Tracy and Mattox (1982), Kinsbron et al. (1982), and Bushnell et al. (1986).

1.5.8.9 Loading Effect

A loading effect occurs in chemically reactive plasmas; it is observed as a change in etch rate in response to a change in the supply (consumption) of the reactant during an etch process (not as a result of changing the inlet supply). Loading effects are categorized as global or macroscopic loading or local or microscopic loading, but the assignment to a given classification is often made differently by different authors.

It was first observed as a reduction in the average etch rate as the total area of etchable material exposed to the plasma was increased; it is due to the average consumption of etchant species during etching (Schwartz et al., 1976; Mogab, 1977; Schaible et al., 1978). This is global loading which affects production since the average etch rate decreases as the number of wafers etched simultaneously is increased. Processing time will, therefore, depend on the number of wafers in the batch. If only a small fraction of the active species is consumed, the effect can be minimized; however, this would require a very large flow rate of the source gas and very efficient pumping of enormous volumes of gas. Another approach is to have the reactor fully loaded at all times, e.g., using an etch pallet made of the same material as that being etched or another material whose etch rate is the same. The use of single-wafer etchers eliminates this problem and is a major advantage of these newer systems. However, the material of which a single wafer reactor is constructed can influence the etch rate. Watts and Varhue (1992) report a loading effect of a quartz microwave window or reactor liner on the etch rate of Si in SF_6.

The local loading effect is a universal problem and difficult to eliminate. One cause, which is perhaps subject to some degree of control, is due to nonuniformities in etch rates and film thickness. However, independent of those factors, the area of the film being etched changes nonuniformly as the endpoint is approached. As the underlying (nonreactive) substrate is exposed, nonuniformly, the local consumption of etchant decreases, leading to increased availability of etchant for the neighboring film, increasing its etch rate. The result may be severe overetching, both into the substrate and, in some cases, undercut of a masked feature due to enhanced lateral etching.

Another aspect, unrelated to nonuniformities in thickness and average rate, is the bulls-eye etch pattern sometimes seen in etching Al and its alloys. The outermost regions of the wafer are adjacent to areas in which reactant is not consumed; thus the local reactive species concentration at the edges is high. As a result, the edges etch faster than do the central regions, all of which are being etched and depleting the reactant supply.

A very important expression of local loading is the pattern factor effect, i.e., local variations in etch rates due to differences in the size, shape, and relative location of masked features, i.e., to differences in local consumption of etchant. Features of low pattern density etch faster than those in high-density areas (Jones et al., 1990). The result may be undesirable differences in the size and shapes of etched features. Differences in chip layout may force changes in the details of the etch process. In addition, this effect may account for incomplete local etching (residues). In RIE of AlCu films in CCl_4/Ar, the narrower spaces cleared more rapidly than the wide ones, whereas in etching Cu in the same system/gases, they cleared more slowly (Schwartz and Schaible, 1983). In etching

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an Al alloy in Cl_2 etching in a biased ECR reactor, the microloading effect was opposite to that seen in the CCl_4 RIE system, i.e., narrow spaces etched more slowly (Aoki et al., 1992). These differences have not been explained.

Giapis et al. (1990) discussed the issues of loading as uniformity control. They stated that uniformity is improved by reducing the gas pressure. Improvement of the macroscopic uniformity is attributed to the fact that the plasma is more homogeneous at low pressure and that the transport of reactants to the surface becomes diffusion limited and thus independent of flow.

1.5.8.10 Feature Size Dependence of Etch Rates

Often large trenches and via holes etch more rapidly than smaller ones when features of different sizes are etched simultaneously. The etch rate differential depends on aspect ratio (AR = depth/width) not on the absolute size of the opening, although Schaepkens et al. (2000) reported a small effect of the diameter of the feature. The etch rate decreases linearly with increasing AR for AR > 2 (Chin et al., 1985). The phenomenon has been given several names: RIE lag (Lee and Zhou, 1990, 1991), aperture effect (Abechev et al., 1991), and aspect ratio-dependent etching (ARDE) (Gottscho et al., 1992). Although Fujiwara et al. (1989) and Sato et al. (1991) called it microloading, Gottscho et al. (1992) called this a misnomer, since ARDE results from microscopic transport within a single feature while microloading and macroloading arise from identical causes. The AR effect can occur without microloading and vice versa.

Because the AR increases as etching proceeds, the etch rate decreases with time. Gottscho et al. (1992) point out that, to be sure the phenomenon is AR related, it is necessary to determine the etch rate as a function of time for several feature widths to distinguish it from other time-dependent etch rates which can arise due to polymer buildup or surface poisoning.

Reverse RIE lag, in which smaller features etch at a greater rate than larger ones, has also been reported (Dohmae et al., 1992; McVittie and Dohmae, 1992; Doemling et al., 1996). Under some limited conditions, AR-independent etching (ARIE) is observed (Bailey and Gottscho, 1995; Hwang and Giapis, 1997).

Since RIE lag is most important in etching via holes in insulators, the subject is discussed in detail in Chapter 4. It also occurs in etching metals, covered in Chapter 5.

1.5.8.11 Angular Dependence of the RIE Yield

When the chemical component of the RIE process is dominant, the angular dependence of the yield is no longer that characteristic of sputtering (see Section 1.5.5) but is highest at normal incidence and falls off monotonically as the angle of incidence is increased, following a cosine-like decrease. At normal incidence the energy is deposited close to the surface where the chemical reaction occurs and from which the product is desorbed. If the velocity of an ion impinging normal to the horizontal surface is v, then an ion impinging at an angle θ has a velocity component $v\cos\theta$ in the direction normal to that surface and a maximum energy of $(½)v^2\cos^2\theta$. According to Steinbruchel (1989) the yield for chemical as well as physical sputtering is proportional to the square root of the incident energy, and thus the cosine dependence of the yield (Cho et al., 2000).

At high angles of incidence, both for physically and chemically dominated processes, the yield decreases rapidly, i.e., etching of vertical and near-vertical features is negligible, an important factor in designing the shape of resist masks used in RIE (Hamblen and Cha-Lin, 1988).

The shape of the yield vs. angle curve depends on the balance of the physical and chemical components which are functions of the etchant, substrate, pressure, and ion energy. At high ion energies, sputtering often becomes more important. Polymer film formation from precursors in the plasma and simultaneous etching by ion bombardment can also affect the results. The angular dependence of the etch rates of several substrates in a variety of etchants has been investigated using (1) RIBE (with a

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tilted substrate holder for a variety of angles) (Mayer et al., 1981; Barkland and Blom, 1992, 1993), (2) a RIE and an ICP system using angled surfaces formed by highly anisotropic wet etching of single-crystal silicon (Hedlund et al., 1996, 1997), and (3) an ICP system, with several tilted substrates mounted in a Faraday cage with small holes in the cover (Cho et al., 2000).

An example of a chemically dominated process showing no sputtering characteristic is the angular dependence of the etch rate of Si in a Cl_2 discharge studied by Mayer et al. (1981) and Hedlund et al. (1997). In a RIE system, the data points, at one bias, lay on a cosine curve indicating that the etch rate was proportional to the current density at the surface and the yield relatively independent of angle. By varying the substrate bias, the behavior went from a little under cosine values at low bias to somewhat over cosine values at high bias It was speculated that at high ion current densities and low ion energies, the Cl was preferentially sputtered and/or desorbed causing the yield to decrease; at high energies more Cl may be implanted and react, leaving the surface as $SiCl_x$, resulting in cosine or over cosine behavior. In an ICP reactor, the angular dependence of the etch rate was significantly under/over cosine as the substrate bias was varied (Hedlund et al., 1997).

The angular dependence of the etch rates of several dielectric films in fluorinated plasmas is covered in Chapter 4.

1.5.8.12 Temperature Effects

Initially, the need to keep the wafer temperature low during RIE was to prevent thermal damage to organic masks. Substrate heating was employed to assist in volatilization and prevention of redeposition of etch products during RIE of Cu.

More recently, very low-temperature (as low as about –150°C) RIE has been introduced in both capacitively coupled and ECR reactors, to improve selectivity and eliminate undercut (Tachi et al., 1988, 1991; Bestwick et al., 1990) and to reduce damage (Whang et al., 1992), microloading (Aoki et al., 1992; Sato et al., 1992), and post-RIE corrosion of Al (Aoki et al., 1992), while maintaining high etch rates. The low-temperature limit is determined by condensation of the reactive gas. At these low temperatures, the chemical component of the etch is reduced, thus suppressing lateral etching, without sidewall passivation (Whang et al., 1992), whereas the ion-assisted reaction is essentially independent of temperature. Giapis et al. (1990) demonstrated that both macroscopic and microscopic uniformity can be improved by etching at reduced temperature because etching occurs in an ion-activated, surface reaction-limited regime. Thus etching is essentially independent of plasma geometry, gas flow, and pressure, as well as reactor and mask materials.

1.6 ELECTROCHEMICAL DEPOSITION

1.6.1 Electroless Plating

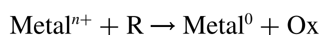
Electroless plating is an autocatalytic process; on a catalytic surface, metal ions are reduced to the metallic state:

$$\text{Metal}^{n+} + n \text{ electrons} \rightarrow \text{metal}^0$$

in the partial (cathodic) reaction in a solution of a reducing agent. The source of electrons for the reduction reaction is the partial (anodic) reaction in which the reducing agent is converted, on the catalyst, to the oxidation product:

$$\text{Reducing agent (R)} \rightarrow \text{oxidized R (Ox)} + \text{electrons}$$

with an overall reaction:



$$\text{Metal}^{n+} + \text{R} \rightarrow \text{Metal}^0 + \text{Ox}$$

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The electrons are transferred from the anodic to the cathodic sites on the conducting catalyst. Once the reaction is initiated and a film deposited, the reaction continues on the film surface. The kinetics and mechanism of electroless metal deposition have been discussed in some detail by Paunovic (1988), and Shacham-Diamand et al. (1995a) have reviewed electroless Cu plating as a metallization method for integrated circuit application.

Since a metal deposits initially only on a catalytic surface, it can be grown selectively within a cavity by activating only the bottom surface. However, all surfaces may be activated for blanket deposition. Ion implantation (Kiang et al., 1992), L/O processing (Harada et al., 1986), evaporation (Dubin et al., 1993), sputtering (Shacham-Diamand et al., 1995b), and focused laser patterning (Cole et al., 1988) are among the methods used to form an active substrate for electroless deposition. Whether the deposition is selective or blanket, the film grows from the activated surface. Thus when only the bottom of a tapered feature is activated, it is not possible to fill it properly. No voids or seams are formed within the deposit. Some examples of electroless deposition are Ni on Si (Sullivan and Eigler, 1987), Ni on Al (Harada et al., 1986; Ting and Paunovic, 1989), Pd on silicides (Sullivan and Eigler, 1987), Ni–Cu(P) on AlCuSi (Dubin, 1992), Ni on TiW (Dubin et al., 1993), and Cu on TiN-coated Cu (Dubin et al., 1995). The deposit called Ni is, in fact, a Ni alloy, either NiP (Feldstein, 1970) or NiB (Schmeckenbecker, 1971).

Si is an active surface for Ni, silicides are active for Pd, and AlCuSi is active for Ni–Cu(P), but activation is needed for the deposition of Ni on silicides and on Al and for Cu on TiN-coated Cu. One procedure used for plating Ni on Al is sensitization in an acidic solution of $SnCl_2$, followed by activation in an acidic solution of $PdCl_2$ (Feldstein, 1973). Another pretreatment before activation in $PdCl_2$ is immersion in a Cu displacement solution to form Cu particles on an Al surface (Schwartz, 1974). Immersion in Cu solution has also been used to activate a TiN-coated Cu surface which then needs no further treatment before plating (Dubin, et al., 1995).

Although deposition of the seed layer through a L/O has been used, is not satisfactory, since the sidewalls become activated as well as the bottom, resulting in overgrowth of the metal. This is illustrated in SEM images of via holes filled with electroless Ni. In Figure 1.37a the activation was accomplished by immersion in a $PdCl_2$ solution, and in Figure 1.37b by deposition of Pd through a L/O mask (Harada et al., 1986). In the latter case, the rim surrounding the deposit is pronounced. The conductivity of Ni alloys is quite low so that their usefulness is limited. Cu is a better choice

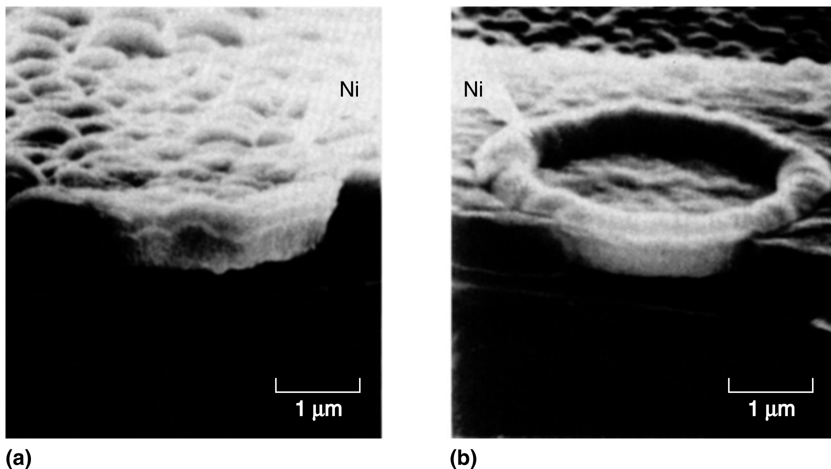

Figure 1.37 SEM images of electroless Ni filling a via hole: (a) seeding with a $PdCl_2$ solution; (b) seeding using a lift-off process. (From Harada, Y., K. Fushimi, S. Madokoro, H. Sawai, and S. Ushio, *J. Electrochem. Soc.*, 133, 2428, 1986. With permission of the Electrochemical Society, Inc.)

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because of its lower resistivity, but the pH of electroless Cu plating solutions is high enough to attack the underlying Al. With the advent of (clad) Cu interconnects, electroless Cu deposition has become a feasible process. Electroless Cu plating is discussed in greater detail in Chapter 5.

Electroless deposition is attractive chiefly because of its low cost and simplicity of equipment and operation. The resistivity of Cu films is close to that of the bulk value and there are no unfilled vias and submicrometer wires are robust and continuous. There are, however, potential problems: e.g., contamination from the solution and reaction byproducts, evolution of H_2, and inadequate or incomplete sensitization, although some success has been reported by Dubin et al. (1995).

1.6.2 Electrolytic Plating (Electroplating)

A brief introduction to the principles of electroplating can be found in Chapter 2. A more complete discussion of electroplating Cu and the properties of plated Cu films is contained in Chapter 5. Chapter 6 covers forming the conducting elements using plated Cu when building a device structure.

The important advantage of electroplating is avoidance of contamination of the film by H_2, since the potential required for deposition of a noble metal (e.g., Cu) from a solution of its ions is less than that required for cathodic liberation of H_2. A disadvantage is that a conducting layer (called the seed layer) must be deposited along the entire surface to provide a path for the current.

Electroplating requires the use of an external anode; the wafer is the cathode. The electrolyte, in which the electrodes are immersed, contains the appropriate metal ion as well as any other constituents needed, chiefly to improve the hole-filling capability of the deposit. The throwing power of the bath, i.e., the ability to cover recesses, is one of its important properties. In the case of the small dimensions existing on a chip, the microthrowing power is important (Lowenheim, 1978). If the deposit is thicker over the peaks, the bath has poor microthrowing properties. If it is thicker in the recesses the bath is said to be leveling, which is desirable in this application. Leveling is achieved using organic additives.

Usually, wafers are processed individually. An example of a single-wafer electroplating cell used for copper deposition, reproduced from the patent of Mayer et al. (2003), is shown in Figure 1.38a. The cathode is at the top of the chamber and the wafer is clamped face down a small distance into the electrolyte. A chemical transport barrier (porous membrane) surrounds the anode to maintain a separate chemical and/or physical environment in the anode chamber, i.e., largely to prevent nonionic organic species from entering the anode chamber. There is provision for circulation and treatment of the electrolyte. The system is automated (Figure 1.38b), with a robot arm to select a wafer from a cassette and transfer it to one of the various electrofill modules and then to post-electrofill modules in which edge bevel removal, backside etching, and acid cleaning can be performed, and finally to return it to the cassette.

The means of protecting the backside of the wafer and applying the current uniformly are described Chapter 5. Pulsed-voltage plating has been used to achieve good throwing power (Contolini et al., 1994). A virtual anode, described in a patent by Poris (1993), was used to improve the current distribution at the cathode and to allow latitude in improving stress, film morphology, and step coverage, without degrading film uniformity.

1.7 SPIN COATING

The art and science of spin coating for semiconductor device fabrication was developed principally in the lithography sector for coating photoresists on wafers. Its use expanded to coating interlevel dielectrics (Chapter 4): spin-on-glasses (SOGs), polyimides, and some of the new low-ε films, the so-called SODs. There was one instance of using spin coating to deposit Cu films (Murakami et al., 1999).

Spin coating has the advantage of using simpler (thus cheaper) equipment than vacuum processes. Also, a spinner can be used for a variety of spin-on materials, without any modification.

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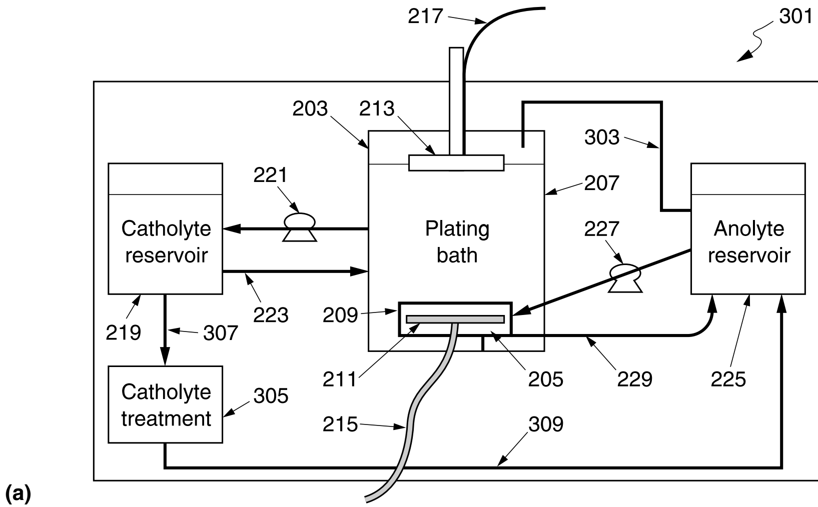

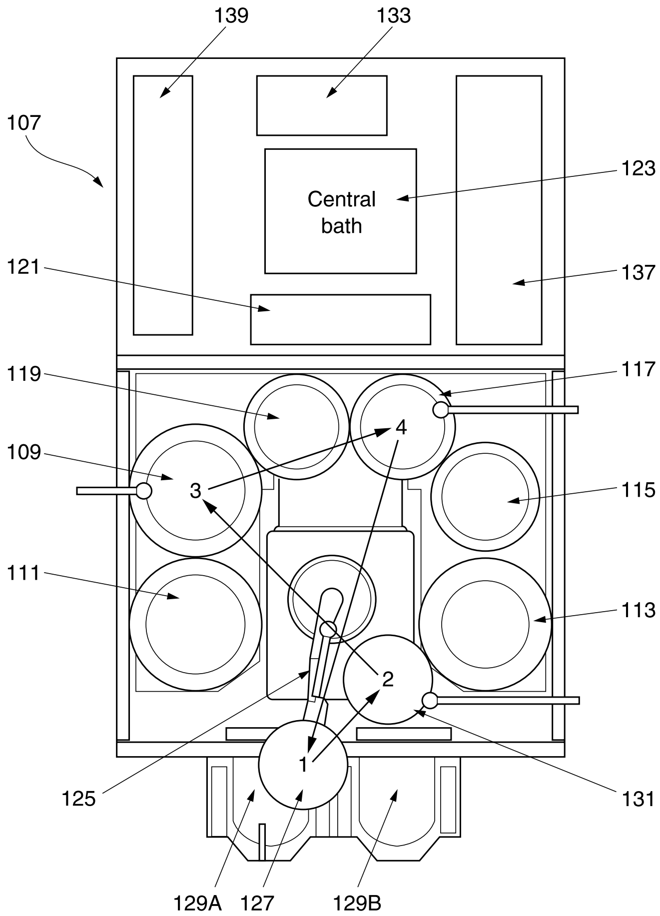

Figure 1.38 Electrochemical plating: (a) plating cell showing circulation of plating bath; (b) the transfer system. (From Mayer, S.T., E.E. Patton, R.L. Jackson, and J.D. Teid, U.S. Patent 6,527,920 B1, 2003.)

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Spin tracks have automated the process, increasing the throughput. For a given solution viscosity, the thickness of the film is controlled by the spin speed. Most spin-on films have good gap-filling and planarization capabilities.

The curing (heating) process following spinning of dielectric films is a critical step. During the cure, solvent evaporation, chemical reactions, or internal bond rearrangements take place. The temperature is raised incrementally; the temperature/time at each step and the final temperature (usually 400 to 450°C) affect the properties of the film. Curing has been carried out in batch furnaces or on individual hot plates; an in-line, single-wafer, hot-plate system requiring very short exposure times at the various temperatures was described by Batchelder et al. (1999). Rapid heating/cooling is also obtained by rapid thermal processing (RTP), also known as rapid isothermal processing (RIP). RIP can be improved using dual spectral sources (a tungsten–halogen lamp (UV, visible, and IR photons) below the wafer and a deuterium lamp (VUV photons) at the top) (Sharangpani et al., 1997). These techniques reduce the thermal budget and processing time. In addition, Bremmer et al. (1999) reported that RTP resulted in an HSQ film of lower ε than did conventional furnace cure. N_2 with a *very* low O_2 content is the curing ambient. Some problems associated with the process are shelf-life of the solutions, edge-bead buildup of the spun-on films, and an inadvertent excess of O_2 in the curing ambient.

Spin-on Cu metal (SOM) is somewhat different from the other spin-on liquids in that it is a dispersion of ultrafine (8 nm) Cu particles in an organic solvent. The concentration of Cu is ~10 to 20%, depending on the required thickness (which may require several coats). The cure is needed only to remove the solvent; the ambient is N_2 to prevent oxidation. The film thus formed has a resistivity of $< 2\ \mu\Omega$ cm (Murakami et al., 1999).

1.8 CONCLUSION

In the past few decades, the processes for the deposition and patterning of the metals and insulators used for multilevel interconnections (as have the choices of the metals and insulators themselves, as covered in Chapter 4 and Chapter 5) have undergone many changes.

For metal deposition, evaporation gave way to sputtering in simple RF capacitively coupled reactors, to magnetically enhanced sputtering systems, to extensive modifications (collimation, etc.), to CVD, to the use of high-density plasmas (IMP), and now, for copper metallization, to electrodeposition. Patterning has moved from wet to reactive plasma-assisted (dry) etching, and most recently to additive (damascene) processes.

Insulators were first deposited by CVD, sputtering, a limited use of spin coating, but most successfully by PECVD in the variety of systems described in this chapter. Spin coating is now reemerging as a contender. Etching is still required, and has changed from wet to dry processes.

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CHAPTER 2

Characterization

Geraldine Cogin Schwartz

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2.1 INTRODUCTION

In this chapter we describe and explain many of the most widely used techniques for characterizing the optical, mechanical, electrical, and chemical properties of thin films, examining structures fabricated from the films, and measuring some reactor properties. Finally, some chemical analytical techniques are discussed.

Table 2.1a, Table 2.1b, and Table 2.1c summarize many of the characterization techniques and their applications.

Table 2.1a Characterization Techniques

Property	Technique	Comments
Thickness	Stylus	Any film; need sharp step
	Interferometry	Dielectric films
	Ellipsometry	Dielectric films
	XRFS	Any film; do not need step; layer thickness in composite film
	RBS	As in XRFS
	Resistance change	Measure metallic film growth
	SEM	Cross-section
Composition	Wet chemical analysis	Elements; some groups[a]
	AES	Elements, some bonding[b]
	w/sputter	Depth profile[c]
	XPS	Chemical bonding[d]
	w/sputter	Depth profile[c]
	RBS	Elements; compound formation[e]
	XRFS	Elements
	Microprobe	Elements
	IR	Dielectrics; bonds
	SIMS	Elements[f]
	XRD	Phases, crystal structure

[a] Destructive. After sample dissolution, instrumental analysis, e.g., chromatography, colorimetry, spectrometry, etc.
[b] Beam damage (desorption, e.g., F); charging of dielectrics; small beam size, quantitative, detection limit can be excellent; sensitive to all elements but H, He; sample cannot decompose in high vacuum.
[c] Destructive; interface distortion
[d] Nondestructive, large area for analysis, sensitive to all elements but H, good for organic films, some depth resolution with angle-resolved XPS, can be quantitative; sample compatible with high vacuum.
[e] No need for standards; depth profile without sputtering; better for high-Z elements; large area for analysis.
[f] Destructive; very sensitive, detects all elements, isotopes, small beam, matrix effects, interface distortion.

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Table 2.1b Characterization Techniques

Property	Technique	Comments
Resistivity	Four-point probe	Sheet, via resistance
Breakdown field	MOS structure: I-V	Measure distribution
Dielectric constant	MOS structure: C-V	High-frequency Si surface in full accumulation
Dopants/impurities content	IR	P, B, F, H, H_2O in dielectrics. Limitations as in Table 2.2a
	AES	
	SIMS	
	XRFS	
	Microprobe	
	Wet chemical	
Stress	Bending beam	
	Wafer curvature	Automated laser probes; XRD
Adhesion	Scotch tape, peel, scratch, blister	
Thermal	TGA, DTA	Organic films
Stability	Anneal = IR	Inorganic dielectric
	Moisture evolution analyzer	
Step coverage	SEM	Cross-section best; on-line instruments
Surface topography	SEM	Tilted sample
	Stylus	
	Optical microscope	
Interface structure	TEM	Cross-section

Table 2.1c Characterization Techniques

Property	Technique	Comments
Poisson's ratio (ν)	Bending beam	Temperature dependence of stress;
	BLS	blanket films, and high AR lines
Young's modulus	BLS	
	EP	
	Nanoindenter	Assume value of ν
	Bulge test	Assume value of ν
	SAW	Assume value of ν[a]
Biaxial modulus	BLS	
	Stress vs. temperature	
Hardness	Nanoindenter	
Porosity	PALS	Closed and open pores[b]
	EP	Closed and open pores[c]
	SXR	Electron density → mass density[d]
	SANS	Pore wall density with SXR
		Closed and open pores[e]
Pore size distribution	EP	
	PALS	
TCE	Bending beam	Temperature dependence of stress
		Two substrates

[a] Need values of thickness, density.
[b] Capping layer to close pores.
[c] Open (interconnected pores).
[d] Determine electron density; elemental composition (RBS) → film density.
[e] Measure before and after immersion in fluid.

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2.2 OPTICAL CHARACTERIZATION OF DIELECTRIC FILMS

2.2.1 Introduction

The measurement of the refractive index n and the thickness d of thin dielectric films is used extensively in device processing. The value of n is an indication of the composition and stoichiometry of a film, but must be used in conjunction with other analytical techniques since, for example, changes in density alter its value without a change in composition. The relationship between refractive index and density is given by the Gladstone–Dale equation:

$$\delta = K_1(n - 1)$$

or the Lorentz–Lorenz formula:

$$\delta = K_2(n^2 - 1)/(n^2 + 2)$$

where δ = density and K_1 and K_2 are constants. According to Pliskin (1977) the first is more applicable to SiO_2, since it is based on the assumption that the material is basically the same except for porosity. For SiO_2, assuming the pores are filled with air:

$$\delta = -4.784 + 4.785n$$

Used alone, n is a process monitor only. Thickness measurements are necessary for process calibration and control in etching and deposition. There are many techniques available; some of those for which commercially available equipment is available are described below. A more complete discussion of others can be found in Pliskin and Zanin (1970).

2.2.2 Ellipsometry

This technique is used to determine the refractive index and thickness of dielectric films and can also be used to determine the optical constants of a substrate. The method is based on measuring the change in the state of polarization of monochromatic light reflected from a substrate. The state of polarization is determined by the relative amplitude of the parallel (ρ_p) and perpendicular (ρ_s) components of radiation and the phase difference between them, $\Delta_p - \Delta_s$. Upon reflection ρ_p/ρ_s (= tan Ψ) and $\Delta_p - \Delta_s$ change. The changes depend on the optical constants n_2, k_2 (remember that $n = n - ik$ where k = absorption coefficient) of the substrate and the angle of incidence θ, the optical constants of the film n_1, k_1 and the film thickness d. The basic theory was developed by Drude and the relationships are given by Pliskin and Zanin (1970).

The light is linearly polarized by the polarizer and elliptically polarized by the compensator. After reflection, a second polarizer acts as the analyzer. Measurements are made by rotating the polarizer and analyzer until the reflected beam from the sample is extinguished. The values of the polarizer and analyzer readings are then used to determine tan Ψ and Δ and from them n_2 and d can be determined. In the early days, the values of n and d were determined by the use of graphs or tables or, eventually, a personal computer. Many of the newer commercially available ellipsometers are equipped with computers having the appropriate software for making the calculation. However, the absolute thickness is not measured, since the same values of tan Ψ and Δ recur regularly; this has been called thickness order periodicity and depends on the value of n_2. Thus a knowledge of the approximate film thickness is necessary for determining the order and, thus, the absolute thickness. There are, however, thicknesses (i.e., values of tan Ψ and Δ) for which accurate values of n_2 are not obtainable (see Pliskin and Zanin, 1970).

A schematic of a simple ellipsometer is shown in Figure 2.1a. Figure 2.1b shows the variation of tan Ψ and Δ as a function of n and d of transparent films on Si.

There are many ellipsometers available commercially. Automatic ellipsometers reduce the time required for measurements significantly, although the earliest of them made no improvements in the

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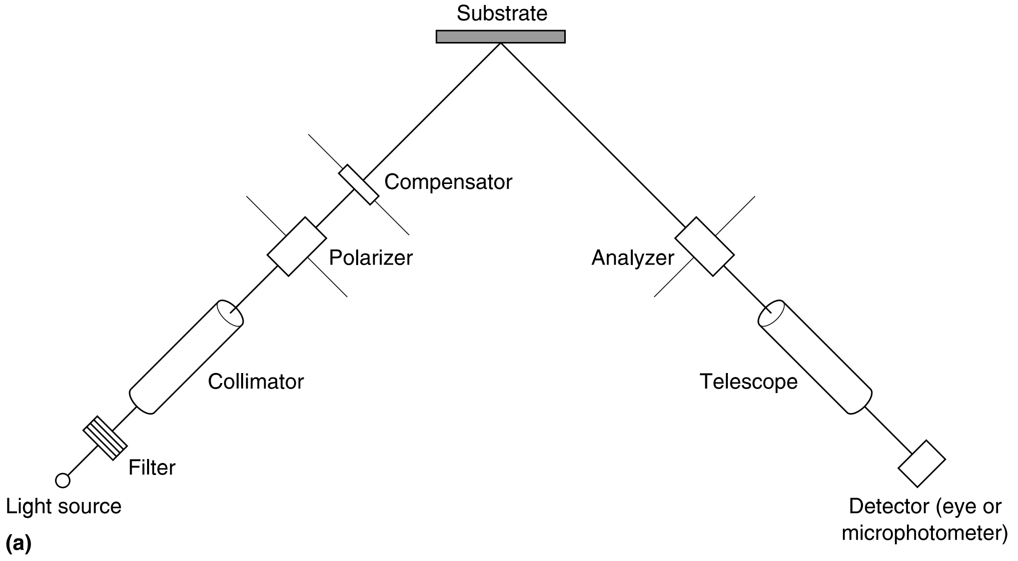

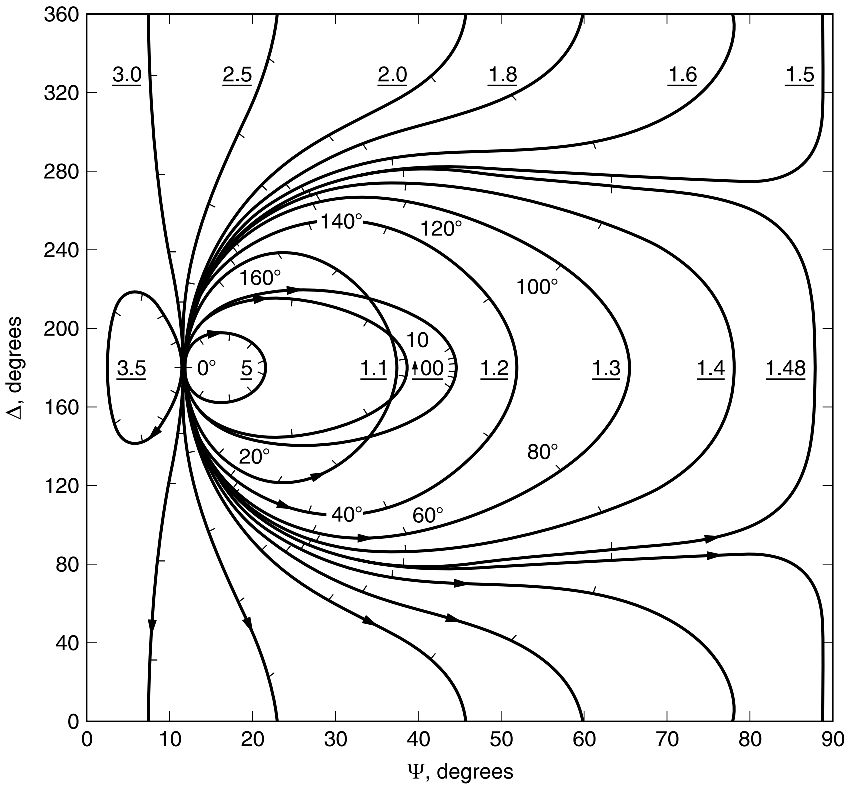

Figure 2.1 (a) Schematic of an ellipsometer. (b) Variation of Ψ and Δ as a function of refractive index and thickness.

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measurements themselves. More recently several improvements on the basic system are being offered, together with automation. The automation includes not only automated rapid data acquisition and calculation but also automatic wafer handling and positioning, as well as the capability of mapping film thickness, as 2D contour maps or 3D representations.

Variable angle (of incidence) ellipsometers allow more accurate measurements of both single and two-layer films as well as absolute thickness determination. Some ellipsometers also have the capability of using both linear and circularly polarized light. Spectroscopic ellipsometers use several wavelengths. They are said to measure very thin films more accurately than single-wavelength or multiple-angle ellipsometers. Absolute thickness can be determined and the thickness order periodicity is eliminated. Multiple film stacks can be measured. In addition, the dispersion of the refractive index can be determined. Rudolph, Gaertner, and Tencor are suppliers of ellipsometers.

2.2.3 Interferometry

2.2.3.1 Principles of Optical Interference

The schematic diagram illustrating two-beam interference is shown in Figure 2.2. A light beam I_0 of wavelength λ is shown impinging, at an angle θ_1, on the surface of a transparent film of refractive index n_λ, at wavelength λ, and thickness d. Part of the beam is reflected at the interface between medium 1 (usually air, $n = 1$) and the film; this is beam I_1; another part of the incident beam is refracted in the film at an angle θ_2 and then reflected at the interface between the film and the absorbing substrate ($n = n_3 - ik_3$); this is beam I_2. The path length between the two beams is $2n_\lambda d\cos\theta_2$. If this difference is $N\lambda$, where N is an integer, the beams will be in phase and there will be constructive interference (i.e., maximum brightness); if N is a half integer, the beams are out of phase by 180° and interference is destructive (minimum brightness). Since $\sin\theta_1 = n_{2\lambda}\sin\theta_2$ (Snell's law), the conditions for maxima and minima are

$$N\lambda = 2d(n_\lambda^2 - \sin^2\theta_1)^{1/2}$$

For normal incidence:

$$N\lambda = 2dn_\lambda \text{ or } d = N\lambda/2n_\lambda$$

Minima are sharper than maxima and are used whenever possible.

When periodic variations in the reflected beam occur, alternating bright and dark regions (fringes) are formed. Fringes can be formed by changing θ, d (nonuniformity or changes during deposition or etching), n_λ, or λ. The fringe system obtained by thickness changes has been utilized for *in situ* measurement of a plasma-assisted etch or deposition rate of a dielectric film.

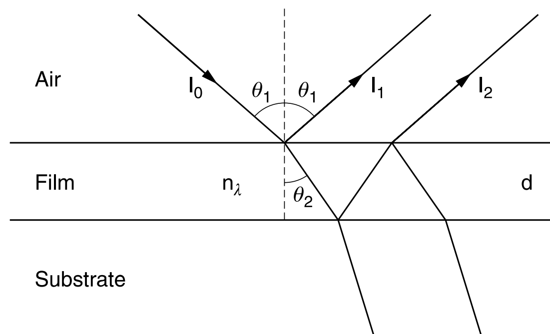

Figure 2.2 Schematic of two-beam reflection or transmission through a transparent substrate.

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The change in n as λ changes is called the dispersion; Pliskin (1987) has compiled an extensive list of the refractive indices and dispersions of inorganic and organic dielectric films used in semiconductor fabrication.

2.2.3.2 Application to Measurement of Film Thickness

There are a number of instruments for thickness determination using interferometry. If the film thickness is known, then n_λ can be determined.

2.2.3.2.1 CARIS/VAMFO

In CARIS (constant-angle reflection interferometry) a spectrometer is used to vary λ at constant θ. In VAMFO (variable-angle monochromatic fringe observation) θ is varied at constant λ. The equations for determining d and n are given in Pliskin and Zanin (1970). If d is known, n can be calculated. The results have been obtained most readily using tables that give the film thickness as a function of the angle of incidence for a particular n, λ, and N. Where necessary, two wavelengths can be used for two successive measurements.

2.2.3.2.2 Multiple-Beam Interfermometry

Multiple-beam interferometry produces sharper fringes (Pliskin and Zanin, 1970). There are two techniques: FIZEAU fringes, generated by monochromatic light which represent contours of equal thickness; this is useful for examining nonuniform films and has been called the TOLANSKY method. The other, fringes of equal chromatic order (FECO), is a more accurate technique. Collimated white light is used to illuminate a sample at normal incidence; the reflected light is dispersed by a spectrometer which varies λ to produce fringes. Pliskin and Zanin (1970) have discussed the principles of the method.

2.2.3.3 Commercially Available Instruments

Interferometric techniques are the basis for instruments available commercially. These systems include rapid automated data acquisition, computation on the basis of a value of n supplied by the user, wafer positioning/mapping, as well as the capability of displaying thickness maps in 2D and 3D (e.g., Nanospec, Prometrix).

An adaptation of the VAMFO technique is the beam profile reflectometer (BPR) (Willenborg et al., 1991); it is available commercially (Opti-Probe) with the usual automation capabilities. The claim for the system is that it has the speed of spectrometer measurements with the accuracy of ellispometry, using a small spot size. A linearly polarized laser beam is focused through a high numerical aperture (NA) microscope objective. A bundle of light rays is thus incident on the surface of the sample, with the central ray normal to the surface. For a 0.9 NA lens, the angles of the bundle range from 0° to $\pm 64°$. Each ray undergoes interference in the film. A line of rays is P-polarized relative to the plane of incidence and an orthogonal line is S-polarized. The measurements are: P- and S-interference profiles and the total reflected power enabling both n and d to be determined.

2.2.4 Prism Coupler

The principles of this method have been given by Tien et al. (1969), Tien (1971), and Wei and Westwood (1978) and the application to thin films on Si by Swalen et al. (1976) and Adams et al. (1979).

A schematic of a prism coupler used to measure d and n is shown in Figure 2.3a. A highly refractive prism and a thin-film coated substrate are pushed into close contact. A laser source and a photodiode detector are mounted on a rotating platform. The angle of incidence of the laser light

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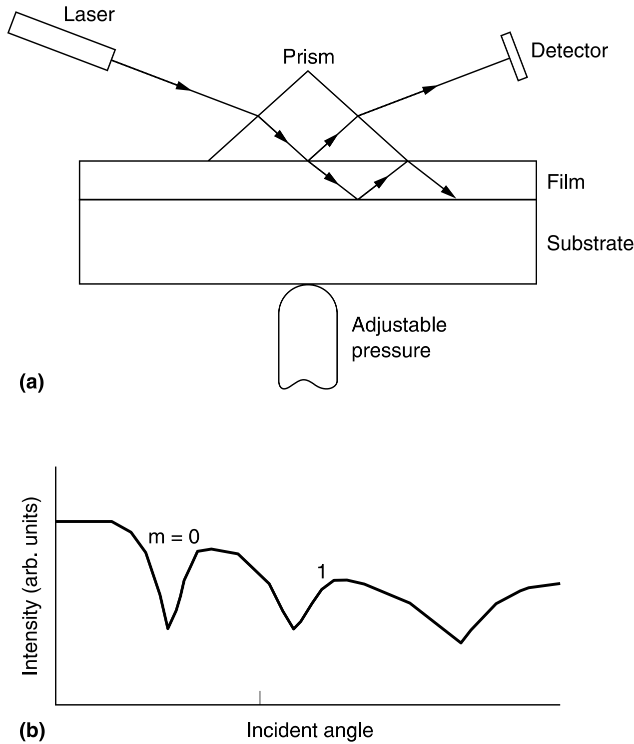

Figure 2.3 (a) Schematic of a prism coupler. (b) Intensity of signal vs. incident angle. (From Adams, A.C. and S.P. Murarka, *J. Electrochem. Soc.*, 126, 334, 1979. Reproduced with permission of the Electrochemical Society, Inc.)

onto the prism face is varied. At the so-called coupling angles, the light is coupled into the film, decreasing the intensity of the reflected light, which is detected by the photodiode.

These angles are a function of n and d; by measuring two coupling angles, both may be computed. There is a minimum thickness, which depends on λ, for the coupling to occur. Figure 2.3b shows the reflected intensity as a function of the coupling angle.

The technique has the particular advantage of allowing the determination of the value of n parallel to the surface of the film and perpendicular to it. This is done using polarized light: the TM mode (electric vector parallel to the surface) yields the value of n in the plane, and the TE mode (electric vector perpendicular to the surface) yields the value perpendicular to the surface.

2.2.5 Other

A new technique for measuring the thickness d and optical constants n_λ and k_λ of a thin film simultaneously is the analysis of reflectance or transmission measurements by the dispersion equations developed by Forouhi and Bloomer (1986, 1988) and patented by them (Forouhi and Bloomer, 1990). The n&k Analyzer consists of the data acquisition hardware and the software for analysis and is supplied by a company called n&k Technology.

2.3 INFRARED (IR) SPECTROSCOPY

Infrared spectroscopy is a powerful technique and one used frequently for characterizing dielectric films.

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2.3.1 Origin of IR Bands

The vibrations of individual atoms within a molecule; e.g., stretching, bending, and rocking modes, absorb energy in the IR if there is a change in the dipole moment. IR spectroscopy consists of the detection and measurement of the position and intensities of the absorption of IR radiation. Transmission is preferred over reflection for reasons enumerated by Pliskin (1973) who also listed the characteristics of the Si substrate required for the best results. Transmitted spectra are plotted as percent transmission on the linear scale of wavenumber, cm^{-1} (which is equal to $1/\lambda$ where λ is expressed in centimeters; the wavenumber is proportional to the frequency of the vibrating unit ν, i.e., wavenumber $= \nu/c$). The position of the band identifies it; the exact position and the half-width can supply information about the quality of a film. Since the peak position can also vary with thickness (Pliskin and Lehman, 1965), equal thicknesses are required when making comparisons.

2.3.1.1 IR Bands

The position and identification of many of the IR bands that are often used are listed in Table 2.2. They are discussed in subsequent sections of this chapter as well as in Chapter 4.

2.3.2 IR Spectrometers

2.3.2.1 Dispersion Spectrometers

Much of the early work was done using dual-beam dispersion IR spectrometers, using a grating or a prism. A film-coated wafer and a bare wafer (the reference) are scanned continuously through the wavelength region of interest and the output is displayed on graph paper, which is driven in synchronism with the dispersing system of the monochromator. Alignment is critical. Sensitivity is a function of the scan speed; greater sensitivity requires longer data collection time. This increases the hazards of component drift and, in some cases, interaction of the film with the ambient. This

Table 2.2 IR Frequencies and Their Identification

Band Position (cm^{-1})	Identification
1050–1100	Si–O stretch
~810	Si–O bending
~450	Si–O rocking
3650	H-bonded Si–OH
~880	Si–H in O-deficient SiO_2
~2260	Si–H in O-deficient SiO_2
3400–3300	Absorbed H_2O
~2160	Si–H (in nitride)
850	Si–N
3350	N–H
930	Si–F
1370	B–O
~670	B–O
~920	B–O–Si
720	B–O–B
~1050–950	P–O
~1350–1300	P=O
2976	Si–CH_3

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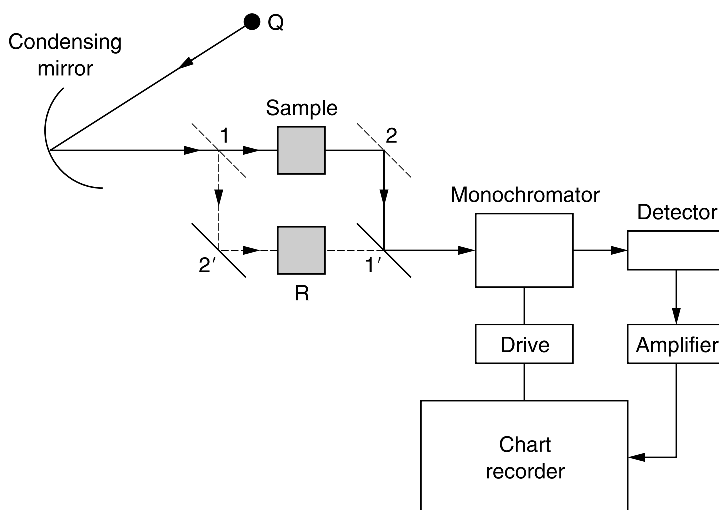

Figure 2.4 Schematic of a recording IR spectrometer.

last can be minimized by flushing the sample compartment with dry N_2. Analysis of the output graph is usually manual, but the data can be fed into a computer. A schematic of a typical spectrometer is shown in Figure 2.4.

2.3.2.2 Fourier-Transform IR (FTIR) Spectrometers

A typical instrument design is shown schematically in Figure 2.5. These instruments are available from several manufacturers and are now the instruments of choice.

The entire frequency (wavelength) range of interest is passed through the spectrometer simultaneously, which produces an output signal containing all the frequencies. This interferogram is fed into a computer (which is an integral part of the apparatus) which performs a mathematical operation called a Fourier transform. The output is a spectrum of intensity vs. frequency. Data collection is rapid, reducing the potential problems of system component drift and wafer instability, but requires separate scanning of sample and reference.

2.3.3 Application to SiO_2

An IR spectrum of a film of interest in semiconductor fabrication, one of a thermally grown SiO_2 film (often used as a basis for comparison with other deposited oxides), is shown in Figure 2.6. The prominent peaks are due to the various vibrations of the Si–O–Si bond. The strongest peak, at 1075 cm^{-1}, is due to stretching, the broader, weaker peak at 800 cm^{-1} to bending, and that at 450 cm^{-1} to rocking.

One important application of IR spectroscopy has been the study of deposited SiO_2 films. For example, for a pyrolytic SiO_2 film, the position of the Si–O stretching band at ~1050–1100 cm^{-1} is shifted to lower frequencies (lower wavenumber, higher wavelength) and the band is broadened by porosity, strain, and oxygen deficiency. An example of the shift due to densification is shown in Figure 2.7.

However, Pliskin (1973) points out that one cannot assume that any band changes are due to only one property change. This caveat is illustrated by the example of an oxide which has strained bonds and is initially porous, so that the IR band due to the Si–O stretch is broad and peaks at a lower frequency. Such oxides react very readily with water to form Si–OH groups, relieving the

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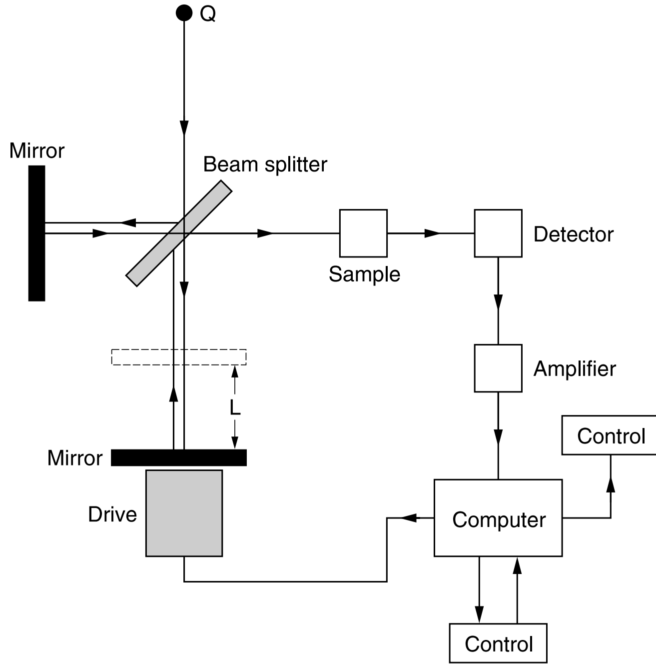

Figure 2.5 Schematic of an FTIR system.

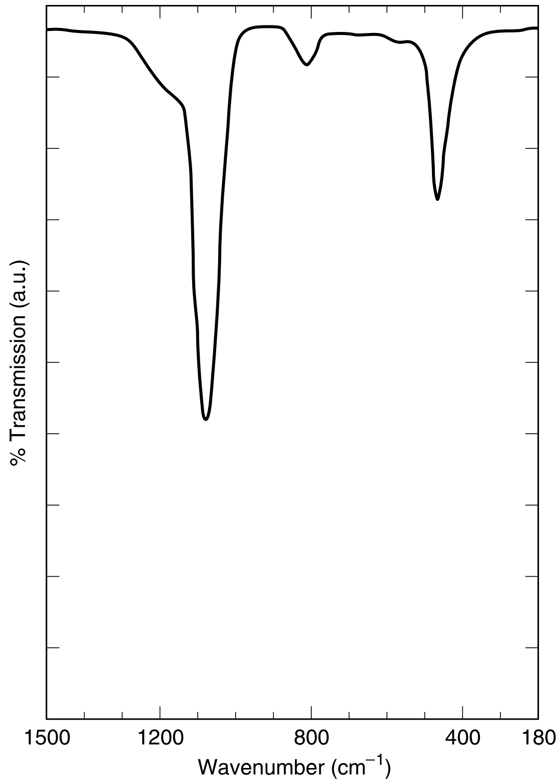

Figure 2.6 IR absorption spectrum of thermally grown SiO_2 film.

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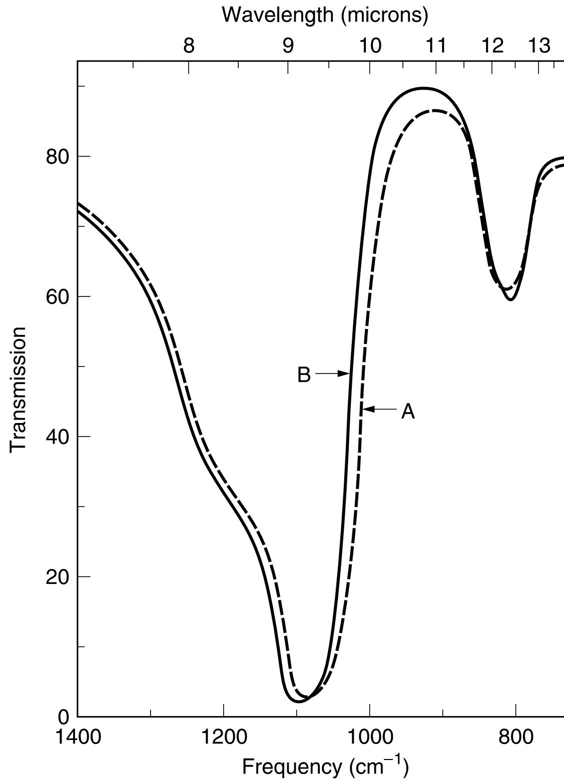

Figure 2.7 IR spectra showing the effect of steam densification of a pyrolyic SiO_2 film. Spectrum A: as-deposited oxide; spectrum B: oxide after densification. (From Pliskin, W.A. and H.S. Lehman, *J. Electrochem. Soc.*, 112, 1013, 1965. Reproduced by permission of the Electrochemical Society, Inc.)

strain. The band will become sharper and will be shifted to higher frequencies, although no densification has occurred. This was verified by Machonkin and Jansen (1987).

The effect of oxygen deficiency was demonstrated clearly by Pai et al. (1986) who correlated the frequency of the Si–O–Si stretching vibration with the composition of SiO_x films. As x was varied from 0 to 2 (Si → SiO → SiO_2) the peak position increased linearly from >950 cm^{-1} to ~1100 cm^{-1}.

2.3.3.1 Detection/Measurement of Impurities

The identification and measurement of impurities such as –OH and H_2O by IR spectroscopy (Pliskin, 1967) has been a very important technique in evaluating deposited SiO_2 films and is relied upon frequently. The effect of moisture absorption on the stretching Si–O band in the spectrum of Si–OH and H_2O is illustrated in Figure 2.8. The other bands are not usually examined since they do not provide additional information.

The identification of Si–OH as hydrogen bonded (3650 cm^{-1}) is based on the fact the band due to free SiOH occurs at higher frequencies and is quite sharp The band for absorbed water occurs at 3400–3300 cm^{-1}. The loss by heating of water and "loosely" bound OH (i.e., silanol groups having a common silicon atom or are near neighbors and form water readily) can be followed by IR spectroscopy since the broad band attributed to them vanishes.

In incompletely oxidized silicon oxide films, absorption bands have been observed at ~2260 cm^{-1} and at ~880 cm^{-1}. These have been assigned to Si–H (Pliskin, 1973). Lucovsky and

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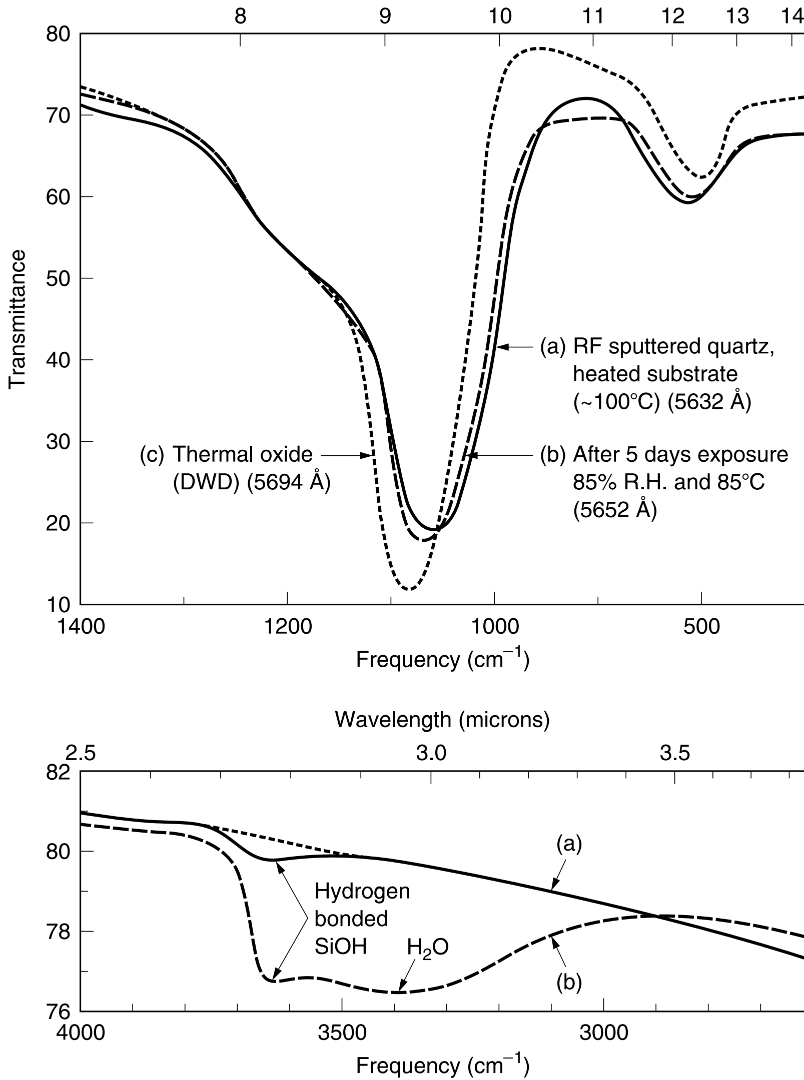

Figure 2.8 IR spectra showing effect of moisture on a sputtered SiO_2 film. (From Pliskin, W.A., in *Measurement Techniques for Thin Films*, Schwartz, B. and Schwartz, N., Eds., Electrochemical Society, NJ, 1967, p. 280. Reproduced by permission of the Electrochemical Society, Inc.)

Tsu (1987) characterize these bands, also seen by them in O-deficient oxide films, as the bond stretching (2250 cm^{-1}) and bond bending (870 cm^{-1}) vibrations of the Si–H bond. Lucovsky and colleagues have relied heavily on many of these findings in their IR studies of silicon oxides deposited by remote plasma deposition (e.g., Lucovsky et al., 1986, 1989; Lucovsky and Tsu, 1987; Pai et al., 1986; Theil et al., 1990).

Other impurities, such as CO and CO_2, have been detected by IR spectroscopy (Pliskin et al., 1969).

2.3.3.2 Detection/Measurement of Dopants

The presence of P in PSG or BPSG films is detected at ~1350–1300 cm^{-1} (P = O) and at ~1050–950 cm^{-1} (P–O) (Hurley, 1987). Incorporation of P causes the Si–O band to shift to higher

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frequency (Pliskin and Lehman, 1965). Adams and Murarka (1979) reported that the P content of PSG films, determined by IR, agreed (to within ±0.3 w/o P) with the results of chemical analysis, neutron activation, and microprobe techniques.

Other additives have been detected and estimated by IR; for example, B in BSG or BPSG: the B bands in BSG or BPSG are at 1370 cm^{-1} and ~670 cm^{-1} (B–O), and at ~920 cm^{-1} (B–O–Si) (Pliskin, 1967; Rojas et al., 1992). Wong (1976) mentions a B–O–B band at 720 cm^{-1}. The B content in silica glass has been determined by the ratio of the absorbance maximum of the B–O band at ~1370 cm^{-1} to that of the Si–O band at ~1070 cm^{-1} (Rojas et al., 1992). The Si–F band in F-doped SiO_2 appears at ~930 cm^{-1}.

The correlation of band intensities with concentration for other many bands has been made using the same techniques used for P concentration.

2.3.4 Application: Silicon Nitrides

IR spectroscopy has played an important role in the characterization of silicon nitride films, particularly in terms of Si–N, N–H, and Si–H bands. Lanford and Rand (1978) correlated the spectral intensities of the Si–H and N–H bands with the H content as determined by nuclear reaction (see below). An IR spectrum of a "typical" PECVD nitride film is shown in Figure 2.9.

The use of multiple internal reflection (MIR) of IR radiation has also been used to study the H content and the effects of annealing of very thin films of LPCVD silicon oxynitride (Stein, 1976) and CVD nitride (Stein and Wegener, 1977). The many reflections amplify the signal from very thin films; this is illustrated in Figure 2.10.

2.3.5 Quantitative Measurements of Spectra

The absorption band intensities in transmission spectra are approximately proportional to thickness or concentration, i.e., they obey Beer's law. Although the integrated band intensity is the best measure of absorption intensity, the absorption intensity at the peak maximum (the optical density, OD) is a good approximation and can be used to determine the concentration.

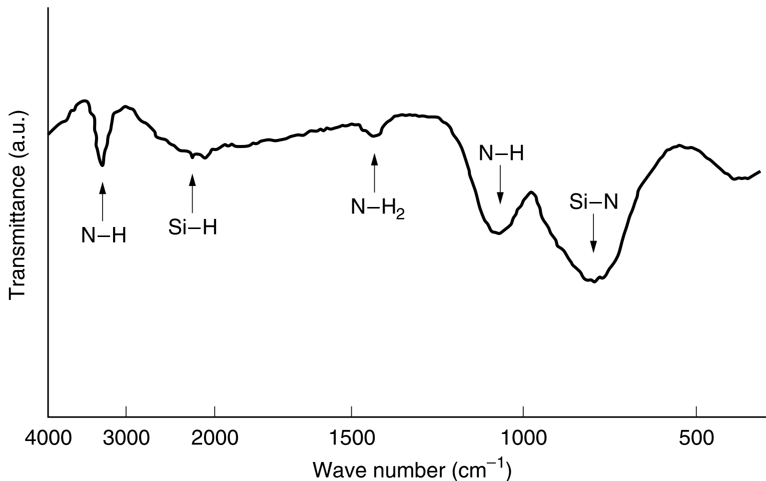

Figure 2.9 Typical IR spectrum of a PECVD SiN film. (Reprinted from Murakami, K., T. Takeuchi, K. Ishikawa, and T. Yamamoto, *Appl. Surf. Sci.*, 33/34, 742, 1988. With permission. Copyright 1988, Elsevier.)

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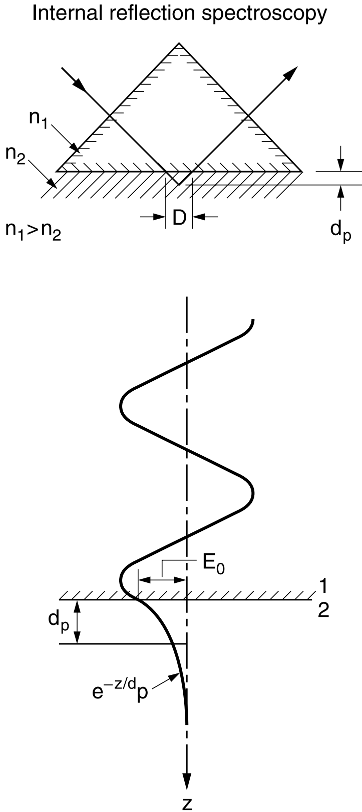

(1) $d_p = \lambda/2\pi n_1 \, [\sin^2\theta - (n_{21})^2]^{1/2}$

$n_{21} = n_2/n_1$

λ = wavelength in free space

θ = angle of incidence

For Si_3N_4/Si and $\theta = 45$

d_p = 3490Å for NH, and 5350Å for SiH

when $d_{film} << d_p$ ($E \approx$ const)

(2) $d_{eff_\perp} = 4\, n_{21}\, d \cos\theta$ ($\perp$ polarization)

$= 3.30d$

(3) $$d_{eff_{||}} = \frac{4\, n_{21}\, d \cos\theta\, [(1 + (1/n_2)^4) \sin^2\theta - (1/n_1)^2]}{(1 - (1/n_1)^2)\, [(1 + (1/n_1)^2 \sin^2\theta - (1/n_1)^2]}$$

$= 3.22d$ (II polarization)

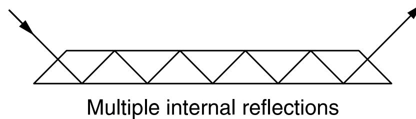

Figure 2.10 Internal reflection technique for obtaining IR absorption data for thin films. (From Stein, H.J. and H.A.R. Wegener, *J. Electrochem. Soc.*, 124, 908,1977. Reproduced by permission of the Electrochemical Society, Inc.)

Quantitative analysis of the water and silanol content of SiO_2 films is related to the band intensities:

$$W = -14A_{3650} + 89A_{3330}(2.2/\rho)$$
$$S = 179A_{3650} - 41A_{3330}(2.2/\rho)$$

where W = wt% water (including H_2O from easily removed silanol), S = wt% OH as silanol; ρ = film density, and $A\nu$ = OD/μm film at frequency ν (Pliskin, 1973, 1977).

2.4 RESISTIVITY OF METAL FILMS

2.4.1 Introduction

The electrical resistivity of a metallic conductor is one of its most important properties. Lowering the resistance of the interconnections decreases signal propagation delay. Thus the trend toward Cu, away from Al and its alloys, although the resistivity of the barriers in which Cu must be encapsulated increases the total resistance and must be taken into account when considering the net advantages of a shift in metallization.

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2.4.2 Sheet Resistance

2.4.2.1 Definition

The resistance of a rectangular-shaped section of a film, shown in Figure 2.11, measured parallel to the surface of the film is

$$R = (\rho/t)(l/w)$$

where ρ is the resistivity of the film, and t the thickness, l the length, and w the width of the conductor sample. If $l = w$, $R = \rho t$ and this quantity is called the sheet resistance R_s; R_s is independent of the size of the square and depends only on the film thickness and is expressed as ohms/square, $\Omega/\square$. Thus, if the thickness is known, the resistivity can be obtained from the measured sheet resistance.

2.4.2.2 Measurement

2.4.2.2.1 Probes

A four-terminal method is required since it eliminates the effect of contact resistance between the film and the probe. Current is fed to the ends of the sample and the voltage drop across several squares is measured, as shown in Figure 2.12a, and the resistance determined: $R = V/I$. To eliminate the need for fabricating special samples, a linear array of equally spaced probes can be placed on a metal surface, as shown in Figure 2.12b; current is fed to the outer probes and the voltage drop across the inner probes is measured to yield R_s (Maissel, 1970):

$$R_s = 4.532V/I$$

The smaller the probe spacing, the better the resolution. A square array, shown in Figure 2.12c, is used for higher resolution. In this case (Maissel, 1970)

$$R_s = (V/I)(2\pi/\ln 2) = 9.06V/I$$

2.4.2.2.2 Eddy Currents

Eddy currents can be induced in a conductor when it moves through a nonuniform magnetic field or in a region where there is a change in magnetic flux. Measurement of such currents is the basis for noncontact resistivity measurement, a desirable technique since it avoids the possibility of probe damage.

There are commercially available systems which can measure the sheet resistance of a film at many points on the surface, rapidly, and have the software for plotting a resistance contour map of

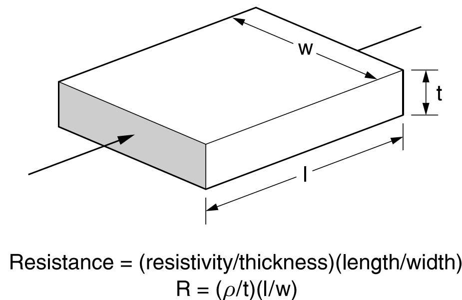

Figure 2.11 Definition of sheet resistance.

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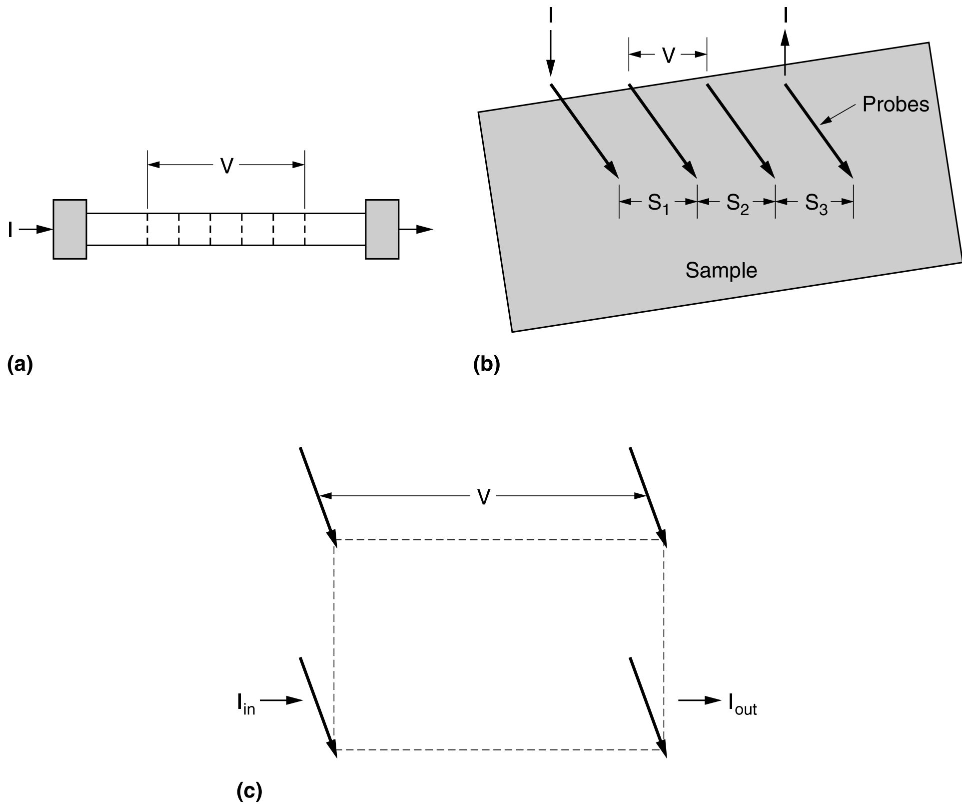

Figure 2.12 (a) Direct measurement of sheet resistance. (b) In-line four-point probe for measuring sheet resistance. (c) Square probe array for measuring sheet resistance.

the surface. The Tencor OmniMapNC110 uses a very small coil and thus can measure the resistance on a small blanket area directly on a product wafer.

If the sample is other than a straight strip, the resistance calculation is more complex, as demonstrated by Hall (1967).

At very low film thicknesses, the resistivity decreases rapidly with increasing thickness, reaching a constant value (in some cases, the bulk resistivity). However, the resistivity of thin films is often greater than the bulk resistivity, due to impurity inclusion and structural defects. If any change is seen when annealing single-metal films, it is a reduction of resistivity. Alloy films may behave differently, due to morphological changes, etc. The addition of other constituents (alloying) increases the resistivity.

2.4.2.3 Temperature Dependence

The resistivity of metal films decreases with decreasing temperature; the temperature coefficient of resistance (TCR) α_T is given by

$$\alpha_T = (R_1 - R_2)/R_T(T_1 - T_2)$$

where $T_1 > T > T_2$. However, if the films are very thin and not continuous, TCR may have a negative value.

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2.4.3 Via Resistance

2.4.3.1 Introduction

Low interlevel (via) resistance (metal-to-metal contact) is another essential ingredient for a fast, reliable MLM device. The subject of contact resistance (metal to semiconductor) is covered in Chapter 3.

2.4.3.2 Measurement

An accurate method for determining the via resistance and the effect of various processing conditions on it is to measure individual vias (preferably of different sizes) using a "double L" (Kelvin) structure, shown in Figure 2.13. This is a four-point measurement which eliminates the influence of probe resistance. An assessment of the via yield for a given process is obtained from via chains; the larger the number of vias in the chain, the better the assessment for a dense chip.

2.4.3.3 Contributors to Via Resistance

Even a clean metal-to-metal contact will exhibit some resistance beyond that due to the number of squares in the area because of current crowding as the current flows from the interconnect into a constricted via hole. Steep via slopes (resulting in thinned metal over the step) and misaligned vias will also add to the resistance; the use of via plugs eliminates the first problem and improved lithographic alignment procedures can minimize the second. The problem remaining, to be discussed in greater detail, is that of an interfacial film.

Some of the common films are organic or carbonaceous and are due to redeposition of organic materials during via etching of a polymer dielectric (Day and Senturia, 1982; Smith et al., 1983) or some SOGs (Shacham-Diamand and Nachumovsky, 1990). Another is specific to Al-based conductors. It is the existence of a film of aluminum oxide at the interface. For example, the native Al_2O_3 on a freshly formed Al surface exposed only to the atmosphere is approximately 3 nm thick. Wildman and Schwartz (1982) reported that the via resistance due to an Al_2O_3 layer increased by

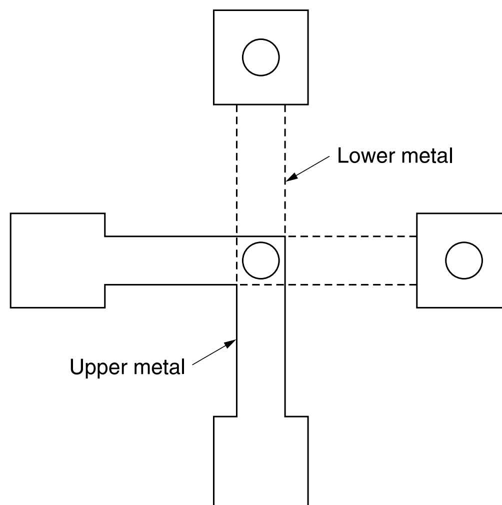

Figure 2.13 "Double L" test structure used for measuring via resistance.

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about one order of magnitude for every 0.2 nm of oxide. Water desorbed from SOG interlevel films during via etch oxidizes the Al surface. Via cleaning, e.g., using a buffered HF (BHF) or BHF/NH_3 dip resulted in thick porous oxide layer (Wildman and Schwartz, 1981); after sintering, however, the via resistance was not abnormally high, probably due to the porous nature of the film which allowed Al interdiffusion during heating. There are, however, many reports of the advantages of an HF dip for removing the oxide if this step is followed by sintering (e.g., Smith et al., 1983). Precautions must be taken to ensure that the BHF is rinsed very rapidly in huge volumes of water to prevent dissolution of the metal which occurs in partially diluted BHF (MacIntyre, 1968).

2.4.3.4 Reduction of Via Resistance

In situ Ar^+ sputter cleaning (Bauer, 1980) or ion milling (Petvai et al., 1978), if done properly, can produce a clean interface requiring no sintering. Bauer found that the presence of Al on the fixturing or on Al blanks in unused positions on the dome (Bauer, 1980) or, even better, sputtering an Al getter electrode before sputter cleaning (Bauer, 1994) suppressed the reoxidation of the cleaned surface by absorbing the moisture in the system. If the cleaned surface can be reoxidized before the next level of metal is deposited, the procedure will not be successful, even though the sputter clean time is sufficient to remove the initial thickness of oxide. However, Tomioka et al. (1989) reported that during sputter cleaning, redeposition of the insulator that surrounds the via left a thin insulating film at the interface.

Alternatives to Ar^+ sputter etching have been proposed. Exposing an oxide-covered Al surface to a CF_4 plasma reduces the O coverage, replacing it with F (Chu and Schwartz, 1976), but AlF_3 is also an insulator and may cause problems. Takeyasu et al. (1994) avoided the potential problem of redeposition of the Al/Al_2O_3 on the side walls of the via by *in situ* RIE of the oxide in BCl_3/Ar before deposition of an Al plug by CVD.

Another alternative is deposition of a thin layer of Ti onto the lower oxidized Al surface, followed immediately by the thick Al-based next metal layer. The Ti will consume some of the oxide by dissolving it in the lattice, not by chemical reduction. Since there is a limit to the amount of oxide the Ti layer can consume, the surface oxide thickness (which may have been thickened by previous processing) can be reduced to that of the native oxide by a dip in phosphochromic etch (H_3PO_4/CrO_3/H_2O). However, the concentration of CrO_3 is critical: too little and H_3PO_4 will attack the Al; too much and certain regions of the chip will be dissolved (Shankoff et al., 1978). Another alternative was proposed by Horie et al. (1984): immediately after deposition, a film of $MoSi_2$ was deposited onto the lower Al surface to prevent oxidation of the Al surface.

2.5 THICKNESS

2.5.1 Introduction

Although some of the following techniques are applicable to dielectric films as well as to metals, they are almost always employed only on blanket films of metals; the optical measurements are preferred for the dielectrics. The method used most frequently in the recent past is stylus profilometry but x-ray fluorescence spectroscopy (XRFS) is now coming into use on the manufacturing line; these are described below.

2.5.2 Early Methods

When stylus profilometry was in its infancy and held to be unreliable and apt to scratch and deform soft films, other methods were preferred. Among them are: (1) gravimetric: density and area

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must be known; (2) beta backscattering (which measures the amount of backscatter from films of beta particles emitted from radioactive source): film and substrate must have a large difference in atomic numbers and standards are required; (3) x-ray absorption and emission: requires expensive equipment and standards; (4) electrical resistance using four-point probe technique: requires accurate knowledge of resistivity which must be constant in the required thickness range (since this often depends on deposition conditions, it is useful for process control, if not for absolute measurement).

2.5.3 Stylus Profilometers

The newest stylus profilometers are viewed as reliable if used properly. There are several suppliers as well as several models from each. The systems have data collection and processing hardware and software including the capability for automated processing.

Initially they were used simply to measure the thickness of a deposited film. For best results, a sharp-edged narrow groove was etched into the film, rather than making a step using a shadow mask during deposition. This had two benefits: better resolution from the steep edge and the ability to level properly using the two steps.

The stylus method is also used to measure step heights of both metals and insulators on patterned wafers, e.g., after RIE. The sizes of the features and the spaces between them have decreased, requiring greater resolution both vertically and horizontally. The new systems provide improved viewing capability for locating measurement sites.

Styli are available in many sizes down to submicrometer radii. Although it is more cost-effective to use a stylus with a large radius because it is less expensive, more rugged, and less likely to cause damage, if the stylus tip is larger than the groove being measured, it will not reach the bottom and register the wrong (too small) depth. The spherical nature of the stylus tip rounds the profiles and broadens them; the effect is more pronounced the larger the tip radius. Decreasing the stylus size increases the downward force of the stylus; this may cause deformation of some surfaces leading to erroneous measurements and lack of repeatability. The equipment provides for the adjustment of the force. If, in trying to avoid damage, the force is set too low, the stylus may hop over features.

The horizontal resolution is increased by increasing the number of measurements made per scan as well as by decreasing the scan speed; different models provide different capabilities. The scan length is also important; the smaller the scan length, the larger the number of measurements. Profilers are supplied by Veeco (Dektak) and Tencor.

The instruments are also used to measure surface roughness.

2.5.4 X-Ray Fluorescence Spectrometry (XRFS)

Routine thickness measurement is a more recent application of this technique. The method is discussed in Section 2.15.

2.5.5 Pump and Probe: Pulsed Picosecond Ultrasonic Technique

A commercially available system for measuring, simultaneously, multimetal films on a production wafer, based on the work of Thomsen et al. (1984, 1986), has been developed by Rudolph Technologies, Inc. The apparatus, called *MetaPULSE*, uses ultrafast light pulses to raise the temperature near the film surface. The resulting rapid thermal expansion launches an ultrasonic wave into the film. When the wave reaches an interface with a lower layer, some of it is reflected back to the surface as an echo; the rest continues into the lower layers. As the echo reaches the surface it changes its reflectivity. A second light pulse detects the change (Morath et al., 1997). A precision of $>1\%$ is claimed for a range of thicknesses of <20 Å to 5 nm.

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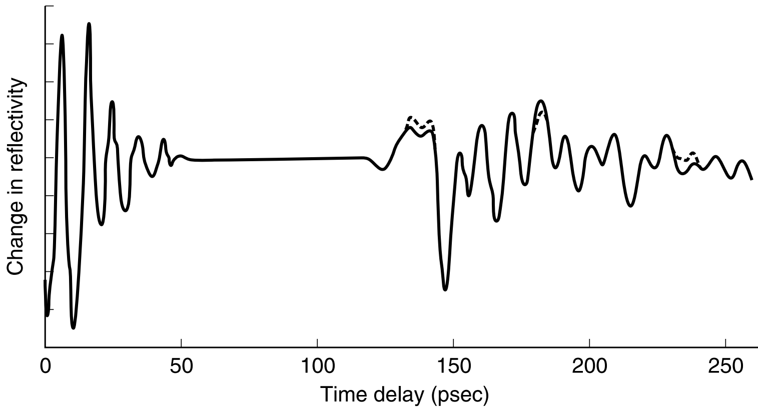

Figure 2.14 Time-dependent reflectivity change for TiN (408 ± 1.2 Å)/Ti (319 ± 1.6 Å)/AlCu (4179.1 ± 0.7 Å)/TiN (1165.2 ± 2.6 Å)/Ti (356.4 ± 3.2 Å)/SiO_2 (987.4 ± 0.4 Å)/Si substrate. (From Morath, C.J., G.J. Collins, R.G. Wolf, and R.J. Stoner, *Solid State Technol.*, 6/97, 85, 1997. With permission.)

An example of the time-dependent change in reflectivity for TiN/Ti/AlCu/TiN/Ti/SiO_2/Si is shown in Figure 2.14. The relationship between time T for sound waves to propagate through the film at the longitudinal velocity of sound v_s and return to the surface and the layer thickness t is

$$T = 2t/v_s$$

The echoes decrease in amplitude with increasing time. Nonideal properties of an interface, e.g., changes in film density, stoichiometry, roughness, adhesion, and contamination, are indicated by the amplitudes of the returning echoes deviating from the ideal., but this phenomenon has no influence on the measured film thickness which uses *only* the *echo time*. A model is constructed from the list of stored materials and, after measurement, software adjusts the parameters of the model to produce a best fit.

The pulsed picosecond ultrasonic technique has also been used to detect ultrathin interfacial layers, e g., CF_x at an Al/Si interface (Tas et al., 1992), and to determine the room temperature thermal conductivity and longitudinal sound velocity in α-diamond and diamond-like carbon (DLC) films (Morath et al., 1994).

2.6 DIELECTRIC CONSTANT OF DIELECTRICS

2.6.1 Introduction

The term dielectric constant as used here (ε) is more accurately called the relative permittivity of an insulator and is one of its most important characteristics. Although ε is used here, k has become the symbol for the dielectric constant in many recent publications. In applications in which minimizing signal delay and cross talk is of paramount importance (i.e., in the interconnections) ε should be as low as possible. There are other applications (not considered as a topic in interconnection technology) for which charge storage is important, so that ε should be as high as possible.

2.6.2 Measurement

The value of ε, at different frequencies and temperatures, is determined from capacitance–voltage (C-V) measurements using a parallel plate capacitor:

$$C = \varepsilon\varepsilon_0 A/d$$

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were C = capacitance, ε_0 = permittivity of free space, A = area, and d = dielectric thickness. Niccolian and Brews (1982) discuss the subject of C-V techniques in detail; Mego (1990) has published brief guidelines for interpreting C-V data.

The capacitor may be a dielectric sandwiched between two metal electrodes (MIM) or between a metal electrode and a silicon substrate (MIS), which is called an MOS structure when the dielectric is SiO_2. The MIS or MOS capacitor is often preferred; this avoids any problems of surface roughness in the lower metal film. In this case, a metal film is deposited on the back of the wafer for contact unless the silicon is very heavily doped (i.e., has very low resistivity). The upper electrode is usually deposited through a shadow mask. Unless the electrode area is very large, the sample is sometimes subjected to a light etch to remove any halo, formed by scattering beneath the mask, to eliminate any error in the electrode area. Mercury probes are used at times, to avoid evaporating the electrodes, but control of the area of the electrode is rather poor. However, their use can be a convenience in another way. When it becomes necessary to heat the dielectric, e.g., to study moisture evolution and absorption, the evaporated metal dots must be etched off before heat treatment and redeposited before making the next measurement.

The dielectric constant is almost always measured at high frequency, i.e., $\geq$10 kHz, to avoid the problem of surface inversion in MIS or MOS capacitors, in which the surface layer of the substrate Si becomes conductive.

2.6.3 Precautions in Measurements

When using an MIS or MOS capacitor for measurement of ε it is essential that the Si surface be in full accumulation. In accumulation, the majority carriers are accumulated at the Si surface; as a result, the capacitance of the Si layer is negligible so that only the capacitance of the dielectric is measured. For p-type Si a negative voltage is applied to the metal electrode; for n-type the polarity is reversed. Taking a full C-V curve will ensure that this condition is met. Another precaution is avoiding formation of a p–n junction at the surface by, for example, doping an n-type wafer with B. This appeared to have occurred during deposition of BN (Nguyen et al., 1994) and may also occur during deposition of BSG and BPSG films.

2.6.4 Dissipation Factor

Since insulators have a finite parallel resistance R, the total impedance Z is found from the vector diagram (ωC vs. $1/R$) shown in Figure 2.15, where $\omega = (2\pi)$ frequency and the angle δ is defined.

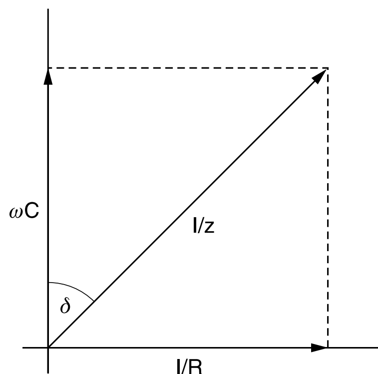

Figure 2.15 Dissipation factor: vector diagram of a practical capacitor showing δ ($\tan \delta$ = loss tangent).

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The value of sin δ is a measure of the energy absorbed in the insulator. For most insulators, R is very large (the loss is very small) so that sin $\delta \sim \tan \delta = 1/\omega RC$ which is readily measured on an appropriate bridge. The quantity tan δ is called the dissipation loss factor or loss tangent; it is very small ($< 10^{-3}$) in good inorganic dielectrics such as SiO_2. Organic films are often electrically "leaky," and thus tan δ may have an appreciable value.

The change in dissipation factor has been used to follow the cure cycle of several thin polyimide films; in this case it reached a minimum value (~0.01) when the films were fully cured but increased upon further heating when degradation set in (Rothman, 1980). The values of the dissipation factors were even lower (<0.004) for other properly cured polyimide films (Samuelson and Lytle, 1984).

2.7 BREAKDOWN STRENGTH

2.7.1 Measurement

A parallel plate capacitor is also used for the current–voltage (I-V) measurements in determining the breakdown strength of an insulator. A DC voltage is applied to a large number of individual capacitors sequentially and the current is measured. The voltage is either ramped (increased continuously) or stepped until a current spike (indicating a self-healing breakdown) is observed or until the capacitor fails catastrophically (becomes shorted). The voltage when breakdown occurs is called the breakdown voltage and the field (V/cm) the breakdown strength. When the catastrophic breakdown criterion is used, the distribution of breakdown voltages of the individual capacitors is usually narrower and the field higher. The distribution depends on the electrode area (larger area, lower strength) rate of change of the voltage (slow increase, lower strength), and may be sensitive to the nature of the lower electrode, its surface, and its method of preparation (Patrick et al., 1992). Those authors also reported that for PECVD films deposited and measured under identical conditions, there was a wide range in the breakdown voltage distribution and its maximum value, making characterization of a dielectric film by this technique questionable.

2.7.2 Application

The low-field breakdowns (not the maximum strength) are the important ones for assessing the reliability of an insulator; this subject is discussed in greater detail in Chapter 7. In device operation, the voltages are low and the thickness of the interlevel insulators as well as the width of the dielectric between adjacent conductors relatively large, so that the operating fields are quite low. (This is in contrast to the fields experienced by the insulator in an FET device.)

A narrow distribution of breakdown strengths is taken as an indication of the homogeneity of the film. The very low-field breakdowns are usually attributed to defects; a preponderance of them is an indication of a very poor dielectric. The poor quality may be due to, for example, improper formulation, application, or curing of a spin-on insulator, or a poor choice of deposition parameters for PVD, CVD, or PECVD films, but the influence of surface preparation cannot be ignored.

2.8 ADHESION

2.8.1 Introduction

A loss of adhesion or delamination results when the bonding forces at the interface between two films are weakened. This may be the result of surface contamination, surface modification

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by a previous processing step, or may be inherent to the specific layers, e.g., Cu on SiO_2, some photoresists on hydrophilic surfaces, etc. Local concentration of stress at edges and bends (stress risers) may lead to adhesion loss. Poor adhesion of a film that has a high compressive stress may result in blistering; in a film in which the stress is highly tensile delamination and cracking result, particularly where there is a stress riser.

The adhesion energy is the difference between the free energy of an interface formed between two surfaces when they are brought together and the original surfaces.

2.8.2 Measurement

There are several techniques for measuring adhesion. Comparisons are valid when different systems are evaluated by a single technique, but results from one kind of test are not readily comparable to those obtained by a different method. However, relative adhesion values are useful. Several systems are of interest: adhesion of an insulator (1) to a metal, (2) to itself, (3) to another insulator, and (4) to the semiconductor substrate as well as adhesion of a metal to various insulators.

2.8.2.1 Scotch Tape Test

Perhaps the most common and certainly the simplest test of adhesion is the scotch tape test in which a piece of adhesive tape is attached to the surface of a film and pulled. It is qualitative and subjective but does screen for some minimum level of adhesion. If the top layer peels, it is usually concluded that the adhesion is too poor to warrant any further testing, and that further work is necessary to change the materials or the process of applying the film or to modify the underlying surface, e.g., by roughening, plasma cleaning, using an adhesion promoter, etc.

The causes of poor adhesion are sometimes determined by examination of each of the surfaces of the failed bond by analytical techniques such as XPS or AES. These same methods are used to assess the effectiveness of surface treatments designed to improve adhesion (Bacchetta et al., 1994).

2.8.2.2 Peel Test

A more quantitative test is the 90° peel test, which can be used when one of the films is thick and ductile. It has been used widely and successfully to measure the adhesion between a polymeric film and metals or inorganic layers but not between two polymeric layers. The concept of the test is shown in Figure 2.16.

This technique is not practical for measuring the adhesion between thin metallic films and inorganic insulators because of the difficulty in attaching the film and initiating peel.

The force required to peel a unit length of film, i.e., separating the film from the substrate, thereby producing two surfaces from the interface, is used to determine the adhesion stress. The puller can be advanced at a programmable speed and has a force sensor to measure the peel force. At steady state, the peeling force is expressed in g/mm (or equivalent units).

It may be necessary to use films for the test that are significantly thicker than those used in a real structure. Since the film is subjected to a steady stretching or deforming force during peel, it is important that the deformation energy be small compared to the total peel energy to avoid the use of corrections which can introduce errors.

2.8.2.3 Scratch Test

In the scratch test, a smoothly rounded tip is drawn across the surface; the vertical load applied to the point is gradually increased until a clear channel is produced (Ahn et al., 1976). The action of the tip involves plastic deformation of the substrate which produces a shearing

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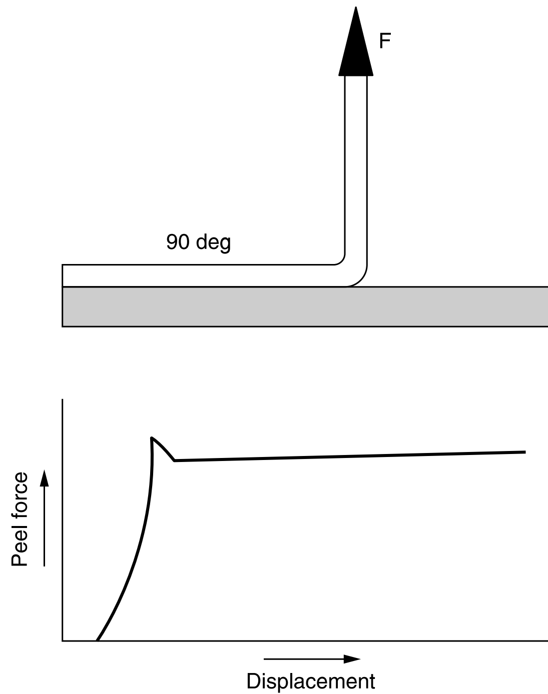

Figure 2.16 Peel test arrangement for measuring stress.

force at the film substrate interface. Hamersky (1969) pointed out that the accuracy depends on the point radius and larger radii were more reliable. Chapman (1974) noted that optical transparency was not a suitable measure of loss of adhesion since the film could become thin and translucent without detachment. A more sophisticated scratch test used a diamond microindenter (microtribometer) (Baba et al., 1986; Otterman et al., 1993). In this technique, as the stylus traversed the sample, the signal generated in a coil by a moving magnet was recorded by a true rms voltmeter. As the load is increased, V_{rms} increases linearly until a break occurs, at which point V_{rms} increases precipitously. The technique has been used to measure the adhesion of several metal and oxide thin films. This method avoids the error cited by Chapman, since it does not depend on visual examination. Valli (1986) in his review of adhesion test methods for thin hard coatings has discussed the scratch test in detail.

2.8.2.4 Blister Technique

Another method is the blister or bulge technique, in which a window is etched in the substrate to expose the interface between it and a thin film. A pressure difference is applied to the film which is deformed; at a critical pressure the radius of the blister expands and the film peels, i.e., debonds. Gent and Lewandowski (1987) and Sizemore et al. (1993) are among those who have analyzed and modeled the test. The crack extension force can be obtained from the measurement of the critical pressure and volume. The test has been applied to films such as polymers, silver, CVD diamond, and silicon nitride. Small et al. (1993) discussed possible causes for inconsistencies in results and suggested improvements, e.g., the use of initially flat reflective samples of well-defined size and geometry whose fabrication they describe.

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2.8.2.5 Stretch Deformation

A stretch deformation method for direct measurement of the adhesion energy was developed by Ho and Faupel (1988). A test sample consists of a polymer substrate clamped at both ends and a metal overlayer. The adhesion energy is measured from the difference in the load vs. elongation curves between film/substrate and substrate alone; the details can be found in their paper.

2.8.2.6 Other Methods

Valli (1986) has mentioned a number of additional tests: ultracentrifugal and ultrasonic tests, acoustic imaging, and laser spallation.

2.9 MECHANICAL PROPERTIES

2.9.1 Definitions

Stress (σ) is the force per unit area.

Strain (τ) is the stretch per unit length.

The elastic or Young's' modulus *(E)* is a material property; its value is an excellent indication of the ability of a film to withstand the rigors of chemical mechanical planarization (polishing), CMP (Chapter 6, Section 8). The value of E of most of the low-ε films is about an order of magnitude lower than that of the films they replaced.

Poisson's ratio *(ν)* is defined as the ratio between the lateral and longitudinal strains.

The elastic biaxial modulus is $E/(1 - \nu)$. It is defined for thin films as

$$(\sigma) = [E/(1 - \nu)]\tau$$

i.e., by the slope of a σ vs. τ curve.

Hardness *(H)* is a measure of the degree of resistance of a body to permanent deformation when it is subjected to a local high stress. The value tracks that of E and the yield strength. It is an indication of the compatibility with the mechanical component of CMP; soft films are easily scratched by an abrasive.

2.9.2 Introduction

The mechanical properties of the new low-ε dielectric films are significantly different from those of the earlier ones they are replacing. For example, many of the newer films have inadequate mechanical strength and hardness and can be damaged during CMP. The coefficient of thermal expansion (CTE) is larger than that of the conventional insulators (SiO_2, SiN) resulting in large thermal strains/stresses during processing. Renewed emphasis, therefore, has been placed on the determination of these parameters. Some of these will be described; with a few exceptions they are applicable to thin films coated on a substrate.

2.9.3 Stress

2.9.3.1 Introduction

Tensile films may fail by delamination or by cracking and the crack may be propagated into the substrate. Very highly compressive films may buckle and eventually delaminate. Thouless (1991)

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has reviewed these failure mechanisms and the conditions that determine which one will operate. Thus measurement of film stress is an important part of process development, guiding the choice of materials and processes.

When a surface is coated with a tensile film (by convention the stress is positive) the coated side is concave; it is convex when the stress is compressive (negative). Film stress is expressed as dyne/cm^2 or as MPa (100 MPa = 10^9 dyne/cm^2).

2.9.3.2 Measurement of Stress

Stress in dielectric films, such as deposited oxides and nitrides of Si, organic and other low-ε films, thermally grown SiO_2, etc., as well as in metal films, have been measured by the methods described below. Murarka (1994) has discussed the origin of stress in metallic films and analyzed the stresses in multilayer metal films.

2.9.3.2.1 Cantilevered Bending Beam

In this method, illustrated in Figure 2.17, the deflection of one end of a coated beam is measured while the other end is clamped. The stress σ is given by

$$\sigma = [E_s t_s / 3L^2 t_f (1 - \nu)]\delta$$

where E_s is Young's modulus of the substrate, ν Poisson's ratio of the substrate, L the length of the beam (substrate), t_s and t_f the thicknesses of the substrate and film, and δ the deflection. The term $E/(1 - \nu)$ is called the elastic biaxial modulus. Single-crystal Si is the substrate used most commonly, but others, e.g., Ge, GaAs, and quartz, have also been used, particularly in determining the elastic constants of deposited films, as discussed below. Table 2.3a lists the values of $E/(1 - \nu)$ for these substrates. The length of the beam is much greater than its breadth. The sensitivity of the method depends on the detection systems used to observe the movement. Campbell (1970) has described several of them: microscopic observation, use of a contactometer, electromechanical, capacitive, or inductive device, a hot wire, or a Michelson interferometer. Abermann (1992) measured the stress during the growth of thin films on a quartz bending beam substrate under UHV conditions.

2.9.3.2.2 Curvature

This method is most widely used for determining the stress in a thin film. The change in curvature of a circular substrate (usually a silicon wafer), resulting from the deposition of a thin film, is measured. This has the advantage of simplicity of sample preparation. The stress is given by

$$\sigma = [E_s/6(1 - \nu)][t_s^2/t_f][1/R_f - 1/R_s]$$

where R_s is the radius of curvature before film deposition and R_f the radius after deposition.

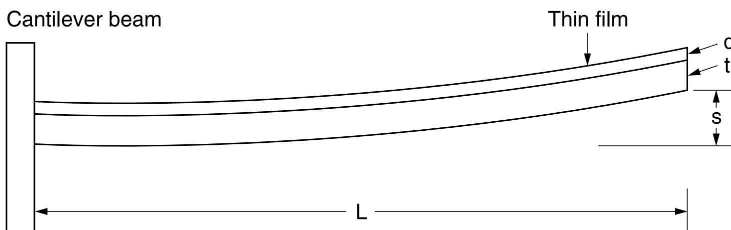

Figure 2.17 Cantilever beam used to measure film stress.

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Table 2.3a Substrates: Value of $E/(1-\nu)$

Material	$E/(1-\nu)$ (10^{12} dyne/cm^2)
Si (100)	1.805[a]
Si (111)	2.290[a]
Ge (100)	1.420[a]
Ge (111)	1.837[a]
GaAs (100)	1.239[a]
GaAs (111)	1.741[a]
Fused quartz	0.854[b]
Bulk silica	0.88[c]
Thermal oxide	0.90[c]

[a] Brantley, W.A., *J. Appl. Phys.*, 44, 534, 1973.
[b] *Handbook of Tables for Applied Engineering Science*, p. 138.
[c] Quoted in Carlotti et al. (1996).

Table 2.3b Oxides: Value of $E/(1-\nu)$

Oxide	$E(1-\nu)$ (10^{11} dyne/cm^2)	Source/Technique
CVD high rate	10	Sunami et al. (1970)
CVD low rate	7.5	Two substrates
PSG; $P_2O_5/SiO_2 = 0.04$	9.8	
BSG; $B_2O_3/SiO_2 = 0.29$	16	
Thermally grown	4.7	Flitch et al. (1989c)/IR
PECVD (N_2O/SiH_4); annealed	10 ± 1	Ambree et al. (1993)/two substrates
PECVD (N_2O/SiH_4); annealed	3 ± 1	Ambree et al. (1993)/IR
LPCVD	8.7 ± 0.5	Bouchard et al. (1993)
PECVD	8 ± 3	Two substrates
LPCVD PSG (4 wt% P)	7 ± 1	
PECVD PSG (4 wt% P)	9 ± 2	
LPCVD BPSG (4 wt% P, 3 wt% B)	4 ± 1	
PECVD BPSG (4 wt% P, 3 wt% B)	6 ± 2	
PECVD	8.0	Doucet and Carlotti (1995)
APCVD	7.1	Brillouin scattering
PECVD PSG	7.4	
APCVD BPSG	7.1	
Siloxane SOG; annealed	1.9	
PECVD (SiH_4)	8.0	Carlotti et al. (1996)
PECVD (TEOS)	8.5	Brillouin scattering
ECR	8.0	
Si-rich	7.7	
PSG	7.4	
Thermally grown	9.0	

The curvature has been measured by many methods, e.g., a light-section microscope (Glang et al., 1965), Newton's rings (Irene, 1976), an optically levered laser technique (Sinha et al., 1978), and a visible light reflection method (Kobeda and Irene, 1986). Meng et al. (1993) measured the intrinsic stress of AlN during sputter deposition onto silicon substrates in an UHV chamber using a scanning laser beam reflection method. Many investigators now use the commercially available automated laser probe systems (e.g., Flexus, Santa Clara, CA). Three-dimensional stress maps, outputs of multiple scans in a stress measurement system, are valuable for visualizing stress nonuniformities not apparent

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in individual scans (Blech and Robles, 1994). Automated stress measurements are an option with surface profilers made by, for example, Veeco/Dektak (Santa Barbara, CA).

The radius of curvature of a single-crystal substrate (usually a silicon wafer) on which a thin film has been deposited can also be measured by x-ray techniques. Both one- and two-crystal measurements have been used (Hearn, 1977). The one-crystal technique is the faster and simpler one but is less sensitive by an order of magnitude. In the two-crystal measurement (Goldsmith et al., 1983), a pair of unstrained crystals is aligned to obtain, in transmission, Bragg diffraction from a set of planes. The crystals can be translated with no change in the x-ray intensity since the Bragg angle is constant across the crystals. A thin film is deposited on one of the crystals; this results in curvature due to the stress it generates. The crystals are again aligned to obtain Bragg diffraction. However, now translation results in the decrease of the x-ray intensity because of the curvature. The Bragg angle θ must be adjusted during translation to maintain maximum intensity. This adjustment, $\Delta\theta$, is used to measure the radius of curvature of the crystal, R:

$$R = L/\Delta\theta$$

where L is the scan length.

Flinn (1989) has reviewed the principles and application of wafer curvature techniques for stress measurements in thin films.

2.9.3.2.3 Deflection Technique

Stress can also be determined by measuring the deflection δ of a circular disk at a distance r from the center of the disk, before and after deposition using, for example, a noncontact fiber optic probe (Schaible and Glang, 1969), a Mikrokater thickness gauge (Choi and Hearn, 1984), and a wafer deflection (stress) gauge (Chen and Fatemi, 1986). In this case the stress is given by

$$\sigma = [\delta/r^2][E_s/3(1-\nu)][t_s^2/t_f]$$

The assumptions for all these measurements are: $t_s >> t_f$, the substrate is linearly elastic, homogenous, uniformly thick, and thin compared to its radius, and the deflection small compared to the wafer thickness. It is also assumed that there is excellent adhesion between film and substrate.

2.9.3.2.4 Other Methods

X-ray diffraction techniques have been used to determine the stress in a thin film by measuring the strain in a single-crystal substrate induced by the deposition of a film upon it; the strain produces a change in the lattice parameters. For measurements made perpendicular to the film plane, the stress is computed from (Hoffman, 1966):

$$\sigma = (E/2\nu)(a_o - a/a_o)$$

where a_o and a are the lattice constants of the bulk and the strained crystal. In the film plane

$$\delta = [E/(1-\nu)](a - a_o)/a_o$$

Polycrystalline x-ray techniques have also been used for stress analysis of metal films, deposited on thermally oxidized silicon, by measuring the d-spacing of a single reflection for several orientations of a sample. The slope of d vs. $\sin^2 \psi$ (ψ = tilt angle) determines the stress (Shute et al., 1989). Further discussion of these and other x-ray techniques can be found elsewhere (e.g., Norton, 1968; Flinn and Waychunas, 1988; Vreeland et al. 1989).

A number of specialized stress measuring techniques have been devised. For example, Ku et al. (1991) monitored the stress as W was sputtered onto x-ray mask membranes, by measuring the resonant frequency of the membrane. The membrane was driven to vibrate using a sine wave applied to a concentric ring underneath the membrane. The oscillations were detected by a fiber-optic

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sensor. Wu et al. (1994) described a microstress measuring apparatus based on polarized phase shifting and image processing which gives the stress distribution and surface deformation on an entire region, in a small region, and in any direction on a wafer. They report the minimum stress measured to be of the order of 10^6 dyne/cm^2.

2.9.3.2.5 Temperature Dependence

Stress is temperature dependent. In the absence of any chemical or structural changes in a film, the stress at any temperature σ_t is given by (Sunami et al., 1970)

$$\sigma_t = \sigma_d + (T_t - T_d)[E_f/(1 - \nu_f)](\alpha_s \alpha_f)$$

where σ_d is the film stress at the deposition temperature (intrinsic stress), α_s and α_f are the average values of the CTE of the substrate and film between temperatures T_d and T_t (since they are temperature dependent), and E_f and ν_f are Young's modulus and Poisson's ratio for the film. This stress, due to the thermal mismatch between film and substrate, can result in cracking or loss of adhesion of the film when it is subjected to heat treatment.

The change of stress with temperature is

$$\mathrm{d}\sigma/\mathrm{d}T = [E_f/(1 - \nu_f)](\alpha_s - \alpha_f)$$

The relative magnitudes of α_s and α_f can be determined from the sign of dσ/dT (Smolinsky and Wendling, 1985), but the absolute value of α_f, however, can be obtained only when $E_f/(1 - \nu_f)$ is known. This, as well as the value for α_f, can be accomplished by determining stress vs. temperature, i.e., dσ/dT, for films deposited on two different substrates. This is discussed in Section 10.2.

2.9.4 Measurement of Young's Modulus (*E*)

A knowledge of Poisson's ratio of the thin film is required to calculate Young's modulus from the experimental data obtained from most commonly used methods. Poisson's ratio is a positive number, <0.5; it usually lies between ~0.2 and 0.4 and a value for ν in that range will often be assumed in calculating E. Since there can be an order of magnitude reduction in E when significant porosity is introduced into a film, the exact value of ν is not critical.

2.9.4.1 Nanoindentation

A commercially available indenter is the nanoindenter (Nano Instruments, Inc.). The indenter is a triangular pyramid-shaped diamond (Berkovich indenter), its position determined by a capacitance displacement gauge. A controlled force drives the indenter toward the sample. The forces and the displacement associated with the indenting process are measured (Doerner and Nix, 1986; Oliver and Pharr, 1992). The surface, during indentation (loading) and after unloading, is shown in Figure 2.18a and a typical result of load (P) vs. displacement (h) in Figure 2.18b.

The initial slope of the unloading curve dP/dh (S) is used for determining the modulus. Assuming the indenter has ideal pyramidal geometry

$$\mathrm{d}P/\mathrm{d}h = (2/\pi)^{1/2} h_p E_r$$

where $h_{plastic}$ (or h_p), the plastic depth, is the depth of the indenter in contact with the sample under load and is determined by the extrapolation to zero load of the tangent to the unloading curve at maximum load, S (see Figure 2.18b). E_r is defined as

$$1/E_r = (1 - \nu^2)/E + (1 - \nu_o^2)/E_o$$

where ν is Poisson's ratio and E is Young's modulus for the film and ν_o and E_o the values for the indenter.

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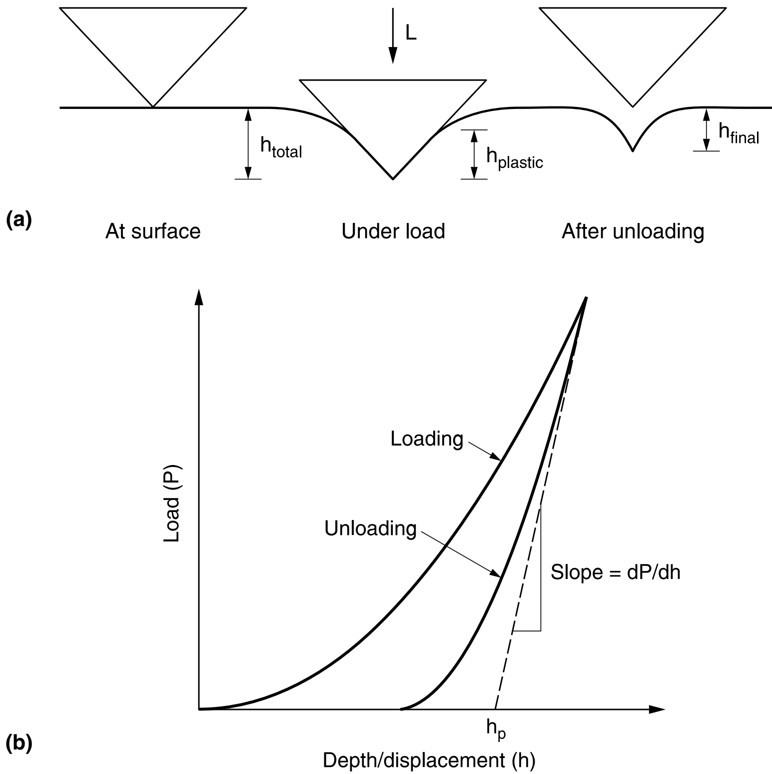

Figure 2.18 (a) Schematic of loading/unloading during indentation. (Reproduced from Doerner, M.F. and W.D. Nix, *J. Mater. Res.*, 1, 601, 1986. With permission.) (b) Load (P) vs. indenter displacement (h). (Adapted from Doerner, M.F. and W.D. Nix, *J. Mater. Res.*, 1, 601, 1986 and Oliver, W.C. and G.M. Pharr, *J. Mater. Res.*, 7, 1564, 1992.)

Another method uses the projected area of contact at peak load (A) (see Figure 2.19) (Oliver and Pharr, 1992; Malzbender et al., 2002):

$$E_r = (\pi^{1/2}/2)S_{max}/A^{1/2}$$

For the case of a perfectly sharp Berkovich indenter, $A = 24.5h_p^2$ (Malzbender et al., 2002). Doerner and Nix point out that "it is not necessary to know ν with great precision to obtain a good value for of E."

2.9.4.2 Surface Acoustic Waves (SAW)

SAW measurements can be used to extract the value of E (as well as the density) by using the measured value of the thickness and the known (or assumed) value of ν.

SAW are generated thermoelastically when a laser pulse is focused into a line shape on a surface. The absorbed heat energy generates broadband wave packets propagating along the surface; these are detected by a piezoelectric transducer pressed into the surface (Kuschnereit et al., 1995; Schneider et al., 1997; Flannery et al., 2001; Flannery, 2001; Flannery and Baklanov 2001; Murray et al., 2002). The dispersion of the waves is measured as a function of frequency as they travel through the film and substrate.

A typical SAW wave packet is shown in Figure 2.20a. A Fourier transform technique allows the extraction of the frequency-dependent velocity dispersion curve. The dispersion curves for silica aerogel films on Si of different thicknesses are shown in Figure 2.20b. Four variables affect the

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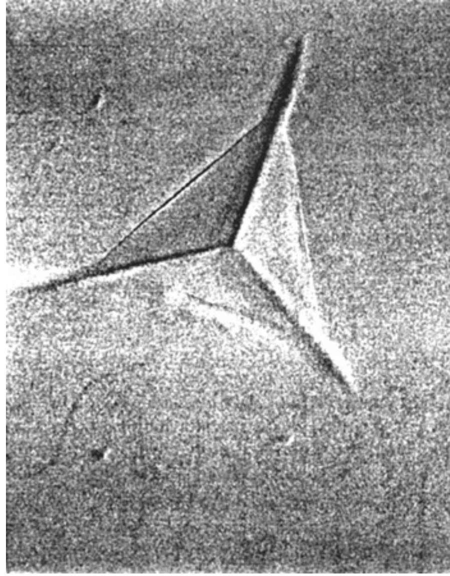

Figure 2.19 SEM image of the imprint of a pyramidal indenter.

dispersion: thickness of the film *t*, Poisson's ratio ν, the average film density ρ, and *E*. The two variables ρ and E were fitted to the curve shape and the values were extracted from the best fit. The thickness can be measured easily and a constant value of $\nu = 0.2$ was assumed (the results are insensitive to ν). The values for ρ and *E* correlated with the measured dielectric constants, decreasing as the dielectric constant decreased. Porosity values of 60 to 70% were derived by assuming a density of 2.27 g/cm^3 for thermally grown SiO_2. The values of *E* were very low (~1 to 2 GPa). Since $E = E_o(\rho/\rho_o)^m$, these measurements imply a value of $m > 4$, higher than usually measured (3 to 4) (Flannery et al., 2001; Flannery, 2001).

2.9.4.3 Ellipsometric Porosimetry (EP)

This method does not require a knowledge of ν. For a description of the technique, see Section 2.21.

According to Mogilnikov and Baklanov (2002): "Change of the film thickness due to microscopic capillary pressure is an elastic response to capillary forces that depend on the value of *E* of the porous film." The method is not applicable if the film swelling is due to chemical interaction with the adsorbate.

The change in film thickness as the relative pressure (P/P_o) is varied during desorption of a liquid from the pores of a nanoporous film, as shown in Figure 2.21. Fitting the data to the equation $d - d_o = -k\ln P/P_o$ (the solid line in the range between P/P_o corresponding to the minimum thickness and $P/P_o = 1$) the value of *k* can be calculated and used in the equation

$$E = d_o RT/kV_L$$

to determine *E*, knowing V_L, the molecular volume of the condensed liquid.

Note that Flannery and Baklanov (2002) and (Mogilnikov and Baklanov (2002) compared the values of *E* for nanoporous films determined by nanoindentation vs. SAW, Brillouin light scattering, and EP. They found that *E* was higher when measured by indentation. They proposed several reasons why indentation overestimated *E*: stiffening by the substrate, viscoelasticity, and tip–film interaction.

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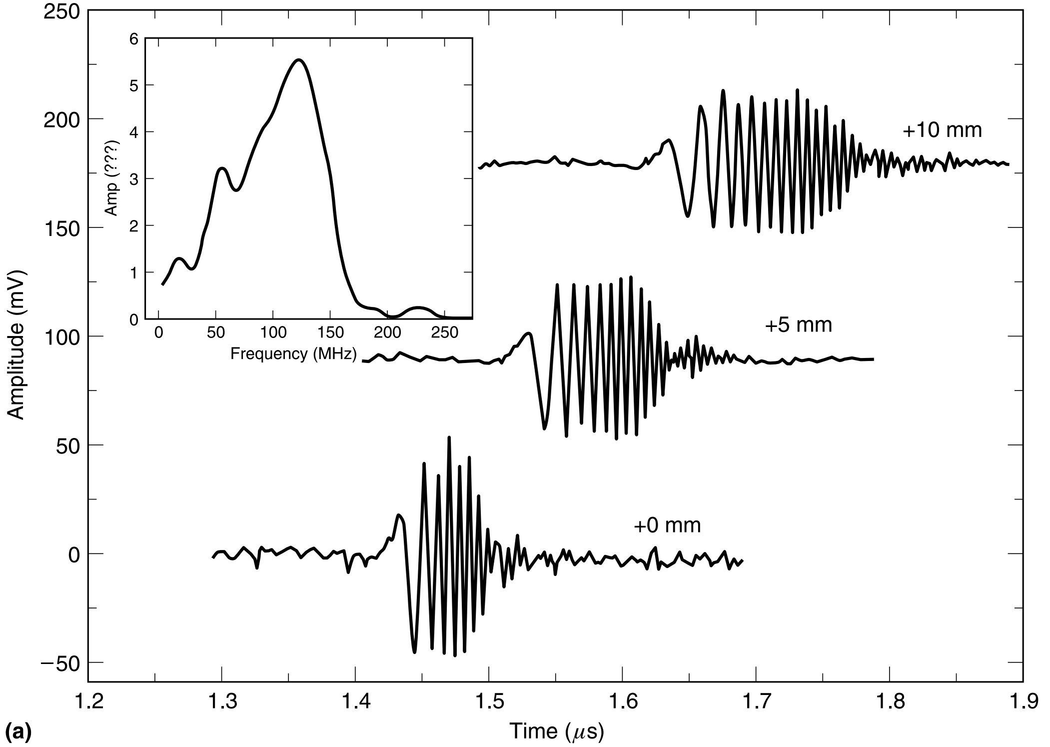

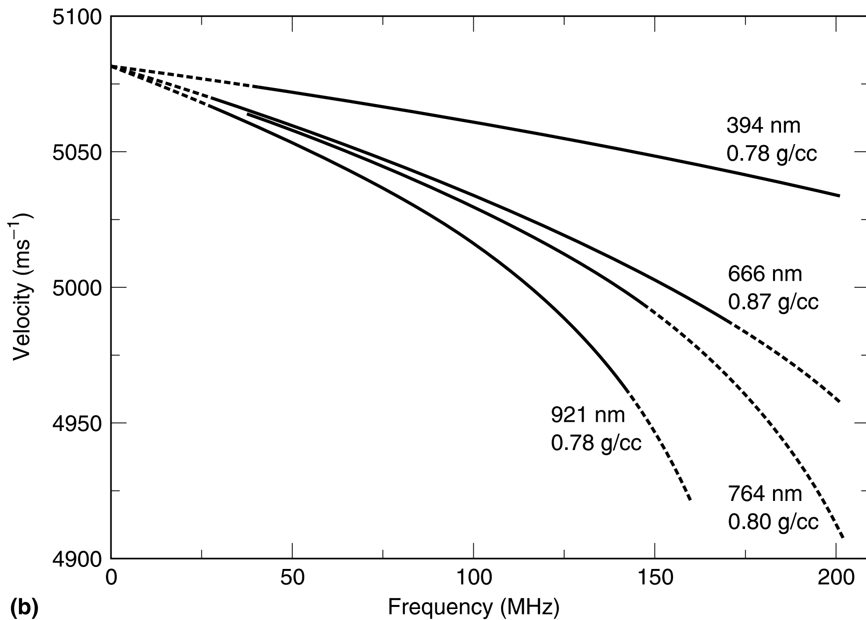

Figure 2.20 (a) SAW wave packets detected at different relative propagation distances on an aerogel layer deposited on Si. Inset: Fourier transform of the wave packet. (b) Dispersion curves calculated from SAW wave packets for different layer thicknesses. (Reprinted from Flannery, C.M., C. Murray, I. Streiter, and S.E. Schulz, *Thin Solid Films*, 388, 1, 2001. With permission. Copyright 2001, Elsevier.)

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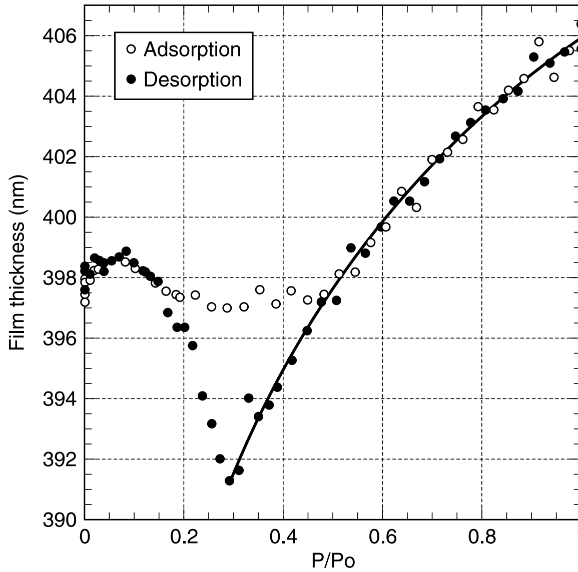

Figure 2.21 Change of film thickness during adsorption and desorption of toluene by a porous low-ε film. Change of film thickness fitted by $d = d_o - k\ln P/P_o$. (From Mogilnikov, K.P. and M.R. Baklanov, *Electrochem. Solid State Lett.*, 5, F29, 2002. With permission of the Elecrochemical Society, Inc.)

2.9.5 Poisson's Ratio (ν)

Poisson's ratio was determined by a combination of experimental measurements and finite element analysis (FEA). The experiments consisted of measuring, by the bending beam method, the stress as a function of temperature of blanket thin films, to determine $E/(1 - \nu)$ (Section 2.10.2), and of a film patterned into a high-aspect-ratio periodic line structure (thickness = 1.2 μm and AR = 3.2, similar to that in microelectronic devices). The FEA calculation was performed on the line samples. It used $E/(1 - \nu)$ as an input parameter and calculated the stress along the line direction under thermal load for different assumed values of ν keeping $E/(1 - \nu)$ constant. The experimentally measured stress–temperature data of the line samples were then used to determine ν. The value of ν for TEOS-based PECVD SiO_2 was 0.24, so that $E = 59$ GPa (Zhao et al., 1999).

A novel technique was proposed to estimate ν directly using the same stress–temperature measurements on the same kinds of samples discussed above. The blanket film was characterized by a two-dimensional biaxial stress state (2D) and the patterned structure by a uniaxial stress state (1D):

$$k_{2D} = ds_{2D}/dT = E_f/1 - \nu_f(\alpha_s - \alpha_f)$$

$$k_{1D} = ds_{1D}/dT = E_f(\alpha_s - \alpha_f)$$

Therefore

$$\nu_f = 1 - k_{1D}/k_{2D}$$

The value of ν of the TEOS-based oxide film was estimated to be 0.23 ($E = 60$ GPa). This compares favorably with the more accurately obtained value of $\nu = 0.24$ (Zhao et al., 2000).

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2.9.6 Method for Measuring Both *E* and ν

2.9.6.1 Brillouin Light Scattering (BLS)

BLS is light scattering by acoustic phonons. Polarized light is focused onto the surface of a film and the backscattered light collected. The spectra of the scattered light are used to determine the elastic constants (c_{11} and c_{44}) from which both the elastic constant E and Poisson's ratio ν can be derived (Doucet and Carlotti, 1995; Carlotti al., 1996).

2.9.7 Measurement of Biaxial Modulus

2.9.7.1 Temperature Dependence of Stress

This is described in Section 2.10.2.

2.9.7.2 Bulge Test

In this technique (Xu et al., 2000) a window of a thin film is formed by etching a square hole in the Si substrate backing the film and the deflection of the membrane δ under a differential pressure P is measured. The stress σ and strain τ at the center of the membrane can be calculated:

$$\sigma = Pa^2/C_3 t\delta$$

$$\tau = C_4\delta^2/a^2$$

where t = film thickness and $C_3 = 3.04$ and $C_4 = 0.451$ for square membranes. The slope of σ vs. τ is $E/(1-\nu)$.

2.9.7.3 BLS

Doucet and Carlotti (1995) and Carlotti et al. (1996) calculated $E/(1-\nu)$ from the values of E and ν measured independently by BLS. Their result for thermally grown SiO_2 was in excellent agreement with that for bulk silica.

Table 2.3b lists the value of $E/(1-\nu)$ for several oxide films. The CVD and PECVD films studied have not been described completely by the various investigators; they may differ in their preparation methods and their properties, e.g., dopant concentration, silanol content, etc., may vary. Thus, differences among the results may be attributed to differences among the films as well as to the method of measurement.

2.9.7.4 IR Spectroscopy (for SiO_2)

The assumption on which this method was based is that the Si–Si distance provides an *atomic* parameter for the strain and that stress relaxation occurs through changes of the Si–O–Si bond angle. The center frequency of the Si–O bond stretching vibration provides a measure of that angle (Flitch, 1989a). The strain obtained from IR spectra is relative to a relaxed oxide, and is calculated from the shifts in the IR bond stretching frequency due to stress in the film (Nakamura et al., 1986; Flitch et al., 1989a,b,c; Ambree et al., 1993). The strain parameter τ is given by $(f-f_r)/f_r$, where f is the measured IR frequency of the Si–O bond in the stressed oxide and f_r the frequency for the relaxed oxide, 1078.5 cm^{-1}. The stress σ was measured by the standard method. Thus $E/(1-\nu)$ could be determined from σ vs. τ (Flitch et al., 1989a,b,c). Carlotti et al. (1996) pointed out that "this method is a probe of the local SiO_2 structure and is well adapted for thermally grown oxide but not for CVD oxides which contain various chemical bonds." Nevertheless, for thermally grown

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oxide, the value measured by IR (Flitch et al, 1989a) was significantly lower than that for silica, which it should resemble quite closely. Correcting for the thermal mismatch between Si and SiO_2 resulted in a somewhat better agreement (Flitch et al., 1989b); they stated that the discrepancy could be explained by the fact that modulus values reported for thin films are typically low by ~50% compared with bulk values (Flitch et al., 1989a).

2.9.8 Hardness (*H*)

Hardness is usually measured using a nanoindenter and measuring the image of the indentation (Figure 2.19). It is calculated by dividing the projected area of contact between the indenter and sample A by the maximum applied load P_{max}, i.e., $H = P_{max}/A$.

The value of H can also be obtained without imaging the indentation but by measuring the plastic depth under load h_p. Knowing the indenter geometry, the projected area can be obtained.

2.10 THERMAL PROPERTIES

2.10.1 Introduction

The thermal coefficient of expansion (TCE), thermal conductivity, and thermal stability are the properties of interest.

2.10.2 Coefficient of Thermal Expansion (TCE or α_f)

As mentioned in Section 2.9.3.2, differences in the TCE of a film and its substrate result in thermal stresses during processing and/or use and this may affect the yield of the process and the reliability of the structure. The value of TCE for a thin film may differ from that for the bulk material.

The value of TCE (and $E_f/(1-\nu)$ can be determined conveniently by measuring the temperature dependence of stress of a film deposited on different substrates whose properties are known. For films deposited on two different substrates

$$(\mathrm{d}\sigma/\mathrm{d}T)_1 = (\alpha_{s1} - \alpha_f)[E_f/(1-\nu_f)]$$

$$(\mathrm{d}\sigma/\mathrm{d}T)_2 = (\alpha_{s2} - \alpha_f)[E_f/(1-\nu_f)]$$

$$\alpha_f = (\mathrm{d}\sigma/\mathrm{d}T)_2(\alpha s_1) - (\mathrm{d}\sigma/\mathrm{d}T)_1(\alpha_{s2})/(\mathrm{d}\sigma/\mathrm{d}T)_2 - (\mathrm{d}\sigma/\mathrm{d}T)_1$$

and

$$E_f/(1-\nu_f) = (\mathrm{d}\sigma/\mathrm{d}T)_2 - (\mathrm{d}\sigma/\mathrm{d}T)_1/(\alpha_{s2}) - (\alpha s_1)$$

Since $(\mathrm{d}\delta/\mathrm{d}T)_1$, $(\mathrm{d}\delta/\mathrm{d}T)_2$ were measured and α_{s1} and α_{s2} are known, α_f and $E_f/(1-\nu)$ can be obtained.

Several substrate pairs have been used: Sunami et al. (1970) and Bouchard et al. (1993) used Si and quartz; Blaauw (1983), Ambree et al. (1993), and Zhao et al. (1999) used Si and GaAs; Retajczyk and Sinha (1980) used Si and sapphire; Zhao et al. (2000) used Si and Ge.

The TCE of bulk samples has been determined by measuring the lattice expansion during heating by x-ray diffraction and the out-of-plane value by SRX (Section 2.18). The values of TCE for many materials used in semiconductor devices are known and are available in various handbooks; a comparison of some materials is given in Figure 2.22 (Brown, 1970).

Burkhardt and Marvel (1969) measured the TCE of a freely suspended sputtered silicon nitride film over a wide temperature range using a cathetometer to measure the distance between two incised marks.

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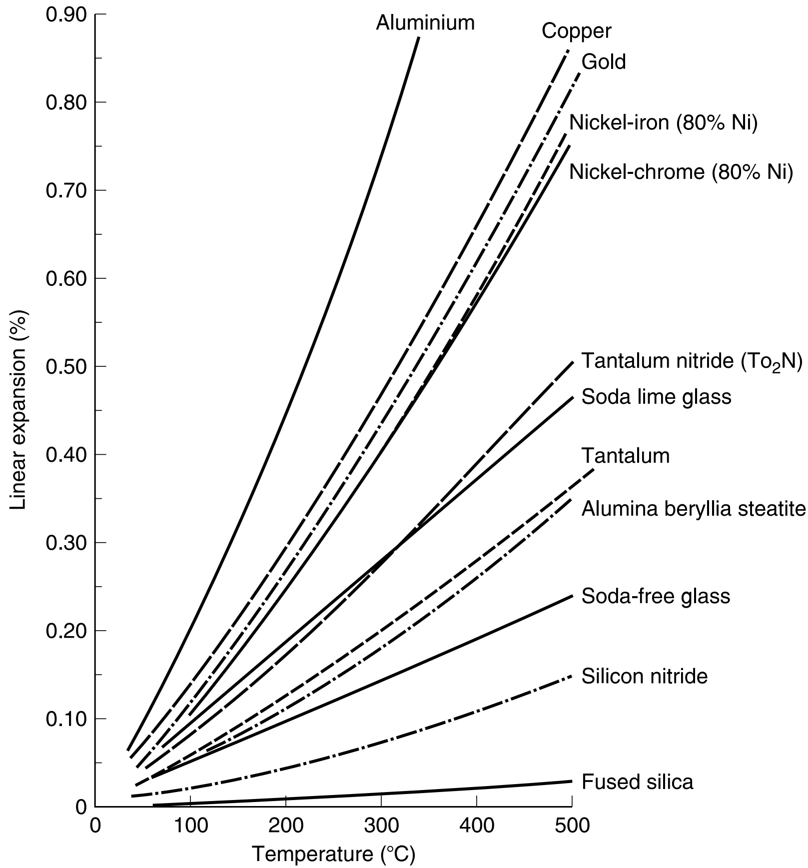

Figure 2.22 Linear expansion as a function of temperature for various materials. (From Brown, R., in *Handbook of Thin Film Technology*, Maissel, L.I. and Glang, R., Eds., McGraw-Hill, New York, 1970, chap. 6. Reproduced with permission. Copyright 1970, McGraw-Hill.)

2.10.2.1 Thermal Mismatch Stress

The thermal mismatch stress is determined by the value of α_f relative to that of the substrate. There is an appreciable mismatch between Si and SiO_2 ($\alpha_{SiO2} < \alpha_{Si}$) so that the stress becomes more tensile as the films are heated. Silicon nitride (CVD and PECVD) is a better thermal match to Si than is the oxide.

By following the changes in stress while increasing and then decreasing the temperature, any hysteresis can be detected. When hysteresis occurs it indicates changes in the composition or structure of the film (e.g., Ramkumar et al., 1993).

Systems, e.g., Flexus, are available commercially in which stress can be measured, in a controlled ambient, as the temperature is cycled. Other work has reported on the stress variations during thermal cycling: e.g., Shimbo and Matsuo (1983), Bhushan et al. (1990), Wu and Rosler (1992).

2.10.3 Thermal Conductivity

The thermal conductivity of metals is high, that of insulators is low. Figure 2.23 (Brown, 1970) illustrates these differences.

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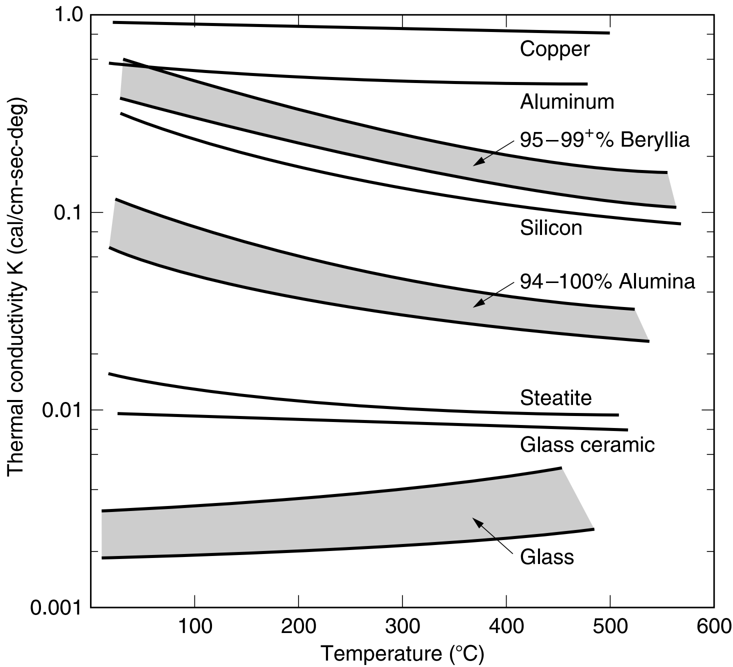

Figure 2.23 Thermal conductivities of various materials as a function of temperature. (From Brown, R., in *Handbook of Thin Film Technology*, Maissel, L.I. and Glang, R., Eds., McGraw-Hill, New York, 1970, chap. 6. Reproduced with permission. Copyright 1970, McGraw-Hill.)

The poor thermal conductivity of insulators is, therefore, a concern since the heat generated by the devices and by the I^2R losses of the metal interconnections during device operation must be dissipated through the insulator. The newer dielectric materials are even poorer heat conductors, which can give rise to hot spots. In reality, the interaction between the interconnection metal and the insulator as well as the removal of heat at the outer surfaces by, for example, metal pins, paste, etc., must be considered in the temperature rise calculation.

2.10.3.1 Measurement: Insulators

2.10.3.1.1 DC Method

Jin et al. (1996) measured the thermal conductivity of low-ε films using a test structure designed for electromigration testing; Figure 2.24a shows a cross section of the metal (with and without a dielectric overcoat). The metal lead was isolated. Heat was generated along it by passage of a current and flowed through the surrounding dielectric materials to the substrate. The efficiency of heat removal from the metal measured their thermal conductivity. Figure 2.24b shows the thermal conduction structure. Measurements of T1–T3 and simulations using a commercial RAPHAEL simulator based on a 2D model allowed the extraction of the thermal conductivity. The thermal conductivity of PECVD SiO_2 was measured as 11.5 and PI as 2.4 and HSQ as 3.7 mW/(cm °C).

2.10.3.1.2 3ω Method

Cahill and Pohl (1987) and Cahill (1990) developed this method; it eliminates blackbody radiation errors at room temperature. In addition, very small samples can be used and the measurements

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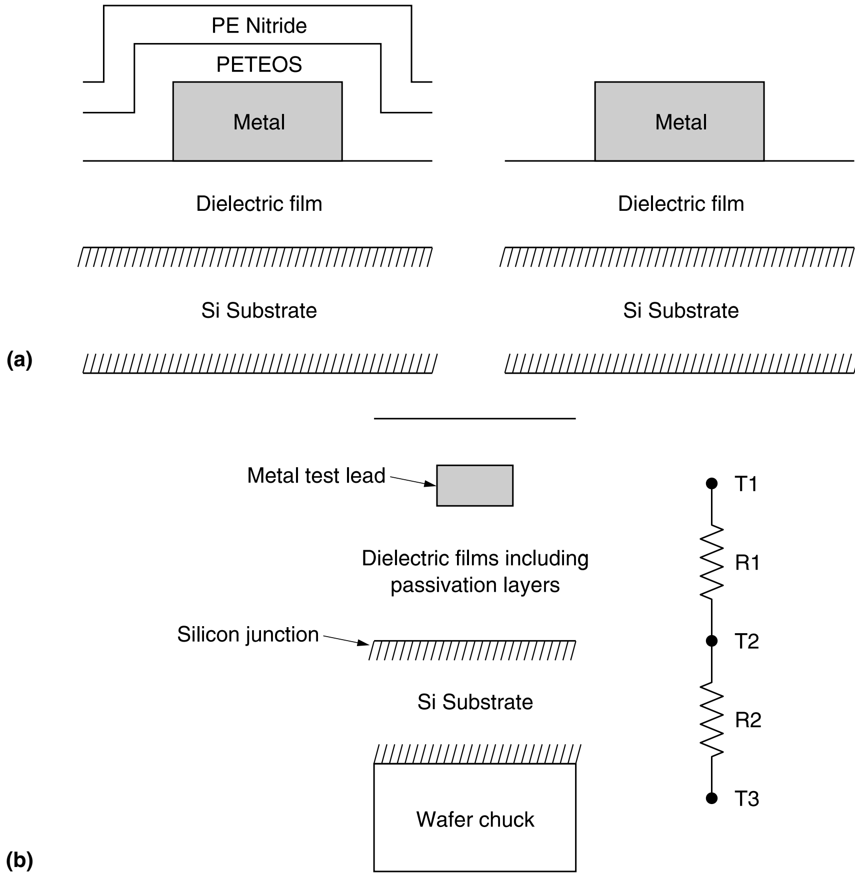

Figure 2.24 (a) Cross-section of test structure used for thermal conductivity measurements of dielectric films. Left: with passivation layers; right: without passivation layers to study thermal conduction contribution of dielectric materials from top and sidewalls of metal structure. (b) Thermal conduction structure diagram. (From Jin, C., L. Ting, K. Taylor, T. Seha, and J.D. Luttmer, DUMIC, 1996. With permission.)

made in a short time. The test structure consists of a thin metal film evaporated onto the surface of the test sample and formed into a thin line with appropriate leads. A single element is used as heater and thermometer.

A current of frequency ω is used; it produces Joule heating at a frequency of 2ω. The resistance oscillation at 2ω multiplied by the excitation current at ω produces the voltage oscillation at 3ω, which is measured at two frequencies, f_1 and f_2. The thermal conductivity Λ is given by

$$\Lambda = [V^3 \ln f_2/f_1/4\pi l R^2 (V_{3,1} - V_{3,2}] \mathrm{d}R/\mathrm{d}T$$

where $V_{3,1}$ is the in-phase 3ω voltage at frequency f_1 and $V_{3,2}$ is the in-phase 3ω voltage at frequency f_2, R is the average resistance of the metal line, V is the voltage across the metal line at ω, and l is the line length.

Cahill and Pohl (1987) compared the thermal conductivities of films of a polymer (PMMA) and of an SiO_2 film: $\Lambda_{SiO2} = 12.3$ and $\Lambda_{PMMA} = 2.0$ mW/(cm K).

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2.10.4 Thermal Stability

2.10.4.1 Organic Films

The thermal stability of organic materials, the temperature above which the film degrades or decomposes, is one of the most important factors in determining the usefulness of such films as interlevel insulators. Thermal stability is measured using thermogravimetric analysis (TGA) in which the weight loss is monitored as the sample is heated at a constant rate in an inert ambient. Figure 2.25a shows a TGA curve. A significant weight loss occurs above 450°C with catastrophic loss above 500°C. However, as shown in Figure 2.25b, if the sample is held at 450°C for extended times, there is insignificant weight loss.

Chemical and physical transformations in organic films are often detected by the following techniques.

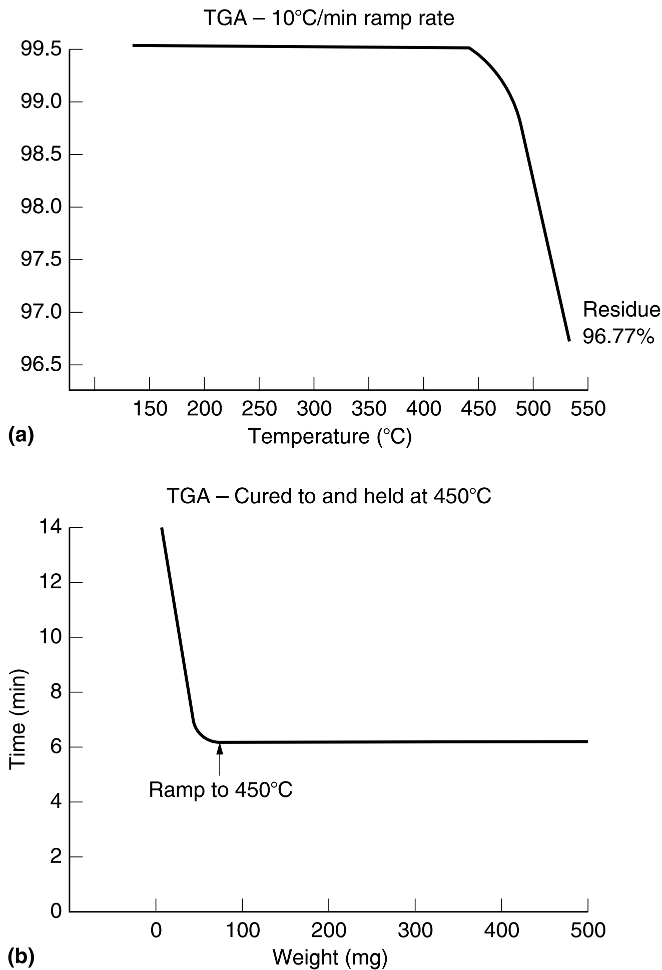

Figure 2.25 Thermal gravimetric analyses (TGAs) of PI: (a) % weight loss vs. temperature (10°C/min ramp rate); (b) isothermal weight loss at elevated temperature (450°C).

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In differential thermal analysis (DTA), the difference in temperature ΔT between a sample and a reference with the same characteristics is observed while both are being heated or cooled simultaneously. This technique should be able to detect any phenomenon that is accompanied by a change in enthalpy (heat content), i.e., ΔH. Polymerization, degree of cure, oxidation, cross-linking, polymer–polymer reactions, and thermal degradation are some of the factors studied by DTA.

Differential scanning calorimetry (DSC) is used in order to determine calorimetric data directly. In DSC, the temperatures of a sample and a reference are maintained at a fixed temperature as the temperature is changed; the variation in power required to maintain this equality in temperature during a transition is measured (Carroll, 1972). Carroll discusses these techniques in detail and demonstrates how to extract the information required from the experimental data.

Among the other techniques mentioned by Carroll are thermodilatometric analysis (TDA) in which the sample length is monitored during heating or cooling and is useful for determining the glass transition temperature, and thermal volatilization analysis (TVA) used to study degradation of a polymer to volatile products by pressure measurements.

2.11 AUGER ELECTRON SPECTROSCOPY (AES)

2.11.1 Introduction

This is a surface analytical technique which can detect all elements heavier than He and is suitable for the analysis of very small areas.

2.11.2 Principles

When an energetic beam of electrons or photons irradiates a surface it dislodges an inner shell (core) electron. After the vacancy is created, an electron from an outer shell can replace the ejected electron (deexcitation) and a second characteristic electron, the Auger electron is ejected:

$$e^- + M \rightarrow M^{++} + e^-_{Auger}$$

The kinetic energy of this electron is characteristic of the element. Although an electron beam (~1 to 10 keV) is usually used for excitation, the energy of the Auger electron is independent of the way the initial vacancy was created. The process of Auger emission is shown schematically in Figure 2.26.

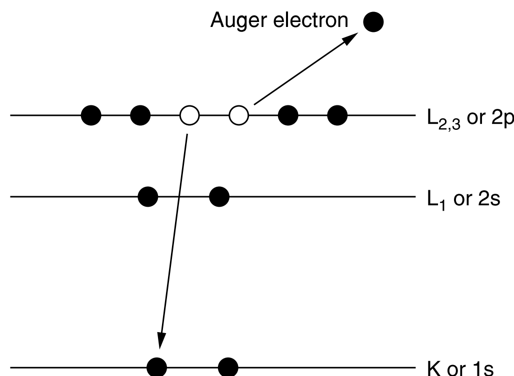

Figure 2.26 Schematic of Auger (AES) deexcitation processes.

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2.11.3 The Auger Spectrum

The Auger spectrum is a plot of the number of electrons emitted *N* (proportional to atomic concentration) vs. kinetic energy *E*, but is usually plotted as a derivative spectrum, d*N* vs. *E*, to facilitate the identification of the Auger electron peaks and suppress the background of the inelastically scattered electrons from the primary beam. The derivative spectrum is produced by modulating the energy selected by the analyzer and using a lock-in amplifier to detect the signal (Bindell, 1988); the difference between the two is shown in Figure 2.27. More recently, due to improvements in instrumentation, *N* vs. *E* spectra have become satisfactory.

The Auger peaks due to the various elemental constituents of a film can be used for compositional analysis. There is also some contribution from the chemical state of the element since changes in the valence electrons influence the binding energy of the core electrons. Therefore the exact energy peak position and/or its shape may provide some chemical information; in general the interpretation is difficult. XPS (discussed below) is preferable for determining chemical shifts. Nevertheless, there has been some success is using AES for this purpose. For example, Madden (1981) analyzed the shape of the Si derivative signal from a thin film of PECVD silicon nitride and concluded that Si–Si, Si–H, and Si–N bonds were present. Wildman and Schwartz (1982), in a study of interfacial resistivity, determined the thickness of the surface oxide on Al from the ratio of the chemically shifted Auger peaks of Al(III) (Al_2O_3) to Al(0) (metal), a method first described by Chang and Boulin (1977). They used the information to calibrate the area under the oxygen curve in the depth profile in terms of thickness. In this way, the thickness of thinner-than-air-grown oxides coated *in vacuo* by an Al film to prevent further oxidation could be determined by Auger profiling. High-resolution spectra showing this chemical shift are shown in Figure 2.28. In

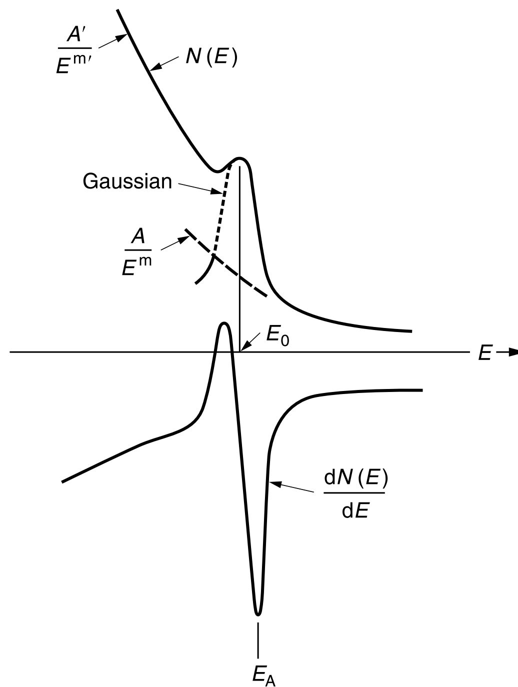

Figure 2.27 Hypothetical AES spectrum, $N(E)$, containing a continuous background, A/E^m, a Gaussian peak and a low-energy step of form $A'/E^{m'}$. The energy of the most negative excursion of the derivative corresponds to the steepest slope of $N(E)$.

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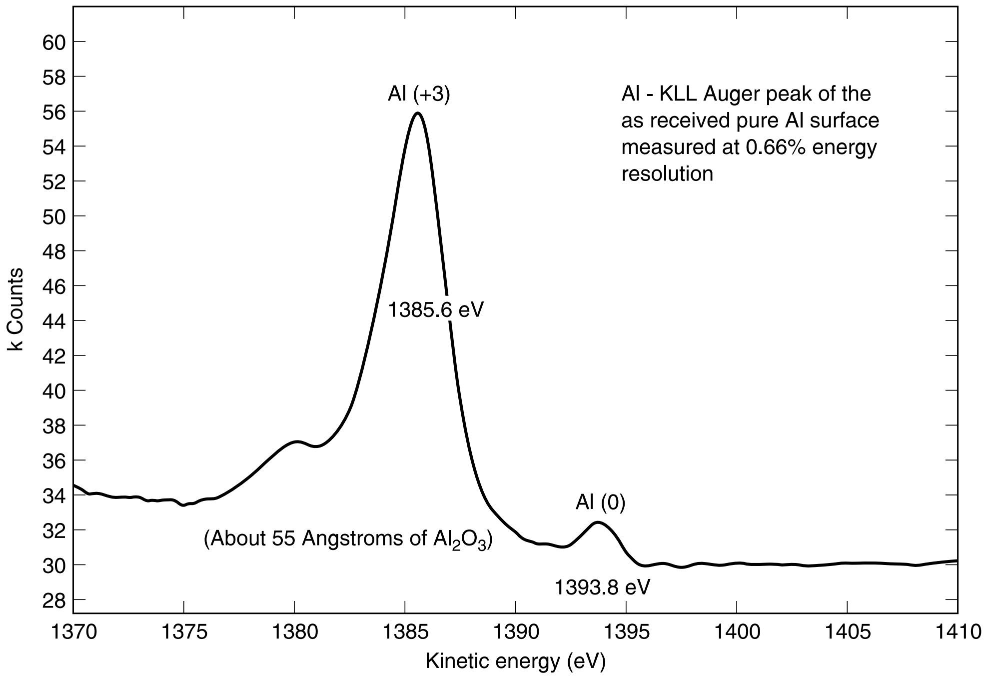

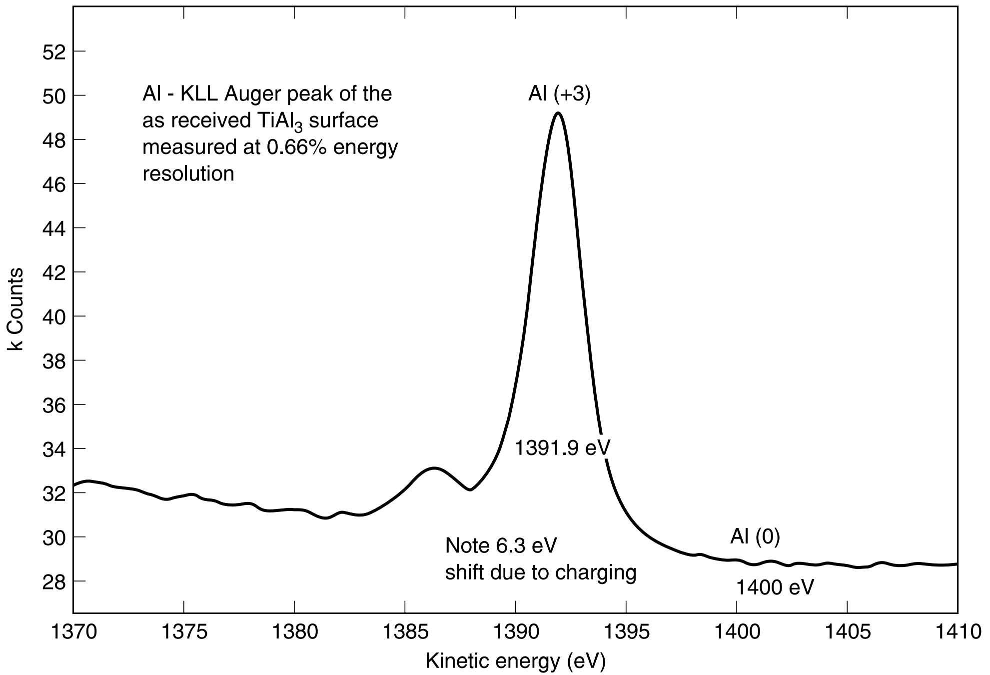

Figure 2.28 High-resolution AES spectra of contaminated surfaces. Top: Al; bottom: $AlTi_3$. (From H.S. Wildman, IBM Analytical Services. With permission.)

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the top spectrum both peaks are evident, and the estimate of the Al_2O_3 thickness is given. In the bottom spectrum the Al(0) peak has disappeared indicating that the surface oxide is very thick; the shift in the peak position due to charging is also apparent. Although the electron beam can penetrate into the film, only the Auger electrons produced in the top 10 to 30 Å of the film contribute to the signal. This depth is called the escape depth and is the region from which electrons are ejected without loss of energy.

2.11.4 Applications

One of the applications of AES is shown in Figure 2.29. The top spectrum is of an Al surface and the bottom of a $TiAl_3$ surface; Figure 2.29a shows the spectra of the surfaces as received (contaminated) and Figure 2.29b the spectra after a brief sputter cleaning. The distortion due to charging is evident at the low-energy part of the spectrum of Figure 2.29a. Also seen are the plasmon loss peaks in the spectrum of the cleaned $AlTi_3$ surface; they are more prominent in the metallic state and their absence indicates the presence of an oxide.

An ion gun is usually an integral part of the apparatus so that compositional variations within a film can be detected and measured by alternating sputtering and probing the surface to produce a depth profile; this is usually plotted as the atomic % of an element vs. sputter etch time. However, during ion milling, an originally sharp interface becomes broadened due to surface roughness, ion-induced topography, angle of incidence effects, cascade mixing (knock-on), and ion-induced diffusion, as illustrated in Figure 2.30. Preferential sputtering and surface segregation are effects that must also be considered.

Despite the problems mentioned above, depth profiles are widely used and provide valuable information. Figure 2.31 shows depth profiles for the Al and $AlTi_3$ samples of Figure 2.29a.

If the sputter etch rate is known accurately, the sputter time can be converted into depth. It should be noted that the depth scale in Figure 2.31 is given as the sputter equivalent of angstroms of SiO_2; since Al_2O_3 sputters more slowly than SiO_2, the thickness of the oxide layer is overestimated. However, the thickness comparison between the two samples is valid, i.e., there is significantly more oxide on the surface of the $AlTi_3$ sample than on that of the Al sample.

In addition, since the sputter etch rate depends on the composition of the film, in general it is not a trivial conversion from sputter time to thickness. It is possible to ion mill a known standard to obtain an approximate time vs. depth scale for a given compound.

The sensitivity of AES depends on the relative Auger electron efficiencies of the various elements, the primary beam energy and current, the equipment, and the inelastic electron background. Thompson et al. (1985) give the approximate sensitivity of AES as 10^{-10} g/cm^2 for the surface layer and the atomic fraction in the bulk as 10^{-3}.

The conversion of the number of electrons emitted is complicated by the influence of the matrix on the backscattered electrons and escape depth. External standards are usually used; if the composition of the standard is close to that of the test sample, the elemental composition can be determined directly from the ratio of the Auger yields (Feldman and Mayer, 1986). The measured surface concentrations may not be identical to those in the bulk, however.

Additional advantages of AES are: the ability to monitor several elements at once, high sensitivity, particularly to low-mass impurities such as oxygen or carbon (common contaminants of surfaces and interfaces), rapid data collection, easily focused to small spots with the possibility of scanning AES (SAM) to produce maps of the surface composition, the ability to vary beam energy to operate under optimum conditions, and commercially available equipment (e.g., Perkin-Elmer, JEOL). Disadvantages include: surface degradation, stimulated desorption, charging of insulator surfaces by the electron beam (mentioned above), and the difficulty of quantitative analysis and interpretation of the Auger chemical shift. In addition, the equipment is expensive (Thompson et al., 1985).

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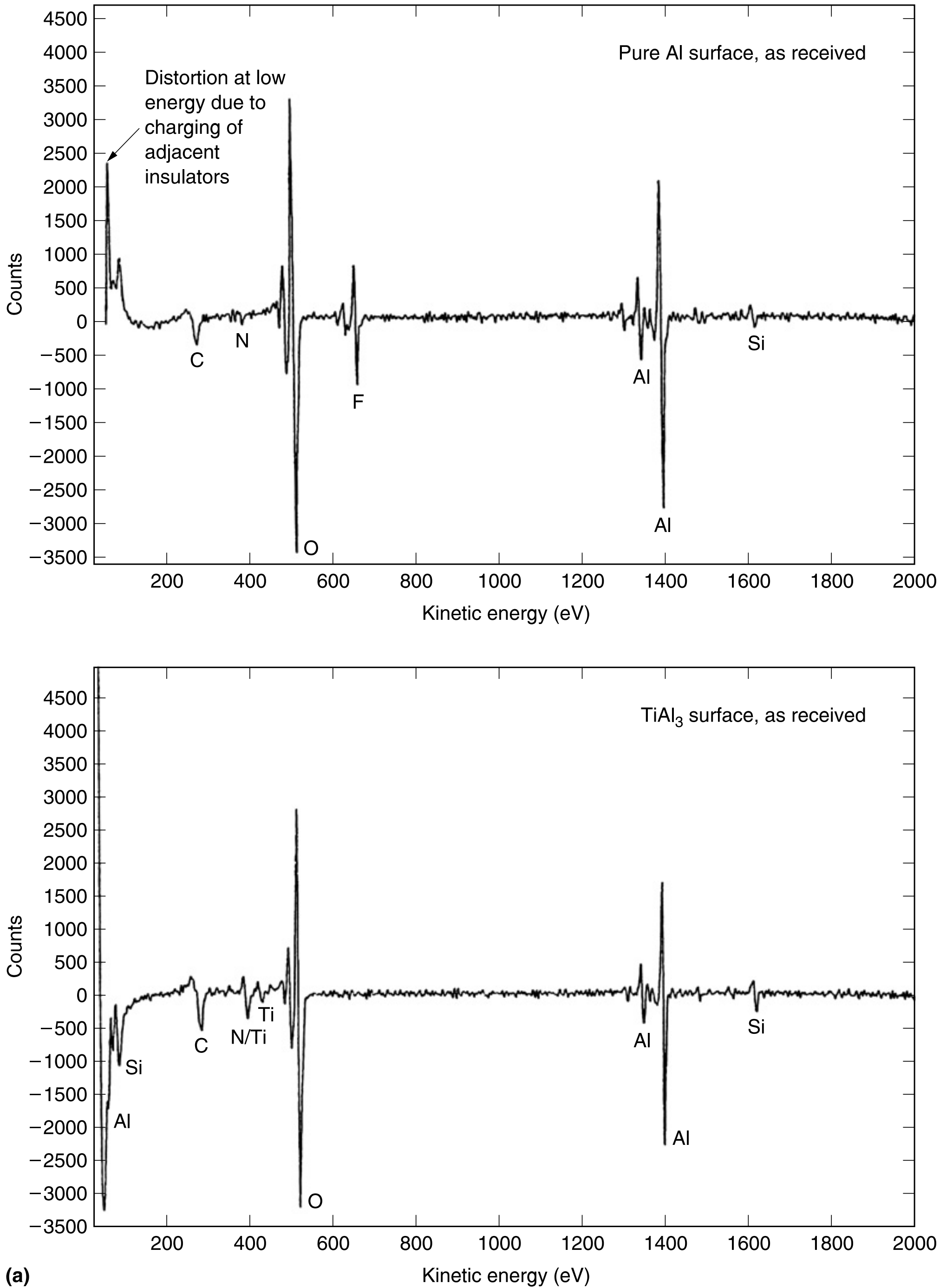

Figure 2.29 AES spectra of Al (upper) and $TiAl_3$ (lower) surfaces: (a) as received, i.e., contaminated, and (b) after sputter cleaning. (From H.S. Wildman, IBM Analytical Services. With permission.)

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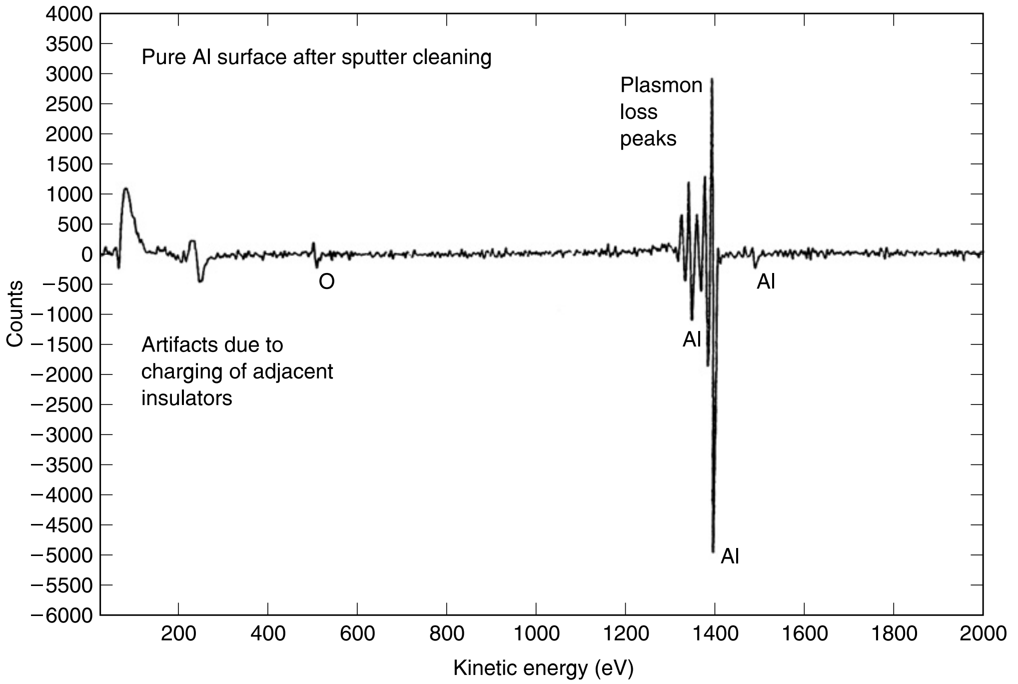

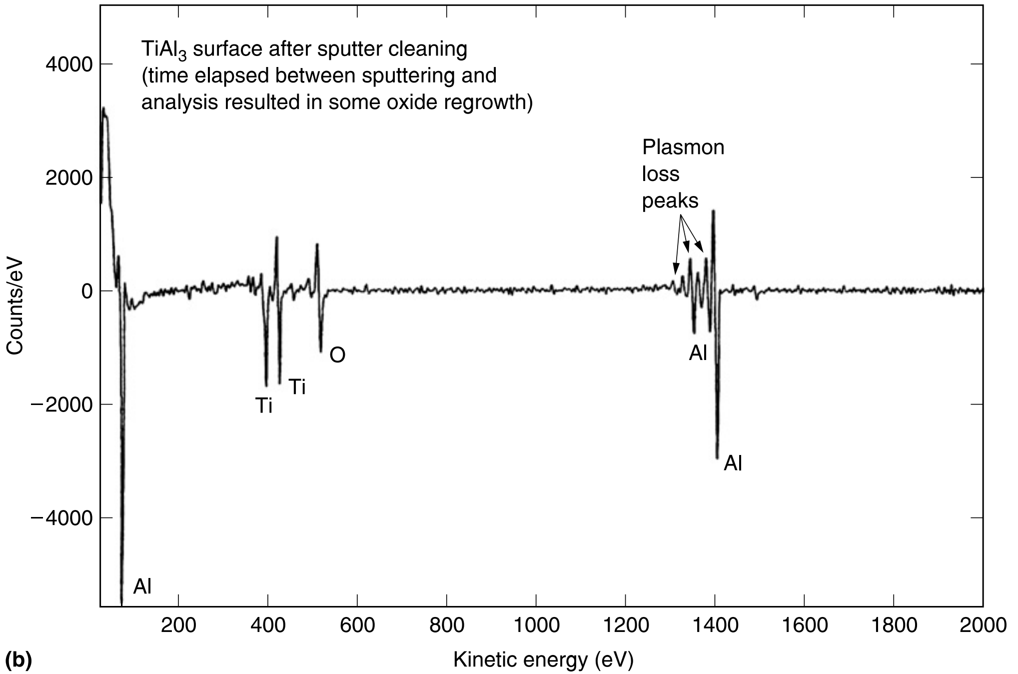

(b)

Figure 2.29 (Continued)

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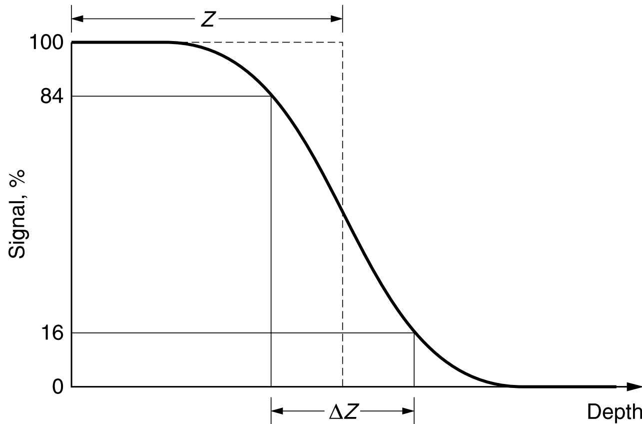

Figure 2.30 Depth resolution in sputter-depth profiling; true profile indicated by dashed line. ΔZ corresponds to depth separation between points on the profile corresponding to 84% and 16% of layer intensity.

2.12 X-RAY PHOTOELECTRON SPECTROSCOPY (XPS); ALSO CALLED ELECTRON SPECTROSCOPY FOR CHEMICAL ANALYSIS (ESCA)

2.12.1 Introduction

This is another surface analytical technique, analogous to AES in that a flux of energy results in the ejection of electrons, of characteristic energy, from within a small escape depth.

2.12.2 Principles

In XPS, also called electron spectroscopy for chemical analysis (ESCA) a beam of low-energy x-rays (often the K-α line of Al, 1.487 keV) is used to probe the sample surface. All the photon energy is absorbed and interacts with the inner shell electrons, causing photoemission of an electron. The electronic transition involved in XPS is shown in Figure 2.32.

From the measured kinetic energy of the emitted electron E_{kin}, its binding energy E_{B} can be calculated from the known photon energy $h\nu$ and the difference in work function between the sample and the spectrometer $\Delta\phi$:

$$E_{\text{kin}} = h\nu - E_{\text{B}} - \Delta\phi$$

2.12.3 XPS Spectrum

An XPS spectrum is the plot of the number of electrons detected (proportional to the relative abundance of the species) vs. binding energy. Superimposed on the XPS spectrum are Auger transitions, as illustrated in Figure 2.33a, which shows the XPS spectrum of Cu.

The exact binding energy for an electron in a given element depends on the chemical environment of that element because the configuration of the valence electrons (due to chemical interaction) will influence the lower lying (core) electrons, changing their binding energies (Feldman and Mayer, 1986). Thus both the element and the type of bonding in the surface constituents can be determined If several valence states of the element are present, they can be distinguished from each other. For example, as shown in Figure 2.33b, the silicon peak from silicon bonded to oxygen is shifted in energy from that in elemental silicon and the relative proportions of each can be determined.

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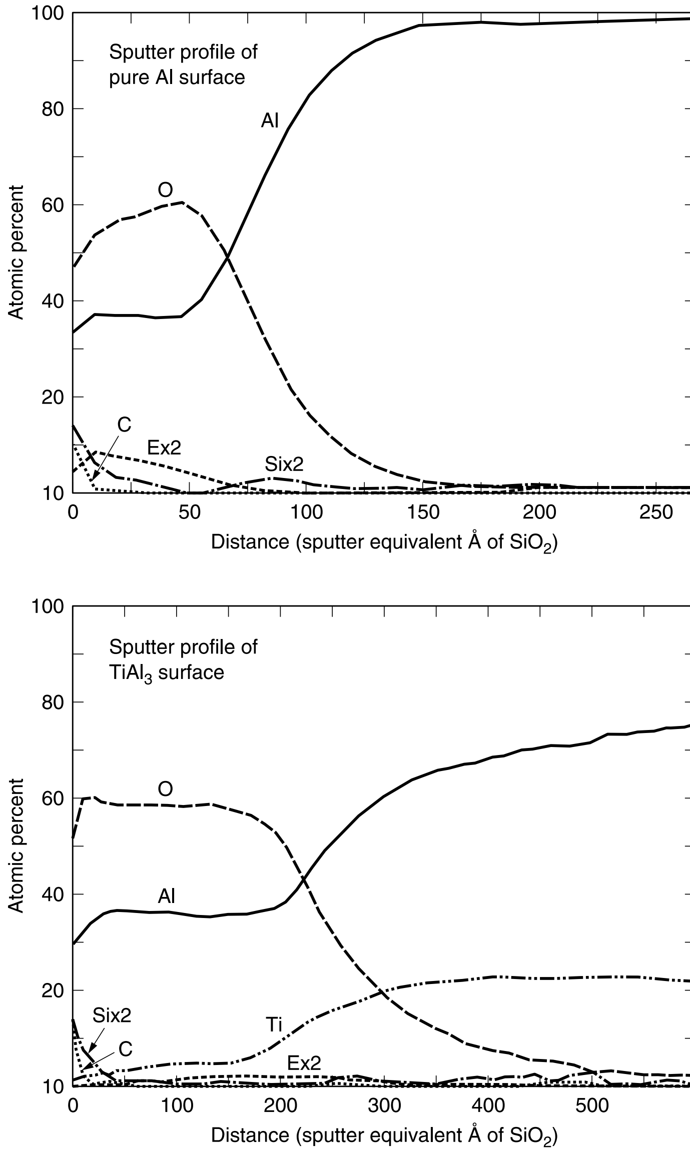

Figure 2.31 AES depth profiles of the samples of Figure 2.29a: Al (upper), $AlTi_3$ (lower). (H.S. Wildman, IBM Analytical Services.)

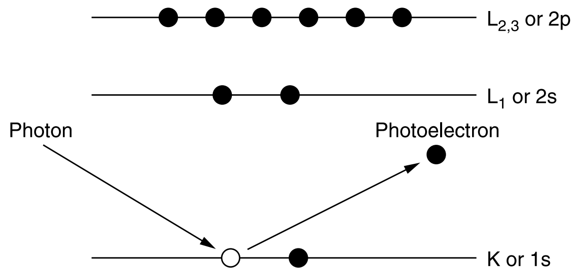

Figure 2.32 Electronic transition involved in XPS.

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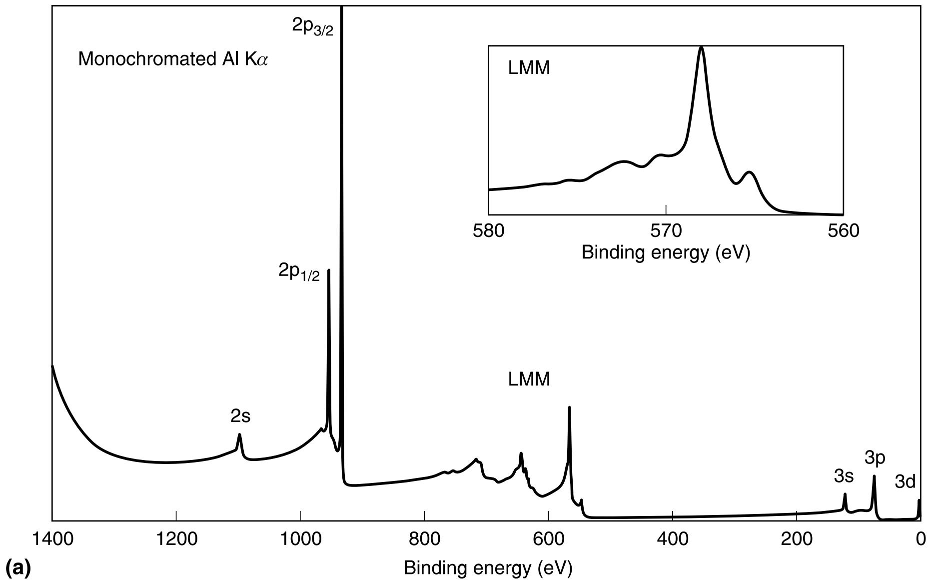

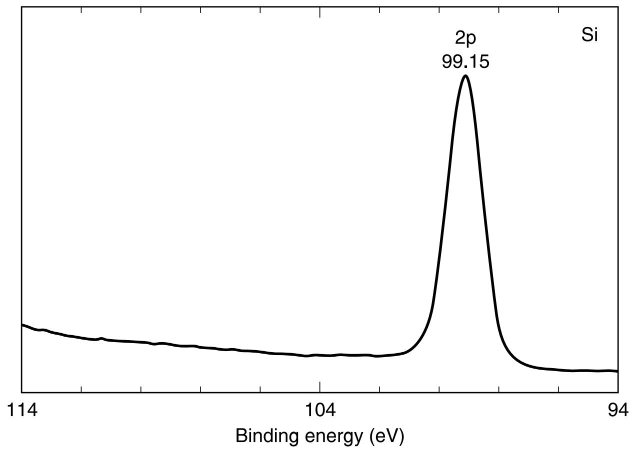

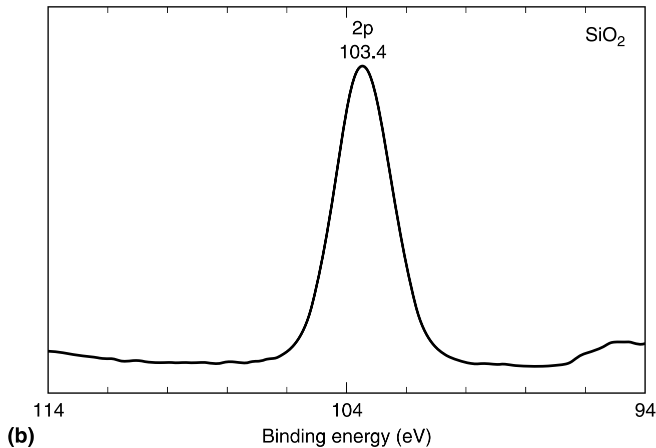

Figure 2.33 (a) XPS spectrum of Cu. (b) Chemical shift in binding energy of the Si 2p line: elemental Si (top), Si in SiO_2 (bottom).

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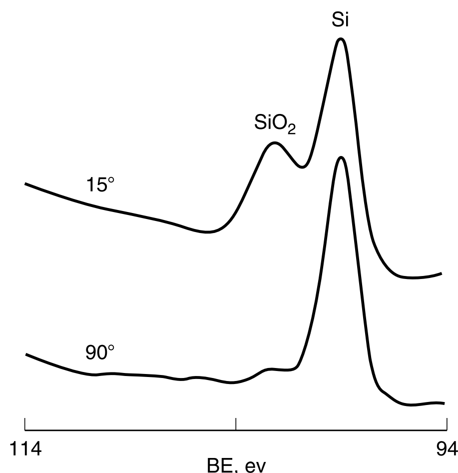

Figure 2.34 Increase in sensitivity obtained by changing the angle of the XPS detector with respect to the sample.

2.12.4 Applications

XPS is used extensively to detect and measure surface compounds or adsorbates and their alteration due to chemical and physical processes, e.g., oxidation of a metallic surface, removal of surface contaminants, etc. It has also been used to study the interfacial reactions during the deposition of metals on polyimide (Ho et al., 1985). Depth profiling by alternating ion milling and surface probing is an option, as it is for AES (with the same concerns about interface broadening, etc.).

Angle-resolved XPS, i.e., reducing the angle of the detector relative to the surface of the sample, increases the surface sensitivity. This is illustrated in Figure 2.34, which shows the XPS spectrum of a Si sample with a coating of approximately one monolayer of SiO_2.

Changing the electron emission angle varies the effective electron escape depth and thus makes possible depth profiling which is nondestructive and yields an absolute depth scale in terms of the escape depth. The technique is restricted to very thin layers, about three times the escape depth (about 50 Å). Changing the kinetic energy of the emitted electrons by varying the energy of the photon source also varies the escape depth and thus is an alternative method of depth profiling (Hoffman, 1966).

XPS has been used to analyze patterned samples as well as flat surfaces. The topography of a periodic structure together with angle-resolved XPS was used to cause geometrical shadowing for selective area analysis after RIE using the parameters of selective etching of SiO_2 over Si (Oehrlein et al., 1988). Matsuura et al. (1991) used XPS analysis of the sidewalls of polysilicon features etched in Cl_2 and Cl_2/N_2 plasmas to clarify the nature of sidewall protection. The photoelectrons were collected both parallel and perpendicular to the etched periodic structures.

The principle advantage to XPS is its ability to provide chemical bonding information. As in AES, neither hydrogen nor helium can be detected. There is less surface damage from the x-rays than from an electron beam and there are no charging effects; however, the spatial resolution is inferior to that of AES and scanning is not feasible. It is not a very sensitive technique; detection limits are about 0.1 to 1.0 at%.

A good reference for a more complete coverage of AES and XPS is Briggs and Seah (1990).

2.12.5 Ultraviolet Photoelectron Spectroscopy (UPS)

This is a technique related to XPS, but of no use for elemental analysis. In UPS the electrons are excited from the valence band by photons of much lower energy, e.g., 20 to 40 eV. However,

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Ho et al. (1985) used UPS to observe the valence states which are directly involved in bond formation at the interface between metals and polyimide.

2.13 SECONDARY ION MASS SPECTROSCOPY (SIMS)

2.13.1 Introduction

This is the most sensitive of the analytical techniques; and is used frequently to determine the very low concentrations and depth profiles of dopants and/or contaminants found in semiconductor devices, as well as of more abundant species. It can be used to detect and measure *all* elements. It is capable of high lateral resolution, and has excellent mass discrimination.

2.13.2 Description

In SIMS, a focused beam of ions is used to bombard the surface and sputter it; excited neutral species and singly or multiply charged ions (positive or negative) are emitted. The secondary ions are detected and counted using an energy filter and a mass spectrometer; an electron multiplier increases the sensitivity. O^{2+} is the primary ion used most commonly for electronegative ions, Cs^+ for the negative ones. The relative abundance of the sputtered species indicates the composition of the layer being removed. If there is preferential sputtering, the surface concentration is rearranged so that the total yield gives the bulk composition. However, analysis of the surface layer at this point would not represent the bulk composition. The detection limit has been quoted as 10^{14} to 10^{17}/cm^3 depending on the element; the sensitivity is greater for the lighter elements (Bindell, 1988). The use of electron neutralizing beams has made possible the analysis of insulators. The influence of sputtering effects on the depth profile is the same as in AES and XPS, i.e., broadening of the interface, ion mixing, etc. For this reason, primary ions of the lowest possible energy are used; altering the incident ion angles can also improve the depth resolution. A schematic of the apparatus is shown in Figure 2.35. To ensure that ions from the walls of the crater being formed during the sputtering process are excluded, the instrument is designed to detect only those from the central portion of the crater, as illustrated in the lower part of Figure 2.35.

The secondary ion yields vary widely from element to element. They are also sensitive to matrix effects which influence the yield of secondary ions. For example, the secondary ion yield from Si could vary over three orders of magnitude depending on the oxygen concentration (Feldman and Mayer, 1986). Thus the ion yield may not allow accurate determination of the relative concentration of the species in the film. Ion implanted samples are used as standards for analysis.

When the conditions are adjusted so that the sputtering rate is very slow, the process has been called static SIMS (SSIMS).

In contrast to AES and XPS, SIMS is capable of analyzing for and profiling hydrogen (Lundquist et al., 1982). There are, however, problems with detection of trace amounts. Magee and Botnick (1981) enumerated them and discussed ways of overcoming them so that H could be detected in Si at <50 ppm atomic.

2.13.3 Related Methods

2.13.3.1 Secondary Neutral Mass Spectrometry (SNMS)

In this technique sputtered neutrals are used for compositional analysis. This avoids some matrix effects. The sensitivity of SNMS and SIMS for detecting low concentrations of impurities is

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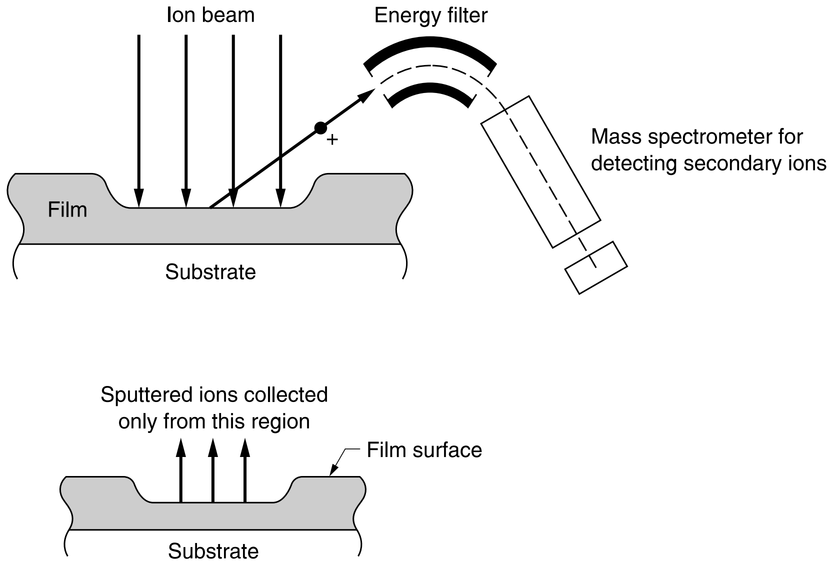

Figure 2.35 Top: schematic of SIMS apparatus showing raster of beam, signal detection from the center of the sweep, and the crater formed during sputtering in the SIMS apparatus. Bottom: the signal is collected from the center of the crater.

about the same (detection limit ~1 ppm). In SNMS, the properties of the substrate should not affect the yield substantially (Feldman and Mayer, 1986).

2.13.3.2 Laser Ionization Mass Spectrometry (LIMS)/Laser Microprobe Mass Analysis (LMMA)

Another related technique is laser ionization mass spectrometry (LIMS) or laser microprobe mass analysis (LMMA) in which a high-energy, finely focused laser pulse volatilizes and ionizes the region of interest. A time-of-flight mass spectrometer is used to identify the ions based the mass-to-charge ratio. Molecular species can also be analyzed by reducing the laser power so that the species are desorbed without decomposition (Singer, 1986).

2.14 ELECTRON MICROPROBE

This technique is used for elemental analysis.

2.14.1 Basis of Method

Analysis by the electron microprobe is based on the detection and measurement of the characteristic x-rays produced when a material is excited by energetic electrons. Since the electron beam can be finely focused, the technique is capable of small-area analysis (~1 μm); the sampling depth is of the same order so that x-rays generated in the substrate may interfere if films less than ~1 μm thick are probed.

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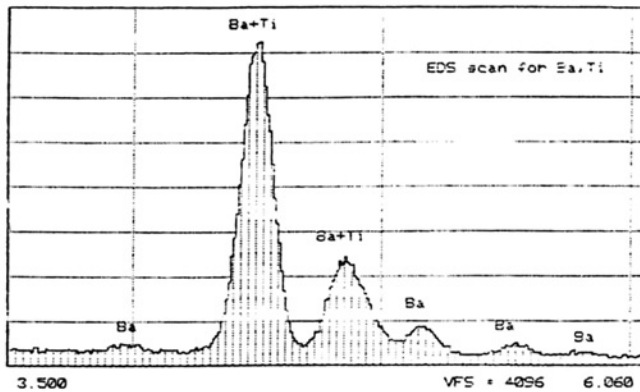
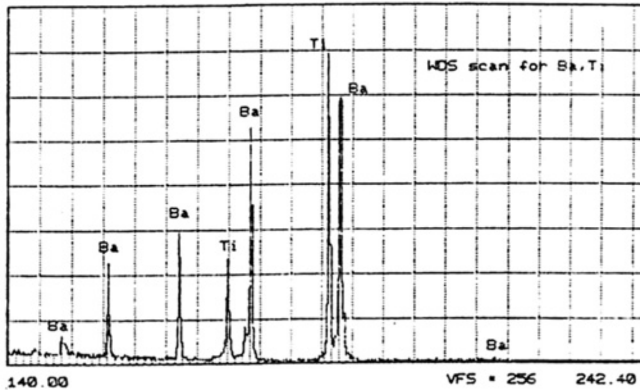
2.14.2 Modes of Operation

There are two modes of operation depending on the type of detector used: energy dispersive (EDS/EDX) or wavelength dispersive (WDS). For EDS a Si(Li) detector, protected by a beryllium window, and kept at liquid nitrogen temperature, is used. Thus only elements of $Z > 11$ can be detected. However, the radiation from all the elements in the sample is detected simultaneously. WDS involves x-ray diffraction from an analyzer crystal. The resolution and range of element detection ($Z \geq 4$) are better than in EDS, but the elements are detected sequentially, increasing the data collection time. Figure 2.36 compares the results from the two modes of operation. According to Smith and Hinson (1986) the detectability limit is 50 to 1000 ppm, and the accuracy is ~5%, with suitable standards. Figure 2.37 shows a microprobe line scan (i.e., a plot of concentration of each element in the sample vs. its position in the sampler). This capability is a feature in some probes.

The analysis may be carried out either in a stand-alone system or in a scanning electron microscope (SEM) equipped with the proper detectors.



(a)



(b)

Figure 2.36 Micropobe analyses of a benitoite (a mineral used as a standard): (a) energy-dispersive x-ray spectrum; (b) wavelength-dispersive x-ray spectrum. (From Falcon, IBM Analytical Services. With permission.)

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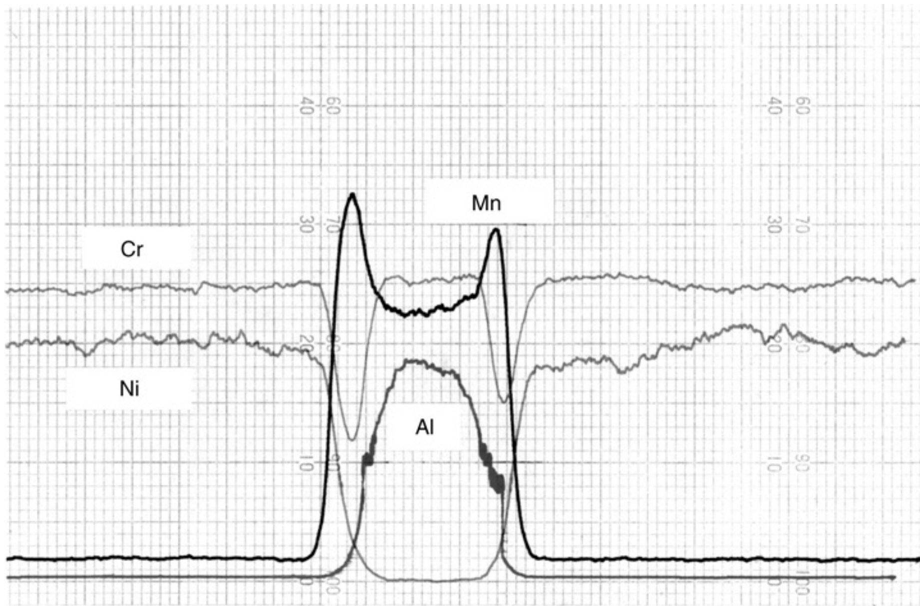

Figure 2.37 Microprobe scan line (about 15 μm across) of a precipitate in stainless steel. (From Falcon, IBM Analytical Services. With permission.)

2.15 X-RAY FLUORESCENCE SPECTROMETRY (XRFS)

2.15.1 Introduction

XRFS is a method of elemental analysis in which identification is made by measuring the wavelength or energy of characteristic x-rays emitted from the atoms in a sample. The lowest atomic number element that can be measured by this technique is carbon (fair sensitivity) and even boron (greater than a few percent). The x-rays can be excited by electron irradiation, but this is an inefficient process with most of the energy converted into heat. There is the potential for vaporizing or melting the samples. It is preferable, therefore, to use primary x-rays to excite the secondary characteristic x-ray spectrum.

2.15.2 Spectrometers

Wavelength-dispersive spectrometers, most commonly employed, use the diffracting property of a single crystal to separate the polychromatic beam emitted by the specimen. Energy-dispersive spectrometers use a Si(Li) detector to give a spectrum of voltage pulses directly proportional to the spectrum of x-ray photon energies emitted; a multichannel analyzer collects and records the pulses according to their energies. XRF instruments of both kinds are available commercially.

There are several specialized instruments: total reflection XRF (TRXFR) for measuring trace components, synchrotron source XRF (SSXRF) for high resolution, and the proton excited XRF (PIXE) whose great sensitivity shortens analysis time and is used for trace elements (Jenkins, 1988).

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2.15.3 Measurement of Concentration

XRFS is very valuable for its ability to detect/identify and measure low concentrations of elements. Standardization is required and the specific procedures used depend on whether a single or multiple element sample is being analyzed. For the measurement of Ar in sputtered SiO_2, one standardization method was measuring the Kα and Clα of a KCl film of known thickness, since K and Cl bracket Ar, to infer the argon mass/argon Kα net counts (Lloyd, 1969). Background and matrix effects must be taken into account for any quantitative analysis. Solid samples can be analyzed directly, powders are fused, and solutions are usually concentrated before analysis. There has been an attempt to use an intensity concentration algorithm instead of standardization procedures but it does not appear to be used widely.

2.15.4 Applications

Examples of the use of XRF are the measurement of the P-concentration in PSG and BPSG films (Grilletto, 1977; Levy et al., 1985; Madden et al., 1989), the argon content of sputtered SiO_2 films (Lloyd, 1969; Hoffmeister and Zuegel, 1969; Schwartz and Jones, 1970), the composition of alloys such as permalloy and AlCu, and the detection of trace contaminants. It was also used to analyze the deposit at points across a substrate to determine the relationship between the distribution of material on the substrate and the region of the multicomponent target from which it was sputtered (Schwartz et al., 1969). XRF is now used to measure film thickness more accurately and faster than stylus techniques (Dax, 1996). It is also possible to identify and measure the thickness of individual components of a mutilayer film. Another more recent application has been the rapid detection of low concentrations (1 to 5 ppb) of transition metals in semiconductor processing chemicals (e.g., HF). The analysis, called "dried residue XRF," can be performed by relatively unskilled personnel right on the manufacturing line (Gupta et al., 1996).

2.16 HYDROGEN ANALYSIS

2.16.1 Introduction

The identification of H incorporated into SiO_2 and plasma nitride (SiN_xH_y) films by IR spectroscopy as Si–H, Si–OH, and N–H has been mentioned. This section deals with the quantitative analysis of H and its depth distribution in films; this information has been used to calibrate the IR bands.

2.16.2 Resonant Nuclear Reactions

2.16.2.1 $^1H + ^{15}N$

The narrow isolated resonance in the nuclear reaction (Lanford et al., 1976)

$$^1H + ^{15}N \rightarrow ^{12}C + ^4He + \gamma \text{ rays (4.43 MeV)}$$

was employed to determine the H content of PECVD SiN_xH_y films (Lanford and Rand, 1978). To carry out the measurement, the sample is bombarded with a beam of 6.385 MeV $^{15}N^{2+}$, since there is an appreciable probability for a reaction only at that energy. The number of γ rays emitted is proportional to the H-concentration at the surface. As the energy is increased, there is no further reaction at the surface, but as the ions are slowed passing through the film, resonance will occur at some depth, and the yield of γ rays is proportional to the H-concentration at that depth. By measuring the γ ray yield vs. ^{15}N energy, a profile of H-concentration vs. depth is obtained. The depth resolution is 5 to 10 nm and the sensitivity is better than 1 part in 1000 or ~$2 \times 10^{19}/cm^3$. The H-content of the

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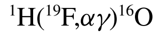
plasma nitride films studied was in the range 20 to 25 at%. It was possible to calibrate the IR absorption bands corresponding to Si–H (2160 cm^{-1}) and N–H (3350 cm^{-1}) and it was determined that the Si–H band had about 1.4 times the absorptivity of the N–H band. Another study of plasma nitrides covered films containing a wider range of H-concentration, 4 to 39 at% (Chow et al., 1982). Xie et al. (1989) extended the measurement to the comparison of LPCVD and PECVD silicon nitrides. Xie et al. (1988) used the technique to determine the H-concentration profiles in as-deposited and annealed CVD PSG.

2.16.2.2 $^{1}H(^{19}F,\alpha\gamma)^{16}O$

Another resonant nuclear reaction for measuring H-concentration profiles is



$$^{1}H(^{19}F,\alpha\gamma)^{16}O$$

which shows a strong resonance at 0.83 MeV (Leich and Tombrello, 1972). According to Lanford et al. (1976), it has a better yield but a poorer depth resolution than the $^{1}H + {}^{15}N$ reaction (~200 Å) and has a limited range (~0.4 μm).

2.16.2.3 $^{1}H(^{15}N\alpha\gamma)^{12}C$

Leich and Tombrello also mention another resonance which may be useful for measuring proton profiles:

$$^{1}H(^{15}N\alpha\gamma)^{12}C$$

which has a strong resonance at 0.40 MeV; the estimated resolution is about 50 Å, and the maximum depth ~3 μm.

2.16.3 Proton–Proton Scattering

Still another method for quantitative determination of H is proton–proton (*p-p*) scattering (Cohen et al., 1972). It was used to measure H-profiles in PECVD nitride (Paduschek and Eichinger, 1980), for which it was preferred to the $^{1}H(^{19}F,\alpha\gamma)^{16}O$ reaction because a tandem accelerator was necessary to generate a sufficient yield of ^{19}F ions with the required high energy (16 to 18 MeV). This *p-p* scattering method has sensitivity in the parts per million range, but at the expense of some loss in depth resolution. In addition, it requires thin samples since it is a transmission technique. This method was used to measure H-concentration in PECVD nitride films, using a standard mylar film for calibration.

2.16.4 Forward-Scattering Elastic Recoil Detection (ERD)

This method (Doyle and Peercy, 1979), which is related to Rutherford backscattering spectroscopy (discussed below) has also been employed. Gujrathi and Bultena (1992) and Godet et al. (1992) coupled ERD with a time-of-flight (TOF) detection system for better depth resolution and increased depth range. A beam of 2.5 MeV He^{+} impinges on the sample; the recoiled H atoms and forward-scattered He^{+} appear in the same direction; the He^{+} are absorbed in a mylar film and the H atoms detected and measured. EDR has been used to measure the H-content of PECVD silicon nitride (Takahashi et al., 1987) and of LPCVD silicon oxynitride films (Kuiper et al., 1988).

2.16.5 Other Techniques

SIMS, discussed above, has been used for H analysis and profiling.

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Mass spectrometry has also been used for the quantitative analysis of the H-content of plasma silicon nitride (Yoshimi et al., 1980). Recently, nuclear magnetic resonance (NMR), with a detection limit of 10^{19} H/cm^3 has been used to measure H incorporated during the growth of an SiO_2 film and that resulting from contamination of the surface during processing (Levy and Gleason, 1993).

2.17 RUTHERFORD BACKSCATTERING SPECTROMETRY (RBS)

2.17.1 Introduction

RBS yields quantitative information about elemental composition and quantitative depth profiles and is used in the analysis of both metals and dielectrics.

2.17.2 Principles/Description

The basis for the measurement is the scattering of impinging ^{4}He ions by atoms (of mass > mass of ^{4}He) in a solid. It is inherently a quantitative technique since the scattering cross-sections and He stopping cross-sections in all elements, required for the analysis, are known. Another advantage is the speed of data collection. The disadvantage is the limitation in the detection of light elements; this can be overcome by using a low-mass substrate such as C. Another weakness is the lack of specificity; two elements of similar mass cannot be distinguished if they appear together in a sample. In addition, the sample must be uniform laterally and in depth (Chu et al., 1978).

When a collimated beam of monoenergetic high-energy (MeV range) doubly ionized ^{4}He strikes a sample, a small fraction of the ions undergoes elastic collisions with the nuclei of the atoms in the sample. The large repulsive coulomb forces between them result in elastic scattering of the ^{4}He ions. Figure 2.38 shows a schematic of a collision between a projectile of mass M_1, velocity v_0, and energy E_0 and the target of mass M_2, initially at rest. After the collision, the velocity of the projectile is v_1 and its energy E_1 and those of the target are v_2 and E_2.

The energy of the scattered projectile, the ^{4}He ion, identifies the atom on the *surface* of the sample since $E_1 = K_m E_0$, where E_1 is the energy after scattering by surface atoms, E_0 the energy of the bombarding particle, and K_m is called the *kinematic factor*, tables of which exist. An example of the difference in E_1 for two elements, Au and Al, after collision with a projectile of a given energy E_0, is shown in Figure 2.39.

The probability that a collision will result in a scattered particle is given by the scattering cross-section σ, which is proportional to Z^2, where Z is the atomic number. High-Z atoms are detected

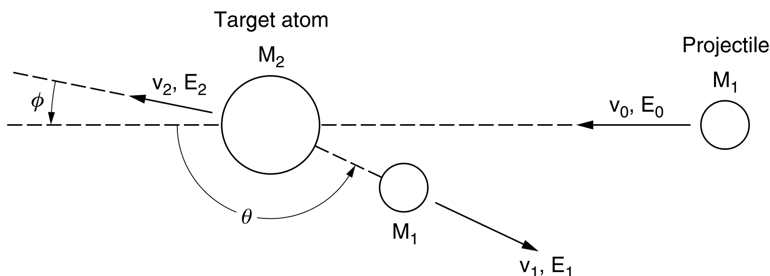

Figure 2.38 Schematic of an elastic collision between projectile of mass M_1, velocity v_0, and energy E_0 and target mass M_2 initially at rest. After the collision, projectile and target mass have velocities and energies v_1, E_1 and v_2, E_2. (Reproduced from Chu, W.-K., J.M. Mayer, and M.A. Nicolet, *Backscattering Spectrometry*, Academic Press, New York, 1978. With permission. Copyright 1978, Elsevier.)

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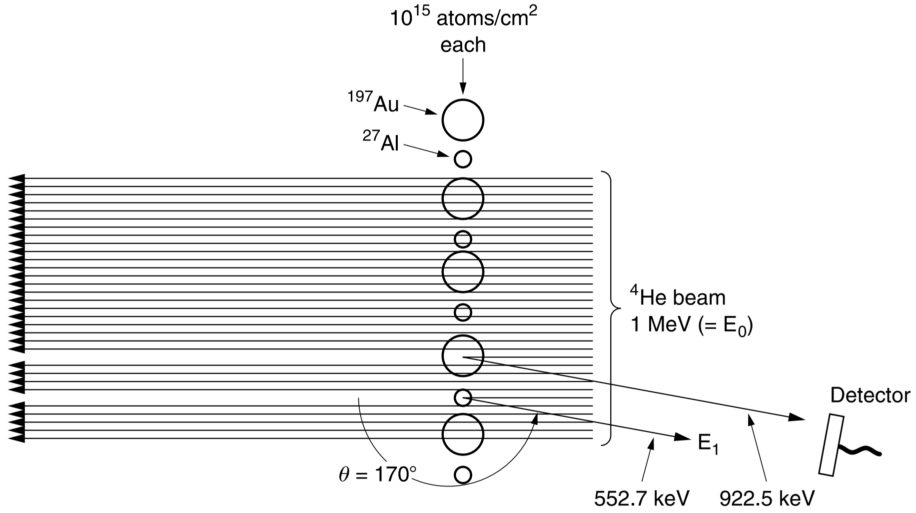

Figure 2.39 Kinetic factor K_m gives the ratio of energy after (E_1) and before (E_0) an elastic collision of the projectile (^4He) with atoms of Au (197 amu) and Al (27 amu). (Reprinted from Chu, W.-K., J.M. Mayer, and M.A. Nicolet, *Backscattering Spectrometry*, Academic Press, New York, 1978. With permission. Copyright 1978, Elsevier.)

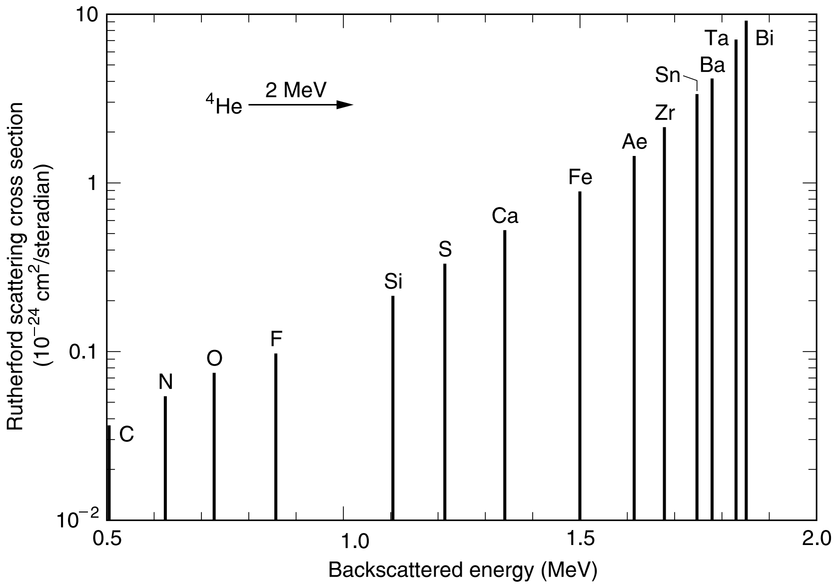

Figure 2.40 Graphical representation of how both Rutherford scattering cross-section and surface backscattering energy vary for elements across the periodic table.

with greater sensitivity than low-Z atoms. However, high-Z atoms are more difficult to distinguish from each other. Figure 2.40 shows how the scattering cross-section σ and surface backscattered energy E_1 vary for various elements.

The use of high-energy resonance backscattering (Li et al., 1995), i.e., the use of incident beams for which elastic scattering is resonant, increases the sensitivity for light atoms such as O, C, and N by enhancing the elastic scattering cross-section.

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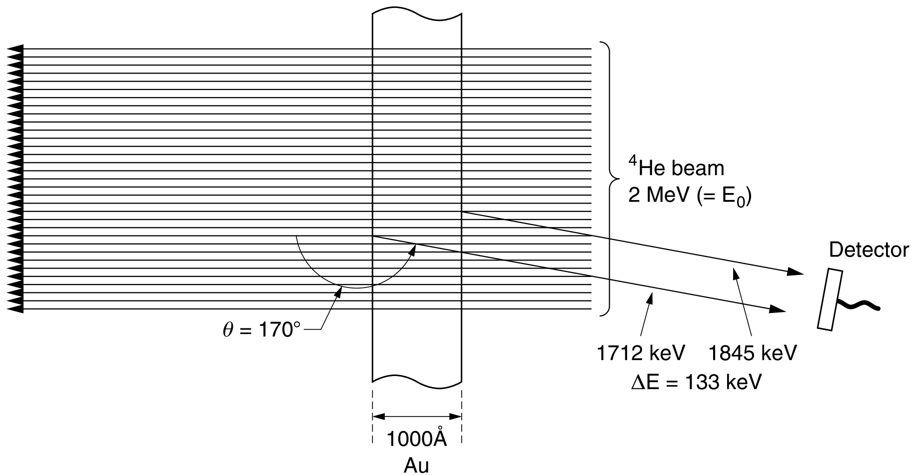

Figure 2.41 Energy loss as particle passes through a dense medium; particle scattered at the rear surface of the film has less energy when detected than a particle scattered at the front surface. (Reprinted from Chu, W.-K., J.M. Mayer, and M.A. Nicolet, *Backscattering Spectrometry*, Academic Press, New York, 1978. With permission. Copyright 1978, Elsevier.)

A particle loses energy as it travels through a solid, losing energy before scattering occurs from the back surface and thence to the detector, as illustrated in Figure 2.41. The loss of energy gives depth information. The values of energy loss through matter are given in tables of stopping cross-sections. Therefore, the differences in energy can be quantitatively related to the thickness of the film.

Since a multichannel analyzer is used to detect the scattered particles, more than one element can be detected simultaneously. This is shown in the example of Figure 2.42 of RBS of a film that contains equal numbers of a heavy atom M and a light atom m. Although the number of atoms of each kind is the same, the yield of the heavier atom is greater than that of the lighter one. The signal due to the light mass is at a lower energy than that of the heavier one.

2.17.3 Applications

Among the applications of RBS are the determination of the composition and thickness of metallic and dielectric films, epitaxial layers, and surface impurities, and the study of thin-film reactions of all kinds (e.g., silicide formation, oxidation, interdiffusion) and implant profiles. Figure 2.41, Figure 2.43, and Figure 2.44 illustrate some of these applications.

RBS has been used increasingly to determine the density of porous dielectric films. The RBS spectrum yields the area density (atoms/cm^2) of the components of the film; from the independently measured film thickness, the average density of the entire film can be obtained. RBS is also used with SXR (see Section 2.18) for density calculations.

For a more complete discussion of RBS, the reader is referred to Chu et al. (1978).

2.17.4 Forward Recoil Scattering

Forward recoil scattering (FRES) or ERD, described in the section on H-analysis, is a relative of RBS and can be performed in an RBS chamber. The method can be used for any atoms lighter than the projectile.

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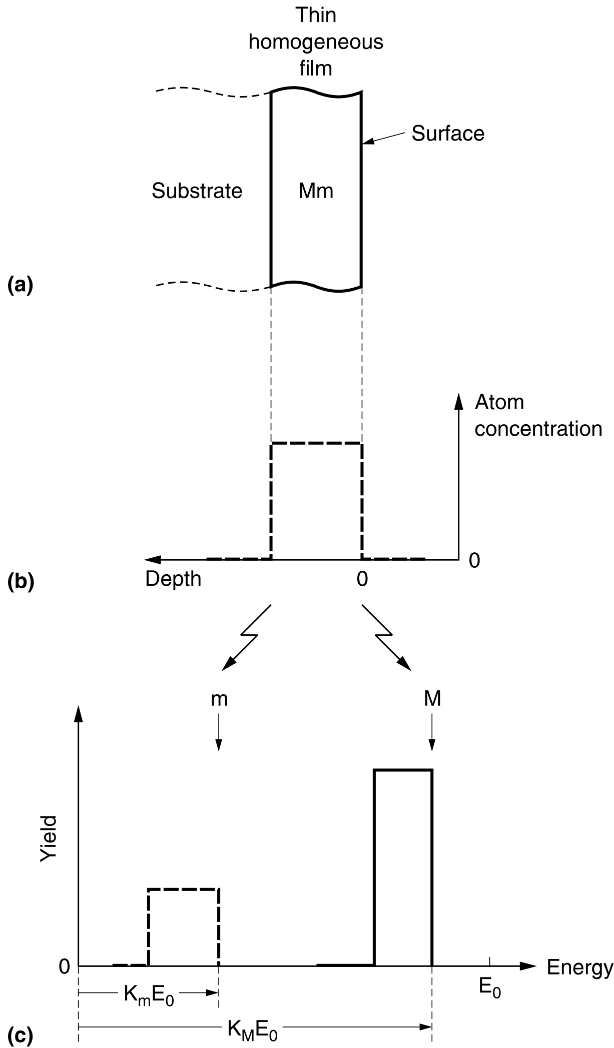

Figure 2.42 Translation of concentration profiles to signals in a backscattering spectrum from a thin homogeneous film of binary compound Mm with elements of a heavy M and a light m atomic mass. In the lower panel profiles appear as two separate signals. Light mass → low energy/yield, heavy mass → high energy/yield. (Reprinted from Chu, W.-K., J.M. Mayer, and M.A. Nicolet, *Backscattering Spectrometry*, Academic Press, New York, 1978. With permission. Copyright 1978, Elsevier.)

2.18 SPECULAR X-RAY REFLECTIVITY (SXR)

This technique is valuable for measuring accurately the structure of thin films (i.e., thickness, uniformity, roughness, average film density) in the direction normal to the film surface. It has been used to characterize porous films, usually in conjunction with small-angle neutron scattering (SANS) (see Section 2.19). SXR results are an average over a lateral dimension of a few micrometers.

The incident x-ray beam has a wavelength λ; the reflected intensity is measured at grazing-incidence angles. The critical angle θ_c determined from an x-ray reflectivity curve (see below) is defined as "the grazing-incidence angle at which a well-collimated beam of e-rays is no longer totally reflected off the free surface, but starts penetrating into the sample" (Wallace and Wu, 1995).

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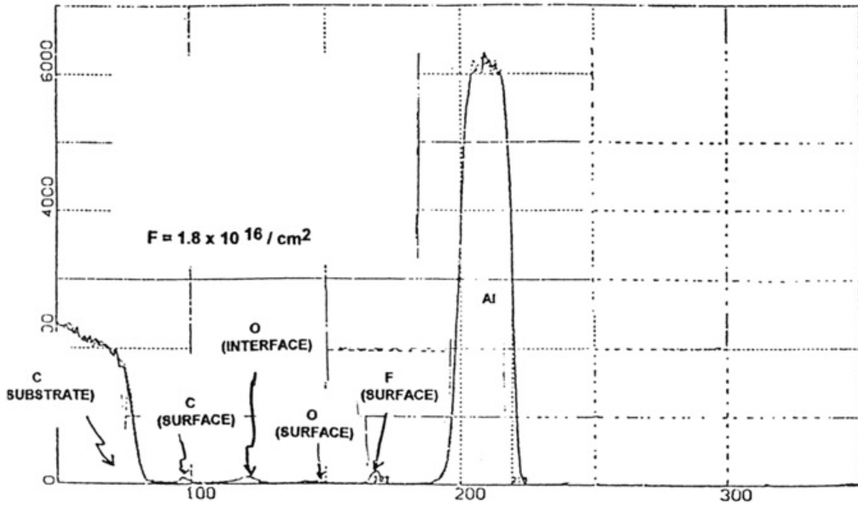

Figure 2.43 Backscattering spectrum for 2.0 MeV $^4He^+$ incident on Al (deposited on a carbon substrate instead of oxidized Si to eliminate interferences) after exposure to a CF_4 plasma during overetch of an overlying SiO_2 film. (From Chu, W.-K. and G.C. Schwartz, unpublished, 1976.)

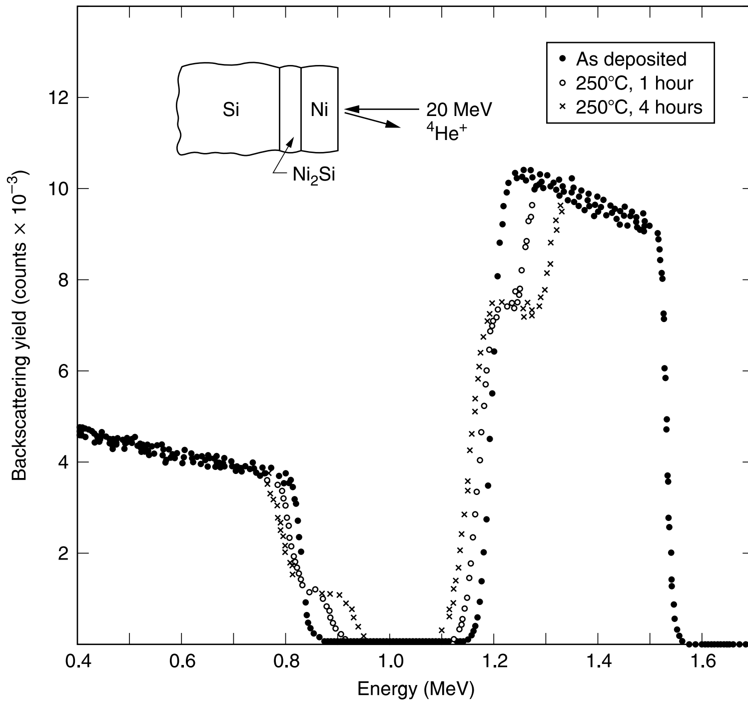

Figure 2.44 Backscattering spectra for 2.0 MeV $^4He^+$ incident on a multilayer sample of Ni on Si, before and after heat treatment; it shows the formation and growth of a Ni_2Si layer at the Ni–Si interface, forming an intermediate layer between the Ni and Si, as indicated by the shoulders developed in the Ni and Si portions of the spectra. (Reprinted from Tu, K.N., W.K. Chu, and J.W. Mayer, *Thin Solid Films*, 25, 403, 1975. With permission. Copyright 1975, Elsevier.)

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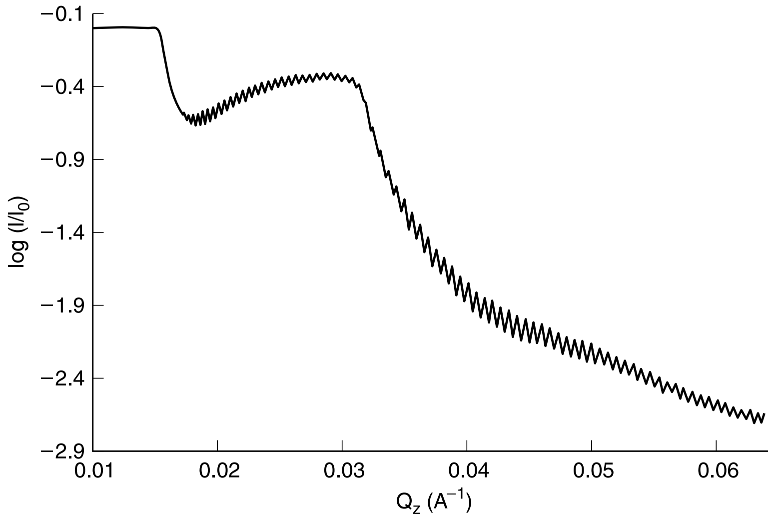

Figure 2.45 Specular x-ray reflectivity (SXR) curve: logarithm of the reflectivity (log I/I_o) vs. the momentum transfer normal to the sample surface Q_z for Nanoglass film on Si. The steep drop at $Q_z = 0.0155$ A^{-1} is the critical edge for reflection of the porous film and at $Q_z = 0.032$ A^{-1} for the Si substrate. (Reproduced from Wu, W.-i, W.E. Wallace, E.K. Lin, G.W. Lynn, C.J. Ginka, E.T. Ryan, and H.-M. Ho, *J. Appl. Phys.*, 87, 1193, 2000. With permission.)

The critical angle can be approximated (Wu et al, 2000):

$$\theta_c = (\rho r_e \lambda^2/\pi)^{1/2}$$

where ρ = electron density, λ = x-ray wavelength, and $r_e = 2.818$ fm, the classical electron radius.

Figure 2.45 shows an x-ray reflectivity curve, log (I_r/I_o) vs. Q_z (for a nanoporous silica film) where I_r = reflected beam intensity and $Q_z = (\pi/\lambda)\sin\theta_c$, the momentum-transfer vector normal to the surface of the film. The drop in reflectivity indicates a critical angle. In Figure 2.45, the first is related to the electron density of the thin film and the second to that of the Si substrate. The high-energy x-rays excite all the electrons in the sample so that the determination of the electron density of a thin sample is independent of chemical bonding and molecular orientation (Wallace and Wu, 1995).

Very small misalignment of the sample can result in large errors in the electron density. The easiest way to obtain the true value is to make the measurements at a sufficiently large number of x-ray wavelengths (energies) and extrapolate the calculated densities to infinite wavelength (Wallace and Wu, 1995; Windover et al., 2000).

From the chemical composition of the film (from RBS and FRES measurements) and the average electron density (from θ_c) the average mass density of the film may be calculated. Windover et al. (2000) point out that the technique measures film density near the surface region. The porosity P, however, requires a knowledge of the density of the pore wall, i.e., of the solid material surrounding the pore ρ_w since $\rho_{eff} = \rho_w(1 - P)$. By assuming a reasonable value for it, the porosity can be estimated, but no information about pore size can be obtained using this method.

The film thickness can be determined by analysis of the periodicity of the oscillations in the reflectivity profile which result from the interference of the x-rays reflected from the air/film and film/Si interfaces. The change of thickness measured upon heating a sample can be used to calculate the out-of-plane coefficient of thermal expansion (CTE).

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Surface and interfacial roughness and density variation can be determined using computer modeling to create electron density depth profiles that best fit the experimental data. Hsu et al. (2000) used a three-layer model to describe a xerogel film (surface modified xerogel/xerogel/substrate) and fit the intensity data and analyzed the x-ray scattering intensity data using a fractal model.

2.19 SMALL-ANGLE NEUTRON SCATTERING (SANS)

This technique can be applied to porous thin films on a Si substrate. Since single-crystal Si is essentially transparent to the neutron beam, the scattered beam is due almost entirely to the structure in the film, i.e., from the difference in the neutron scattering length of the connecting pore wall material and the pores themselves (taken as zero). Often many samples are stacked to enhance the signal. The wavelength λ of the neutrons is 6 Å and the beam is incident normal to the sample. The resultant scattering vector q is given by

$$q = (4\pi/\lambda)\sin\theta/2$$

where θ is the angle between the incident and scattered beam paths. The data can be interpreted qualitatively from the shape of the log I vs. q curve (I = absolute intensity, derived from the scattering intensity data using water as a standard). Low values of q represent larger length scales; higher q values represent smaller length scales. Quantitative analysis, however, requires a suitable model. A two-phase model in which there are only pores and matrix material which is homogeneous is the simplest. The SANS intensity, based on this model, is (Wu et al., 2000)

$$I(q) = [8\pi P(1-P)\Delta\rho_n^{\,2}\xi^3]/(1 + q^2\xi^2)^2$$

where P = porosity, $\xi/(1-P)$ = average dimension or chord length, ξ/P = average dimension of the wall between the pores, $\Delta\rho_n$ = neutron scattering length contrast between the two phases; it is linearly proportional to atom or mass density and explicitly $\Delta\rho_n = \rho_{wn}$ the neutron scattering length of material between pores. In turn

$$\rho_{wn} = \left(\sum n_i b_i / \sum n_i m_i\right)\rho_w$$

where n_i = atomic fraction of element i, b_i = neutron scattering length of element i, m_i = atomic weight of element i, and ρ_w = mass density of connecting material between pores.

The chemical composition (except H) can be determined by RBS (Section 2.17) and the H-content by FRES (Section 2.16.4); the neutron scattering values are known; only ρ_w is unknown.

By rearranging the equation for $I(q)$

$$1/I(q)^{1/2} = 1/(c\xi^3)^{1/2} + \xi^2 q^2/(c\xi^3)^{1/2}$$

where $c = 8\pi P(1-P)\Delta\rho_n^{\,2}$ and plotting $I(q)^{-1/2}$ vs. q^2 (Figure 2.46), c and ξ can be determined from the slope and zero q intercept (obtained by extrapolating the linear portion of the curve). The quantity c is related to the porosity P and ρ_w as $P(1-P)\rho_w^{\,2}$. The thin-film density $\rho_w(1-P)$ can be determined from SRX measurements (Section 2.18) so that P and ρ_w can now be determined. The value of ρ_w of a xerogel, for example, is significantly less than that of dense SiO_2, although they have often been assumed to be equal (Murray et al., 2002).

Pore interconnectivity can be evaluated by immersing the sample in an organic solvent. An example is shown in Figure 2.46, where the upper curve is for the original sample and the lower curve is for the one immersed in the solvent. If all the pores were filled the curve would merely be displaced by a factor related to the difference in scattering between air and the solvent. There is a difference in shape indicating that not all the pores are filled and the volume fraction of filled pores can be determined from the known neutron scattering length of the solvent and the results of the

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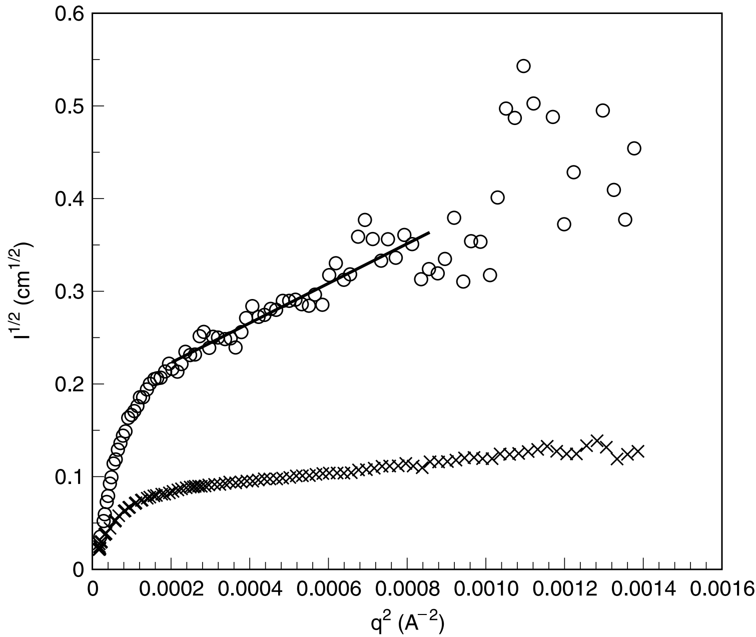

Figure 2.46 Plot of $I(q)^{-1/2}$ vs. q^2 for a stack of Nanoglass films. $I(q)$ is the SANS intensity, q is the scattering vector $(4\pi/\lambda)\sin \theta/2$, and θ is the scattering angle. Open circles (upper curve): the films as received; crosses (lower curve): the films immersed in deuterated toluene. (Reproduced from Wu, W.-i, W.E. Wallace, E.K. Lin, G.W. Lynn, C.J. Ginka, E.T. Ryan, and H.-M. Ho, *J. Appl. Phys.*, 87, 1193, 2000. With permission.)

calculations for the original sample. In the same way, the moisture uptake can be measured by immersing the sample in water.

2.20 POSITRONIUM ANNIHILATION LIFETIME SPECTROSCOPY (PALS)

This is a method for determining the pore size distribution (PSD) of closed pores (e.g., Gidley et al., 1999, 2000; Sun et al., 2001) as well as the average pore size of open pores.

A focused beam of positrons of several keV impinging on a thin film forms positronium (Ps, the electron–positron bound state) over a distribution of depths that depend on the beam energy. In a porous film, Ps localizes in the pores where its natural lifetime of 142 ns is reduced by annihilation with molecular electrons during collisions with the pore surfaces. The collisionally reduced lifetime is correlated with void size and permits a PALS lifetime distribution to be transformed into a PSD if Ps is trapped in isolated voids of varying sizes. The Ps decay rate $(1/\tau)$ for Ps of thermal velocity v is

$$\lambda = 1/\tau = \lambda_T + vP_A/l$$

where $l =$ mean free path between collisions (a linear measure of pore size, $l = 4 \times \text{volume}_{\text{void}}/\text{surface area}_{\text{void}}$), λ_T is the vacuum decay rate of Ps, and P_A is the probability of annihilation per collision with the solid surface ($vP_A = 0.021$ nm/ns for silica powders).

If the pores are interconnected (as in xerogels), the highly mobile Ps atoms diffuse throughout the pore network out of the film and into the vacuum and annihilate with a single, average lifetime (~140 ns), very near the vacuum lifetime. If a capping layer is deposited, diffusion of Ps into the vacuum is prevented and an average pore size can be measured from the observation of a single average lifetime of Ps diffusing within the porous network. The measured Ps lifetime was, indeed, longer for the more porous film which does have larger pores.

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In the case of a more complex structure, one with both closed and interconnected pores (e.g., porous MSQ), capping allowed the observation of two shorter lifetime components of closed pores (l ~ 1.5 and 3.5 nm). In dense MSSQ, only very short lifetimes were observed, i.e., the film contained only micropores, not mesopores.

2.21 ELLIPSOMETRIC POROSIMETRY (EP)

This is a new version of the well-known method, the analysis of the adsorption isotherm, for determining the PSD of open pores in films.

The dependence of the quantity of an adsorbate in the pores on the ratio of the vapor pressure in the pores to the equilibrium vapor pressure of a flat liquid surface (P/P_o) is an adsorption isotherm. Isotherms of mesoporous films, e.g, xerogels and other porous ILD films, are characterized by a hysteresis loop since the process of condensation (which requires a nucleus for condensation) and that of evaporation (which occurs spontaneously) are not necessarily exact reverses of each other.

EP uses the changes in the optical characteristics of the porous film, i.e., the changes of the ellipsometric angles Δ and Ψ (changes in refractive index n and thickness t) as the vapor pressure of the absorbate is varied during filling and emptying the pores by a nonpolar solvent. It is designed to replace the classical method of direct weighing of an absorbate (e.g., liquid N_2, Hg) by using an ellipsometer installed in a vacuum chamber. It is, therefore, applicable to thin films deposited on a Si substrate and the method has been used to determine the PSD of xerogels (Dultsev and Baklanov, 1999; Baklanov et al., 2000; Baklanov and Mogilnikov, 2000).

The relation between the refractive index and the material composition of a multicomponent system can be described by the Lorentz–Lorenz equation:

$$B = \sum N_i \alpha_i = 3(n^2 - 1)/4\pi(n^2 + 2)$$

where B is the polarizability of a unit volume, N_i the number of molecules of component i, and α_i the molecular polarizability of the ith component.

The full pore volume, i.e., the relative porosity V, can then be calculated:

$$V = 1 - B_p/B_d = 1 - [(n_p^2 - 1)/n_p^2 + 2] + [n_d^2 - 1)/(n_d^2 + 2)]$$

using the values of n of the porous film (p) and the dense part of the material (d).

The open or interconnected pore volume can be calculated knowing n and ρ (density) of the adsorbate. In this case the adsorptive volume in the pores is:

$$V_{ads} = (V_{mol}/(\alpha_{ads}t_1)(B_1t_1 - B_0t_0)$$

where V_{ads} is the volume of the open pores, V_{mol} is the molecular volume of the adsorbate, α_{ads} is the polarizability of the adsorptive molecule, and t_0 and t_1 are the film thickness before and after adsorption.

The Kelvin equation

$$\ln P/P_o = (-2\gamma V_L/RT)(1/r_m)$$

is used to interpret the isotherm. In the equation, γ is the surface tension and V_L the molar volume of the absorbate and r_m is the radius of curvature of the concave meniscus of the liquid in the pore; this has been taken as equal to the radius of the pore minus the thickness of the film adsorbed on the walls, i.e., the *core* size. BET and related methods are used for estimating the thickness of the adsorbed layer. The relation of r_m to pore size requires a model of the pore shape; often a cylindrical model is assumed so that r_m equals the pore radius r^p.

The pore size distribution also makes use of the Kelvin equation. For cylindrical pores ($r_m = r^p$), this is accomplished by finding "at any point (n_i, P/P_o) on the isotherm, the volume v^p of all the

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pores having r^p values up to and including r_i^p was given by $n_i V_L$. From the curve of v^p vs. r^p, the size distribution curve dv^p/dr^p vs. r^p is obtained" (Gregg and Sing, 1982).

2.22 SCANNING ELECTRON MICROSCOPE (SEM)

2.22.1 Introduction

The SEM may be the most widely used of the modern analytical instruments since there are microscopes designed to be installed in fabrication facilities and used by the personnel there, for inspection and measurement. There are, in addition, instruments designed for highly skilled microscopists. The SEM is used to study the surfaces of thin films as well as the structures fabricated by the various processes discussed in this book. Some of the newer models allow for extensive examination of entire wafers but, in many cases, only small pieces can be accommodated.

2.22.2 Application

For many applications the SEM has completely superceded the optical microscope because the small dimensions of semiconductor devices require much higher magnification. The SEM offers not only greater resolution and depth of field, but also typically comes with the ability to perform some analytical functions, such as EDS and WDS (described earlier). With some modifications of the SEM, electron induced current (EBIC) and voltage (EBIV) may be observed to study semiconductor devices. Many of the smaller SEMs do not perform well at the low accelerating voltage required to eliminate image distortion due to charging of insulated regions; therefore samples are coated with a thin conducting layer. This may hide buried features, e.g., voids in an insulator-coated metal, which are seen easily in an optical microscope.

2.22.3 Operation

The electron–specimen interactions are shown in Figure 2.47. Figure 2.48 shows a schematic of an SEM.

An electron gun generates a narrow electron beam with a high brightness. W or LaB_6 (for thermonic emission) or a field emission gun (for high brightness and long operating life) are used. As the beam is rastered across the sample surface, secondary electrons are emitted from the surface (from the escape depth) and create the image displayed on a CRT; this image is the one used most widely. Tilting the sample increases the secondary electron signal; this is illustrated in Figure 2.49. More complete topographical information can be gleaned from tilted samples, but this requires a large sample chamber if entire wafers are to be examined

Backscattered primary electrons originate from a much larger volume within the depth of the sample. In this mode, the higher density regions appear brighter, so it contributes additional information, e.g., observation of Cu segregation to the grain boundaries in an AlCu alloy film.

2.22.4 Examination of Cross-Sections

Examination of cross-sections is one of the most valuable SEM operations. Both cleaved and polished sections are used, but artifacts can occur more readily using the more easily prepared cleaved sections. Often the samples are decorated with an appropriate etchant to reveal features such as growth seams and grain size, but the fact that defects are often exaggerated must be kept in mind. It is often difficult to isolate specific structures when they are not periodic; thus time-consuming polishing may be necessary. A more complete description and discussion of scanning electron microscopy can be found in references such as Wells et al. (1974).

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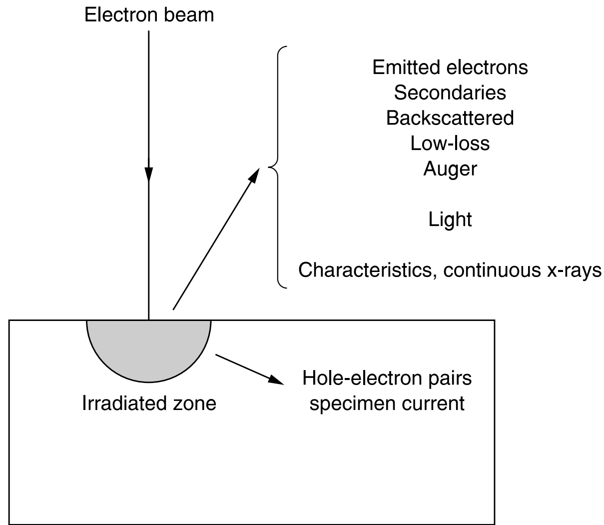

Figure 2.47 Electron–specimen interactions in an SEM.

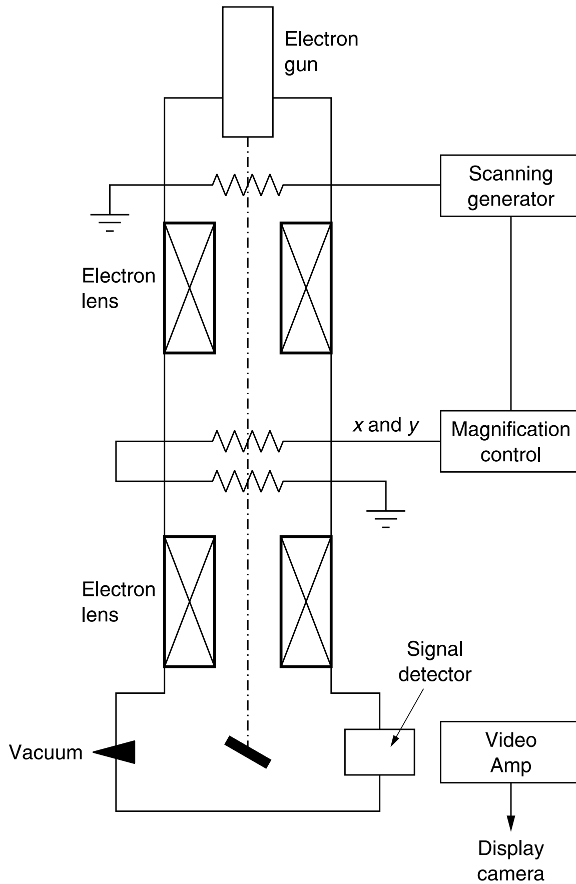

Figure 2.48 Schematic of an SEM.

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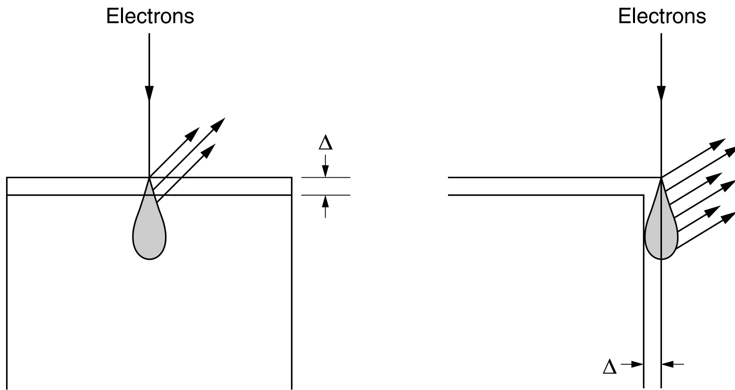

Figure 2.49 Enhancement effect of specimen tilt on secondary electron emission in an SEM (Δ = escape depth).

2.23 TRANSMISSION ELECTRON MICROSCOPE (TEM)

The TEM is being used more widely in spite of the labor-intensive and time-consuming sample preparation (see below). It continues to be a research instrument and is the only technique capable of solving structure and processing problems encountered in device fabrication.

2.23.1 Operation

A schematic of a TEM, equipped also for x-ray and energy-loss spectroscopy, is shown in Figure 2.50.

A TEM uses a high-energy electron beam which impinges upon and passes through a very thin sample; the entire imaged specimen area is illuminated simultaneously. Electron diffraction patterns are produced, so that structural and chemical information can be obtained. Both flat (plan view) and vertical (cross-section) samples can be examined.

However, unless the very large (and rare) very high-voltage TEM is used, only very thin samples can be examined; this requires tedious and lengthy sample preparation and mounting. Mechanical or electrochemical polishing, chemical etching, and ion milling are methods used to attain the desired thickness. Dual-beam FIB-SEM (FIB is covered in Section 2.24.2) equipment is now being used to prepare clean, very thin, accurately located specimens for examination (Pantel et al., 2002).

2.23.2 Scanning TEM (STEM)

In the STEM, the specimen is scanned in a raster, point-by-point, with a small electron probe.

2.23.3 Analytical TEM

2.23.3.1 Electron Energy-Loss Spectroscopy (EELS)

In EELS the primary processes of electron excitation are studied; each process results in a fast ($\geq$ 100 keV) electron losing a characteristic amount of energy. The beam of transmitted electrons is directed into a TEM which separates the electrons according to their kinetic energy, producing an electron energy-loss spectrum showing the inelastic scattered intensity as a function of the

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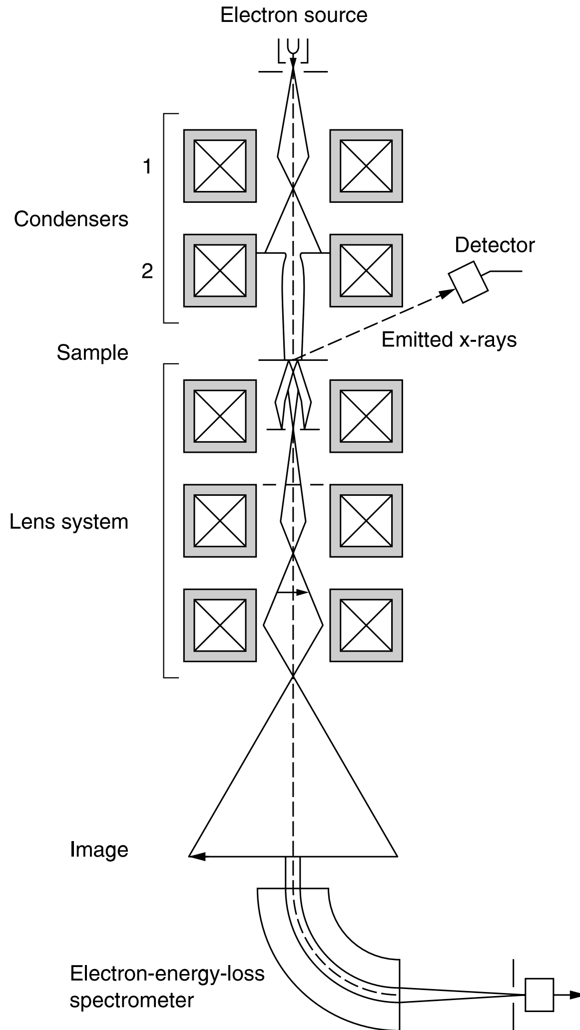

Figure 2.50 Schematic of a TEM.

decreasing kinetic energy of the incoming electrons. One of the most important energy losses is due to atomic ionization, i.e., ejection of electrons from inner shells of the atoms. To accomplish this, the incoming electrons must have an energy more than the critical ionization energy E_c which is a function of the specific atom and electron shell and is, therefore uniquely defined. The characteristic signals, ionization edges, are seen in the spectrum at energy losses corresponding to E_c; they identify specific elements. The intensity of the edge can be related directly and quantitatively to the amount of that element. The samples must be thin (50 to 150 nm) to avoid unwanted multiple scattering peaks.

In a typical spectrum there also appears a zero-loss peak which includes electrons that have not been scattered, i.e., have lost no energy and emerge undeflected. In the low loss region are the peaks due to inelastic scattering from outer-shell electrons, which can sometimes be used to identify the material (Egerton, 1996; Keast et al., 2001).

In addition to elemental information the ionization edges have small intensity fluctuations, just above the edge onset, called energy-loss near-edge structures (ELNES). These are dependent on

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details of the local atomic environment: coordination, valence, and type of bonding. According to Keast et al. (2001), “the main advantage of ELNES is the potential to examine changes in bonding with a spatial resolution at the nanometer level and even approaching the level of interatomic spacing.”

Electron scattering theory, instrumentation, quantitative analysis, and applications of EELS are discussed in depth in Egerton (1996).

2.23.3.2 Energy Filtering TEM

“The incorporation of an imaging filter in an electron microscope greatly increases the amount of information that can be obtained about the object” (Rose and Krahl, 1995). It improves the contrast of the image.

Filters can be an integral part of the TEM (within the column) or one can be attached beneath the viewing screen (postcolumn image filter). The energy selecting slit can be centered at the zero-loss peak. The result is suppression of chromatic aberration with the improvement of contrast and resolution; small details not seen in the unfiltered image become visible. Another selects ranges of the energy-loss spectrum corresponding to elements in the sample. So-called color images are obtained when several exposures are taken, each with different characteristic energy losses so that each color corresponds to a specific element (Pantel et al., 2000).

Types of imaging energy filters are described in detail by Rose and Krahl (1995) and Egerton (1996). They include the Castaing–Henry filter (a triangular magnetic double prism and an electrostatic mirror), magnetic filters, and a retarding Wein filter (a combined electric–magnetic spectrometer), and for postcolumn filtering, a magnet with curved pole faces followed by a sequence of multipoles.

2.23.3.3 Analytical TEM with Auxiliary Equipment

Extensive physical and chemical characterization of complex systems has been performed by adding EDX, electron microdiffraction, and STEM Z contrast mode (in which electrons scattered at a large angle are collected; compounds containing Z elements are brighter) to the TEMs described above. Advanced detectors and fully integrated software enhance the analytical capabilities of the system. The Al/Ti/W/Ti interface reaction was studied completely using such a TEM (Pantel et al., 2000).

2.24 FOCUSED ION BEAM (FIB)

2.24.1 Introduction

Ion beams, focused to submicrometer dimensions (0.04 to 0.1 μm), have been used in many ways in the development of IC fabrication processes. Commercial FIB equipment is available (Seiko Instruments, Inc.; JEOL).

2.24.2 Description

An FIB system consists of an ion source (a liquid metal), an ion optical column, and a sample stage; it resembles an e-beam exposure system, with ions replacing electrons. The FIB system can deliver the desired dose with 0.1 μm accuracy, aligned to existing features on a wafer. Ion milling with inert ions, reactive ion-induced deposition, and etching for mask and circuit repair are done with elemental sources (Melngailis, 1987, 1988).

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FIB deposition has been modeled by Overwijk and van den Heuvel (1993). To test their model they used the deposition of W (from tungsten hexacarbonyl directed at the surface through a nozzle close to it) and a raster-scanned Ga^+ FIB source. As might be expected, redeposition and loss of sputtered material is important.

Alloy sources are used, with mass separation (since several species of ions are sometimes emitted by the source) for implantation without masking. Thus FIB can be used for process optimization by implanting neighboring devices, which may have different geometries, with different dopant doses and for dose gradation within a device. Another possible use is in lithography (replacing e-beam exposure) since there is little or no proximity effect and writing speed is higher (Melngailis, 1988).

2.24.3 Applications

Nikawa (1991) has reviewed the application of the FIB techniques, mentioned above, to failure analysis. FIB is used to prepare maskless, clean, accurate microscopic cross-sections as well as multiple cross-sections in a very small area. Secondary electrons are emitted as a result of ion impingement, making it possible to view the cross-section *in situ* (by tilting the sample stage) using scanning ion microscopy (SIM). Other applications are preparation for further failure analysis by changing a circuit (cutting and connecting metal lines), making holes in a dielectric layer for electron beam probing, depositing probe pads, and marking for electron spectroscopy observation. A recent application is micromachining for TEM specimen preparation (Szot et al., 1992). Nikawa et al. (1989) have listed the advantages of FIB vs. SEM and TEM for cross-section examination.

An important application of the SIM function of the FIB is the observation of aluminum microstructure and thus grain size distributions (Nikawa et al, 1989; Nikawa, 1991; Pramanik and Glanville, 1990). In the SIM image, the strong contrast reflects the crystallographic orientation of each grain; this has been confirmed by comparison with TEM images. Thus the true microstructure can be obtained without the extensive sample preparation required for cross-sectional SEM or for TEM examination, which are the alternatives, since what appear to be grain boundaries upon optical and SEM observation of an aluminum surface are often merely surface shapes, since the surface is covered by the native oxide.

Some examples of the potential of FIB for fabrication of very small features for device fabrication have been reported. In one, in which 100 nm wide refractory metal lines were formed on Si, Koshida et al. (1990) exposed MoO_3 (a high-contrast negative resist for exposure to Ga^+ FIB), developed after exposure in alkaline solution, and reduced to Mo in H_2 at 800°C. The limiting resolution was determined by the FIB diameter. Yasuoka et al. (1990) fabricated microcontact holes in the SiO_2 insulating a Ge substrate.

2.25 ATOMIC FORCE MICROSCOPE (AFM)

The AFM (invented by Binnig and colleagues) “is a combination of the principles of the scanning tunneling microscope and the stylus profilometer” (Binning et al., 1986). “It is a method for high resolution topographic imaging” (Putman et al., 1992). An AFM measures attractive or repulsive forces between a tip (probe) and the sample by sensing the atomic force interactions between tip and sample. The distance of the tip to the surface is controlled within the scale of chemical bonds, i.e., a few angstroms. An AFM can image any surface, insulating or conducting. The probe does not damage the surface.

In operation, a constant force is maintained between the sample and the stylus, attached to a flexible cantilever, as it follows the contours of the surface. The cantilever stylus should have a sharp tip, a low force constant, and a high mechanical resonance frequency. The size of the cantilever can be reduced and very sharp tips produced using microfabrication techniques (Albrecht et al., 1990). The

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displacement of the cantilever is most often detected by the optical beam deflection technique (e.g., Putman et al., 1992). Other methods include optical interferomety (Erlansson et al., 1988), laser diode feedback detection (Sarid et al., 1990), and capacitive lever displacement (Goddenhenrich et al., 1990).

These instruments are being used increasingly to determine the surface finish after CMP; an instrument used for this purpose is available commercially (*Veeco Instruments Vx* atomic force profiler) (Cunningham et al., 2000). The AFM can also indicate elasticity (hardness) and measure the friction between tip and sample (Baselt, 1993).

2.26 THERMAL WAVE-MODULATED OPTICAL REFLECTANCE IMAGING (TW)

2.26.1 Introduction

This technique is often called simply thermal wave imaging. Its principal use is the detection of voids within a metallic conductor which is beneath an overlying dielectric layer.

2.26.2 Description

A small (0.8 μm) region of a sample is irradiated by a modulated Ar ion laser beam; the light is partially absorbed by the substrate. Periodic heat waves flow into the sample. If there are voids in the conductor, the heat flow is impeded so that the temperature of that region is higher than the regions that are void-free. Optical reflectance is a function of the surface temperature and it is the modulated reflectance of the irradiated area that is measured using a HeNe laser probe The laser beams remain stationary and the sample rastered beneath them (Smith et al., 1990a).

2.26.3 Application

The technique is very often used to detect stress voids and can also be used to detect electromigration voids, microcracks, and precipitates in Al alloy metallization (Smith et al., 1990b). The technique has been combined with surface imaging by laser deflection, which is sensitive to surface topography, to detect and measure roughness, hillocks, and scratches (Smith, 1991).

The technique is nondestructive (does not require removal of the dielectric film), rapid, and can detect defects smaller than the probe size. A commercially available apparatus is available (Therma-Wave, Inc., Fremont, CA).

High-energy backscattered electron imaging, using an STEM at 120 kV (or above) has been also used to detect small (~0.1 μm) voids in Al metallization beneath overlayers, as has TW. However, only small samples can be used (Follstaedt et al., 1991). In addition the instrument is much more complex than the TW apparatus and probably requires much more expertise in operation.

2.27 X-RAY DIFFRACTION (XRD)

2.27.1 Introduction

XRD is a method for determining the arrangement of atoms in a substance. Since the wavelength of x-rays is comparable to atomic spacing, diffraction can occur. XRD is usually used during process development.

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2.27.2 Applications

Among the applications are identifying the components of a thin film, e.g., an intermetallic phase in deposited or annealed alloy films ($CuAl_2$ in AlCu) or as the product of reaction between adjacent films during heat treatment (Ti/Al → $TiAl_3$), or identifying which silicide is formed when a metal reacts with the substrate during heat treatment. Other uses are: distinguishing between a single crystal or polycrystalline structure and between polycrystalline and amorphous structures, and determining texture (preferred orientation) in polycrystalline films. X-ray methods are also used in stress measurement.

2.27.3 Diffraction Pattern

An XRD pattern consists of a series intensity peaks vs. angle; each peak corresponds to a specific atomic spacing *d*. Bragg's law shows the relationship between the angle measured for each peak and the corresponding spacing:

$$n\lambda = 2d\sin\theta$$

where n is an integer (constructive interference), λ the wavelength of the radiation, d the spacing between adjacent planes in a crystal, and θ the angle that the primary and diffractive beam make with the plane; θ is called the Bragg angle. The diffraction pattern is a characteristic of a material and therefore can be used as a basis for identification.

The powder method is used most frequently; it depends on the diffraction of a collimated monochromatic beam from many randomly oriented crystallites. The earlier method recorded the spectrum on film. Today, the powder pattern is recorded using a counter diffractometer shown in Figure 2.51. There are various methods for detecting the radiation: Geiger counters, gas proportional counters, or crystal scintillation counters. During the measurement, the counter turns at an angular velocity ω and the sample turns at a velocity of $\omega/2$ to maintain focusing conditions and simple absorption geometry. The 2θ-values for each reflection are read directly from such a recording (Warren, 1990). Each line, in its position and intensity, represents a set of crystal planes, unique to the material. Identification is made by matching the powder pattern with one in the Powder Diffraction File. Every component in a mixture can be identified since each has a characteristic pattern, not altered by the presence of others. A diffractometer recording of the powder pattern of plated Cu is shown in Figure 2.52.

Detailed information about the fundamentals of x-ray crystallography, equipment, etc., can be found in various sources, e.g., Brown (1966), Wormald (1973), and Warren (1990).

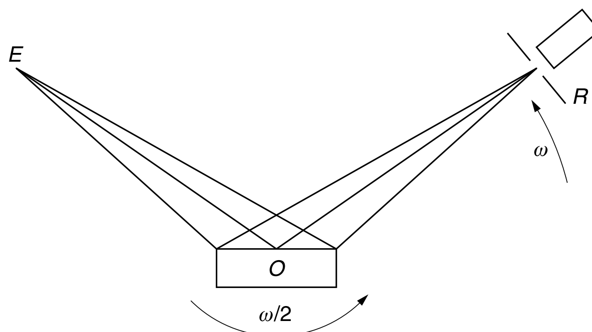

Figure 2.51 Schematic of a counter diffractometer as used for recording powder patterns.

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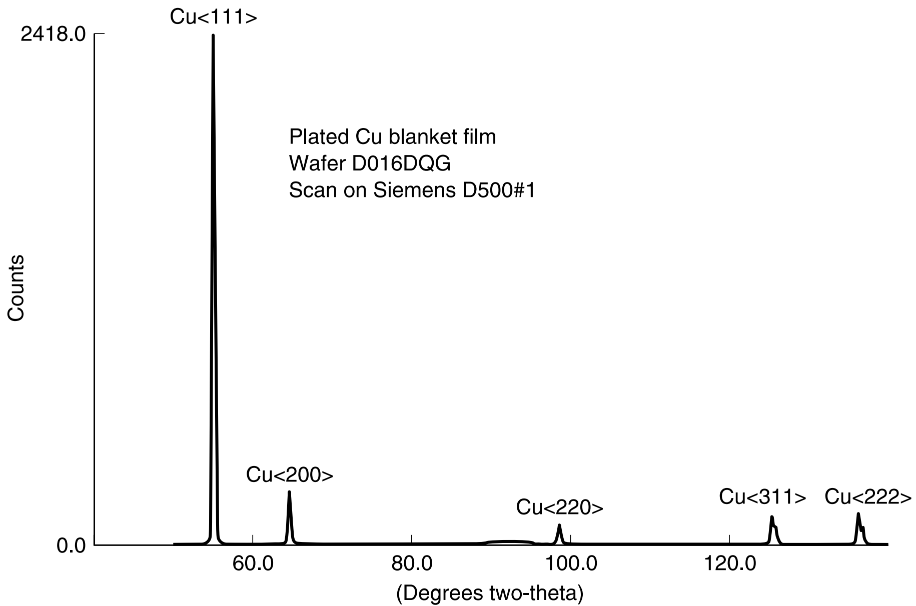

Figure 2.52 Powder pattern of a plated Cu film. (Courtesy of P. Dehaven, IBM Analytical Services. With permission.)

2.28 WET CHEMICAL METHODS

These may be divided into characterization techniques and analytical techniques.

2.28.1 Characterization

The evaluation and characterization of SiO_2 and plasma silicon nitride thin films is commonly carried out in HF-based solutions. One of these is the so-called preferential or "P" etch, 15 parts of 49% HF, 10 parts of 70% nitric acid, and 300 parts of water (Pliskin and Gnall, 1964), although dilute HF and buffered HF (NH_4F/HF mixtures of varying ratios) solutions are also used. Often the ratio of the etch rate of the oxide film in question is compared to that of thermally grown SiO_2. The etch rate (or etch rate ratio) is an indication of composition, bonding, and density, but *must* be used in conjunction with other tests to avoid erroneous conclusions. For example, increased density and excess silicon decrease the etch rate, whereas bond strain increases it (Pliskin, 1970); without other knowledge, one could not conclude which properties were responsible for the measured rate. The P-etch rate of PSGs tracks the phosphorus content. The etch rate of plasma nitrides in HF-based etchants correlates well with their H-content, which in turn influences the stress, density, and electrical properties of the films.

The etch rate in an alkaline solution has been used to characterize the completeness of the imidization reaction in curing polyimides (Ginsburg and Susko, 1984).

2.28.2 Analysis

The wet portion of the analysis, these days, consists of the dissolution of a sample and, when necessary, preparation for further instrumental analysis. The instrumental methods are discussed in another section of the chapter.

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One use of these techniques is in the analysis of the P-content of PSG films. In two of the methods, all the phosphorus is converted to orthophosphate and, in one case, reacted to form a colored solution which is analyzed by spectrophotometry (Hughes and Wonsidler, 1987) and, in another, coprecipitated as beryllium phosphate and counted by x-ray fluorescence (Adams and Murarka, 1979). The solutions have also been analyzed, without any further treatment, using ion chromatography of both phosphate and phosphite ions (Houskova et al., 1985) or of orthophosphate ion (Hughes and Wonsidler, 1987), or inductively coupled plasma/atomic emission spectroscopy (Levy and Kometani, 1987). Houskova et al. (1985) reported that the ion chromatography method did not account for all the P in the sample (compared to colorimetry).

These same methods have been used to determine the B-content of BPSG and BSG.

2.29 CHROMATOGRAPHY

This is a technique for the separation and identification of components in a mixture using the interaction between the species in the mixture (the mobile phase) and a stationary material. The mobile phase may be a gas or a liquid. The liquid may be nonpolar or polar (ionic). Most often, the stationary phase is a resin, packed in a column, but there are other chromatographic methods (e.g., Miller, 1975). Separation of ionic species by this method is called ion chromatography (IC). It has been used for analyzing processing chemicals, processing residues, and materials incorporated into multilevel metal structures. They must be converted into a form suitable for IC; this may require dissolution, extraction from a surface, or concentration. The unknown is introduced at the top of the column followed by the eluent (an ionic solution) and both migrate through the column.

Both suppressor and nonsuppressor ion chromatographs are available commercially; a description of their operation can be found in Smith and Chang (1983). The affinity of the column material for the species in question determines the time it takes for each to reach the end of the column. The resulting chromatogram is a series of peaks, one for each component, separated by time intervals. The emerging species are identified and their concentrations measured by mass spectrometry, photometry, conductivity, absorption of radiation, etc.

2.30 OTHER ANALYTICAL TECHNIQUES

2.30.1 Neutron Activation

An example of this technique is the determination of the P-content of PSG. The films were irradiated using a thermal neutron flux and the beta activity from ^{32}P counted, using P-doped Si as a reference.

2.30.2 Inductively Coupled Plasma Atomic Emission Spectroscopy (ICP-AES)

In this technique, the material to be analyzed is vaporized or an aerosol solution of it is injected into a plasma and a spectrometer used to measure the peak intensities of the atomic emission lines in the plasma. The intensities are calibrated using standard solutions of the elements being analyzed. The method was improved by the use of internal standards (Cargo and Hughes, 1989).

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2.31 THERMOMETRY

2.31.1 Introduction

The temperature of the wafer during processing is a critical parameter. In reactive plasma-assisted etching it determines the etch rate and profile of both the substrate and the mask; in addition, too high a temperature causes mask distortion in any plasma-assisted etching process. In deposition, by CVD, PECVD, or sputtering, temperature influences the accumulation rate and, at times, the reaction mechanism and step coverage. Film properties such as structure, chemical reactivity (e.g., etch rate), stress, optical and electrical properties, and in many cases contaminant incorporation are a function of the temperature during deposition.

Many processes are carried out at low pressures where thermal conduction is poor. Thus, unless a suitable heat transfer medium is interposed between the wafer and its holder, there can be a substantial difference in temperature between them so that measuring the temperature of the holder is meaningless, making wafer temperature measurements necessary.

2.31.2 Measurement

Many devices for measuring wafer temperature have been suggested.

2.31.2.1 Thermocouples

Thermocouples, securely welded to the wafer, can give accurate results, e.g., in an evaporator (with a stationary wafer dome) or in rapid thermal processing or in a CVD reactor, but they are perturbed by an RF field. This effect can be eliminated by appropriate circuitry, but substrate heating through the thermocouple wires raises the temperature of the monitor wafer which is, therefore, not representative of any other wafer in the system.

2.31.2.2 Interferometers

A fiber-optic Mach-Zehnder interferometer was described by Hocker (1979). Another technique is the use of optical fiber Fabry–Perot interferometers (Yeh et al., 1990). Still another is infrared laser interferometry which measures the temperature-dependent optical path length from the front to the back of a wafer (Donnelly et al., 1992). The usefulness in a plasma was demonstrated by measuring the wafer temperature during etching of Si in Cl_2 in a helical resonator plasma reactor. A thermometer based on changes in reflectivity, at optical wavelengths, of metals and semiconductors has also been described (Guidotti and Wilman, 1992). Its use in a plasma was shown by measuring the temperature of product wafers during RF sputter deposition of SiO_2; it requires that a hole be drilled in the substrate holder so that the probe can see the back side of a polished wafer.

2.31.2.3 Pyrometry

Infrared pyrometry overcomes the RF problems, but must be used with caution. The detector requires calibration using an emission representative of the radiating surface. This infers that the emission must remain constant during processing. This can be accomplished for etching, using a special monitor wafer (Schwartz and Schaible, 1981), but is not useful for deposition. A two-color fiber optic IR detector (Koroychenko and Matthews, 1986) is independent of variations in emissivity but presents problems for measuring temperatures below 400°C.

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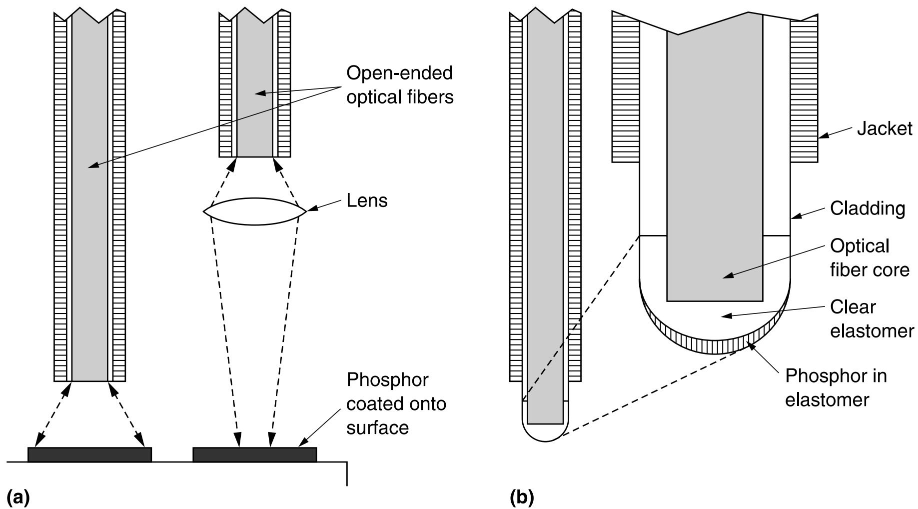

Figure 2.53 (a) Remote fluoroptic thermal probe; phosphor coated on surface of sample. (b) Contact fluoroptic thermal probe. (From Wickersheim, K. and M. Sun, *Res. Dev.*, 11/85, 114, 1985. With permission.)

2.31.2.4 Fluoroptic Thermometry

Probably the most widely used technique is fluoroptic™ thermometry, not only because of its ability to measure wafer temperature during plasma processing but also particularly because of the commercial availability of the apparatus (Luxtron). One measurement is based on the temperature dependence of the UV-light-induced optical emission of a rare earth phosphor. The first phosphors were europium-activated lanthanum or gadolinium oxysulfide. A high-vacuum port is required for the fiber optic probe which transmits the UV light to illuminate the phosphor which emits sharp lines whose relative intensities change with temperature; this temperature-related fluorescence is fed out through the probe to a detector. "By isolating two appropriate emission lines and determining the ratio of their intensities, a signal-independent measure of phosphor temperature can be obtained" (Wickersheim and Sun, 1985). It is used in one of two ways: (1) the phosphor is embedded into the tip of the probe which is either bonded to the wafer or held in close proximity to it (Egerton et al., 1982; Hussla et al., 1987; Castricher et al., 1987; Hess, 1993) or (2) the phosphor is coated on the back of the wafer and the tip of the optical probe placed against it (Nakamura et al., 1988). The basic configurations are shown in Figure 2.53).

Another system uses a "phosphor, magnesium fluorogermanate activated with tetravalent manganese; it is illuminated briefly with a pulse of blue light; the rate of decay of the fluorescence is measured and correlated unambiguously with temperature" (Wickersheim and Sun, 1985). However, the temperature measurement techniques require extra ports (often not available in production reactors) for probes, or preparation of monitor wafers so that they do not appear to be suitable for use during production processing, but are useful in the preliminary design experiments.

A more complete discussion of these techniques can be found in Herman (1996).

2.32 ELECTROCHEMICAL METHODS

2.32.1 Introduction

The interest in electrochemical methods is driven by the need to understand Cu electroplating and to monitor and control the plating baths.

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The plating reaction is driven by the difference between the interfacial potential $E = \phi_m - \phi_s$ (the difference in potential between the metal and the solution) and the equilibrium potential E_{eq}. The overpotential $\eta = E - E_{eq}$ is the difference between the potential of an electrode under the passage of current and the thermodynamic value.

The relationship between the plating current density (c.d.) i_s and η is, according to Butler–Volmer kinetics

$$i_s = i_o[\exp(a_a zF\eta/RT) - \exp(-a_c zF\eta/RT)]$$

where i_o = exchange c.d., a_a and a_c are the anodic and cathodic transfer coefficients, z = valence of the ion, F = Faraday constant, R = gas constant, and T = absolute temperature.

To drive plating at reasonable rates above i_o, large negative overpotentials are required. In this case the equation reduces to the Tafel limit:

$$i_s = -i_o \exp(-a_c zF\eta/RT)$$

or

$$\ln i_s = \ln i_o - (a_c zF\eta/RT)$$

2.32.2 Electrode Processes

There are several methods used to study electrochemical reactions (and determine i_o and a). One is measuring the Tafel slope from a plot of i vs. η. Another is the potentiostatic method in which the voltage is stepped or cycled as a function of time. In another (galvanostatic), it is the current that is stepped, cycled, etc. Description and discussion of them, however, are beyond the scope of this book. Details can be found in Damaskin (1967), Paunovic and Schlesinger (1998), and other standard texts on electrochemistry.

2.32.3 Plating Bath Monitoring and Control

Analyses can be done either offline or online. For offline analysis a sample aliquot is removed from the plating solution; for online analysis the apparatus is connected to the bath reservoir.

2.32.3.1 Inorganic Constituents: Cu^{2+}, Cl^-, H_2SO_4

Absorption spectroscopy can be carried out for Cu^{2+} (at λ = 814 nm) and for Cl^- (scattering at λ = 440 nm of AgCl colloidal suspension).

Titration can be carried out for H_2SO_4 with NaOH. Ethylene diaminetetraacetic acid (EDTA) is also used for the determination of the concentration of Cu^{2+}. EDTA chelates Cu^{2+}, releasing two H^+ for each Cu^{2+} chelated; the H^+ are titrated with NaOH. The titration for Cl^- by Ag^+ can also be followed by measuring the voltage between two electrodes. The endpoint is reached when the curve of potential vs. volume of $AgNO_3$ flattens out (Contolini et al., 2000).

2.32.3.2 Organic Additives (Suppressor, Accelerator)

2.32.3.2.1 Chromatography

The drawbacks of this method are the time required for analysis and the need to dispose of relatively large volumes of solution, particularly if frequent analysis is necessary.

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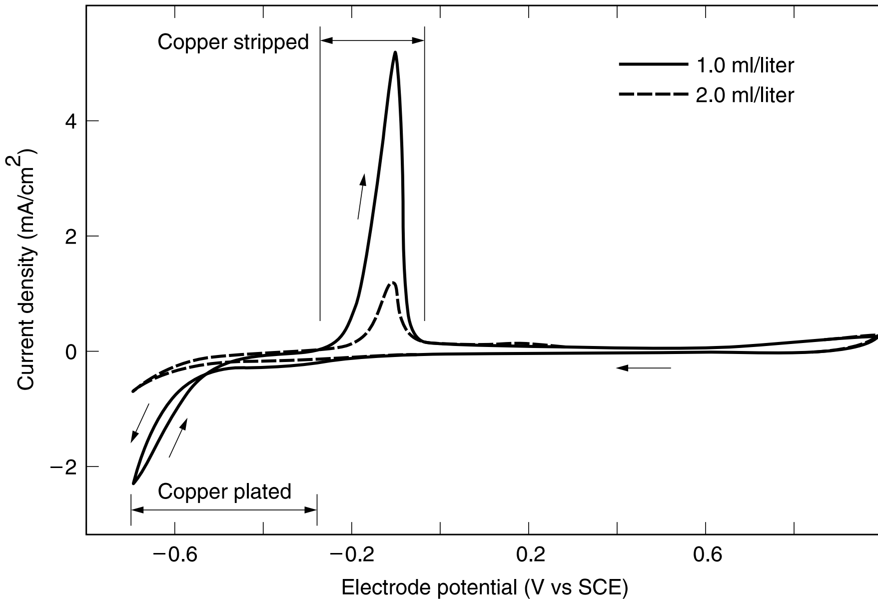

Figure 2.54 Cycic voltametric stripping (CVS). Steady-state linear sweep cyclic voltammograms: Cu plating baths. Upper curve: 1.0 ml/liter brightener; lower curve: 2.0 ml/liter brightener. (From Tench, D. and C. Ogden, *J. Electrochem. Soc.*, 125, 194, 1978. With permission of the Electrochemical Society, Inc.)

2.32.3.2.2 Cyclic Voltametric Stripping (CVS)

This technique, introduced by Tench and Ogden (1978), is a widely used electroanalytic method for determining the concentration of species. It is based on the effect of the additives on the rate of metal deposition. The current is measured as the potential of an inert rotating electrode is cycled in the bath as a function of time. During cycling, a small amount of metal is alternately deposited and stripped (i.e., dissolved anodically). The charge (area under the stripping peak) required to strip the metal is related to the deposition rate which depends on the concentration of the additives. A typical voltammogram of a Cu bath, with different concentrations of an additive, is shown in Figure 2.54. CVS can, therefore, be used to monitor the plating bath and to be incorporated into a control system. Since some bath components may affect the results in ways not directly affecting the deposition and stripping rates, matrix effects (Taylor et al., 1998), calibration procedures are often required.

2.32.3.2.3 Cyclic Pulsed Voltametric Stripping (CPVS)

This method was reported to mitigate the effect of contaminants that absorbed on a platinum electrode. The electrode is pulsed sequentially between plating, stripping, cleaning (in the O_2 evolution region to oxidized organic contaminants), and equilibrium potentials (at relatively negative potentials to reduce platinum oxides and condition the electrode). Thus, the electrode surface is kept in a reproducible state. The steady-state charge density for stripping the Cu deposit plated at constant potential for a given time is proportional to the additive concentration, unaffected by bath contaminants (Tench and White, 1985).

2.32.3.2.4 CVS + AC Voltammetry

In this technique an AC voltage (1 to 100,000 Hz) is superimposed on a DC CVS scan. A phase shift can be detected between the applied AC voltage and the measured AC current signals. The

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phase shift is related to the time it takes for a given surface-active species to cover the electrode. The concentration of a species is proportional to the magnitude of the current at a given phase shift (Contolini et al., 2000).

2.33 PLASMA DIAGNOSTICS

2.33.1 Optical Diagnostics for Plasma Processing

2.33.1.1 Introduction

These techniques are used to monitor a plasma within the reaction chamber (1) during process development, to study species formed from the reactants and etch products, the changes produced by variations in the processing parameters (e.g., power, pressure, mode of operation, etc.) which, together with physical examination of the processed wafers, leads to an understanding of the mechanism of the process and, ultimately, to its optimization, and (2) during processing, for detection of the end point, impurities, and particulates as well as for monitoring etch uniformity.

2.33.1.2 Optical Emission Spectroscopy (OES)

Many of the excited species formed in a plasma emit light; OES is used to detect and identify these excited (not ground-state) light-emitting species, which constitute a small fraction (~5%) of the species in the plasma. Not all activated species emit light; they may be deactivated by collisions or are metastables with no optical transitions.

OES is the most commonly used optical technique. A description of monochromators and light detectors, some typical spectra, and practical examples as well as some problems, such as light absorption by windows in the reactor, spectral resolution, second-order diffraction, etc., can be found in a review by Selwyn (1993).

2.33.1.3 Actinometry

Actinometry is the term applied to the process by which the concentration of the ground-state species (the chemical reactants) is derived from the optically detected species. It has been used in studying reaction mechanisms and in process evaluation. The emission intensity of a trace concentration of a second, nonreactive species is used to compensate for the emission intensity of the reactant species due, not to changes in the ground state population, but to changes in the electron density or energy distribution. A widely used application is the determination of the concentration of ground-state F atoms in a discharge containing a source of F (Coburn and Chen, 1980, 1981; d'Agostino et al., 1981a,b; Gottscho and Donnelly, 1984):

$$(F^*) = kf(F)$$

where (F^*) = number of excited species, (F) = number of ground-state F atoms, and kf = rate of electron-induced excitation.

A similar relation holds for Ar emission, the actinometer:

$$(Ar^*) = k(Ar)$$

If the two species have similar electron cross-sections, then

$$(F^*)/(Ar^*) \sim (F)/(Ar)$$

Since (Ar) is constant and known, by measuring the intensities of both F^* and Ar^* at the appropriate wavelengths, (F) is obtained and can be monitored as operating conditions are changed.

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In addition to the condition stated above about cross-sections, two other criteria must be met for the valid application of actinomtery: (1) both species must be produced by electron impact excitation of the ground-state species, and (2) deexcitation must be chiefly by light emission (Gottscho and Miller, 1984). Plasma reactions of interest for which actinometry is not valid are, for example, excited species production by electron-induced dissociation, $M_2 + e \rightarrow M^* + M$, and collisional quenching, $M^* + X \rightarrow M + X$.

2.33.1.4 OES for End-Point Detection

In the simplest cases, this may be based on (1) the consumption of reactant species: when the reaction is complete, their concentrations rise reaching a limiting value; or (2) the production of etch products: when the reaction is complete, their concentrations diminish and ultimately become zero. A uniform etch rate results in a sharp change in signal. Selwyn (1993) discusses in detail some of the factors that may influence the choice of an OES end-point strategy.

2.33.1.5 Laser-Induced Fluorescence (LIF)

This technique is used primarily in research. In LIF, a laser beam impinging on a plasma is absorbed by the plasma; this induces an electronic transition to an upper state. Subsequent relaxation and emission follow rapidly. LIF directly probes ground-state species; it is very sensitive and selective and is capable of high spatial resolution (Gottscho et al., 1983; Miller, 1986). When this technique is available, actinomtry is not needed. However, commercial reactors do not have the number of ports (three) required to use LIF.

High-resolution LIF measurement of the line profiles has been used to measure the ion and neutral temperatures in an ECR reactor (Nakano et al., 1991). Laser light scattering is used to detect particles generated in the plasma.

2.33.2 Plasma Probe Techniques

2.33.2.1 Introduction

Langmuir probes and microwave interferometers are used in the development of a plasma reactor or process to acquire basic understanding, but not as process monitors. They complement optical techniques but are, for the most part, research tools.

2.33.2.2 Langmuir Probes

These probes are considered intrusive, a source of contaminants and causing perturbations in a plasma. The theory used to interpret the current–voltage characteristics is relatively complicated. The probe consists of a small electrode in contact with the plasma; the simplest is a bare wire. The probe current is measured as its potential is increased as both positive and negative biases are applied to the probe. The ion density, electron temperature, floating potential, and plasma potential can be extracted from the measurements. Some of the many applications of Langmuir probe measurements are characterization of etching processes (e.g., Steinbruchel, 1983; Kopalidis and Jorne, 1992), of divergent ECR reactor configurations using inert and reactive gases (Forster and Holber, 1989; Shatas et al., 1992), and of a multipolar ECR reactor (Hopwood et al., 1990; Forster et al., 1992). Ashtiani et al. (1992) have described other probe configurations: the emissive (heated) probe which is said to have advantages for measuring the plasma potential in a magnetic field and a dual-probe assembly of both a conventional and an emissive probe. Herskowitz (1995) has a complete description of these probes.

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2.33.2.3 Microwave Interferometer

The microwave interferometer is a nonintrusive instrument. It measures the electron density along the path of the probing microwaves. The microwaves, 10 to 100 GHz, are split into two beams, one of which is sent through the plasma. This wave combines with the reference beam in a mixer; the two beams interfere and the result is a measurement of the phase shift caused by the plasma. The shift depends on the electron plasma density and the microwave frequency, unless the microwave frequency ($\omega/2\pi$) is greater than the electron plasma frequency, when the wave is reflected. This means that the method can be used when the electron density is in the range 10^9 to 10^{13}, and the device greater than 10 cm. One application of the method has been the characterization of an ECR reactor (Rossnagel et al., 1991). A detailed description can be found in Breun (1995).

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CHAPTER 3

Semiconductor Contact Technology

David R. Campbell, Revised by Catherine Ivers

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3.1 INTRODUCTION

The quality of the electrical contacts within an integrated circuit is critical to the performance of the chip. In view of both its technological importance and the many ways possible to form contacts, no other single area of circuit technology appears so extensively investigated, with the possible exception of gate oxides. As shown in Figure 3.1, there was the problem of the interaction between Al and Si in the earliest practical silicon contacts in which Al, and later AlSi, was the interconnection metallization.

An extensive annealing or sintering process was required to reduce the Si suboxide by formation of Al oxide, thereby providing a measure of direct contact between Al and Si. In the course of this annealing, Si would also diffuse into the overlying Al at weak points in the porous oxide that partially separated Al from Si. As the metallurgical limitations of this simple structure emerged, improvements were made by introducing platinum silicide (PtSi) as the first Si-contacting layer. Platinum was sputtered into a contact hole, formed in the overlying SiO_2 layer by patterning and etching, and then sintered. Platinum reacted readily with Si, more easily reducing the native oxide on Si and forming either ohmic or rectifying (Schottky barrier) contacts of consistently high quality. Reaction between the overlying Al metallization and the silicide again led to junction penetration, so that diffusion barriers were required to prevent interdiffusion and subsequent reaction. A typical contact structure including both silicide and a diffusion barrier is shown in Figure 3.2.

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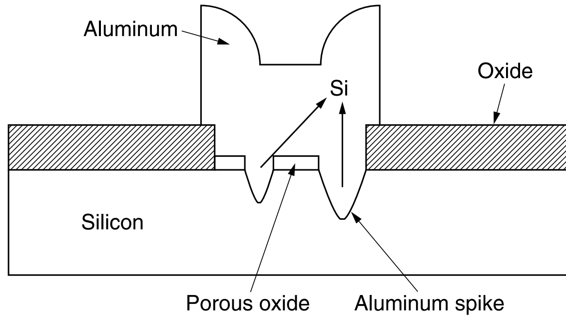

Figure 3.1 Typical early contact structure for Al metallization on Si that underwent Al spiking as a result of sintering. Note Al metal directly contacts Si surface.

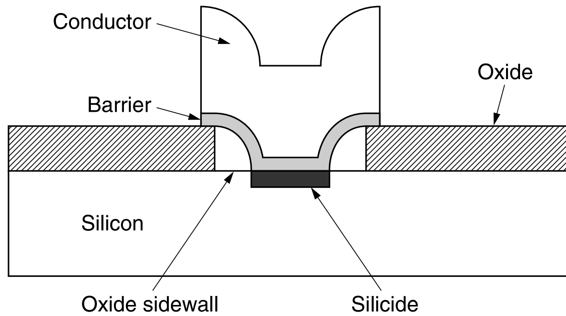

Figure 3.2 Contact structure complete with conductor, diffusion barrier, and silicide contact to Si. Sidewalls formed on the vertical surfaces of the contact opening provide for a smooth transition from the level of the interconnection to the surface of Si.

The purpose of the following review of contact technology is to chronicle the significant steps in developing state-of-the-art Si contacts. This review follows contact development, from the early beginnings of VLSI circuit technology (in the late 1960s) to the present. It draws from both patent and technical literature sources.

3.2 IMPORTANCE OF CONTACT TECHNOLOGY

Contact technology accounts for a substantial amount of the time and resources of chip interconnection technology, that is, the back end of the line (BEOL) processing, and the majority of the reliability problems. Problems with ohmic contacts range from early, fatal electrical malfunctions such as incompletely formed or electrically open contacts and penetrated junctions, etc., to slower emerging, but ultimately equally serious, metallurgical problems. (An electrically open contact is typically one in which the contact hole in the insulating layer is not etched deep enough to reach the silicon surface.) The latter may involve progressive kinetic phenomena such as interdiffusion, phase formation, and voiding, all of which can contribute to electromigration divergences and cause very resistive, and even opened, interconnects. Since Schottky diodes (rectifying contacts) are resistive structures as compared to ohmic contacts, they are less sensitive to some of the factors that contribute to excessive resistance in ohmic contacts. The presence of metallic oxides or other poorly conducting interlayer contaminants at the metal-to-metal interfaces that are included in the finished

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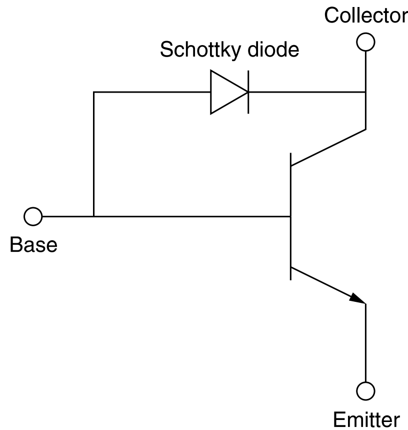

Figure 3.3 Circuit with Schottky barrier diode used as an emitter current clamp which prevents the transistor from reaching saturation and avoids subsequent decrease in switching speed. The diode is connected between the base and collector terminals. (From Tada, K. and J.L.R. Laraya, *Proc of* IEEE, 55(11), 2064, 1967.)

contact structure are examples of such. However, they are still highly sensitive to the condition of the metal–silicon interface and to any change in this interface during processing or operation. These conditions influence the barrier height of the diode (discussed later) and therefore its operating characteristics. Successful circuit applications of these diodes require stable *I–V* characteristics for the transistors with which they combine in various circuits. Figure 3.3 illustrates a typical use for a Schottky barrier diode (SBD) as a clamp on the emitter current port of a bipolar transistor. This prevents the transistor from going into saturation and thereby increasing the time required for switching between logic states.

3.3 ELECTRICAL ASPECTS OF SILICON CONTACTS

Two properties, barrier height, ϕ_B, and contact resistance, R_c, are essential parts of any discussion of the electrical characteristics of a metal–silicon contact. The physics of contacts appear in several texts (Grove, 1967; Muller and Kamins, 1977; Sze, 1969a) and a brief review is included to aid discussions of material choices for contacts. Barrier height, as the name suggests, is the energy or potential barrier for the passage of electrons between the metal contact and the single-crystal silicon device. Together with the width of the barrier (W), these two material parameters determine whether the contact is rectifying or ohmic in nature. Since the contacts are part of an electrical circuit, contact resistance directly influences circuit operation. Low R_c values provide small resistance–capacitance time delays (RC). For high R_c values, the reverse applies.

3.3.1 Barrier Heights

Figure 3.4 shows the energy band diagram for n-type Si. Contact with a metal layer through an intervening, insulating layer represents the most general case. However, in Figure 3.4, an interfacial layer is omitted in the interests of simplicity. This removes any potential influence of such an interfacial layer to the subsequent discussion, except to assume that electrons can flow through it and that the density of interface states, N_{ss}, is a property of the silicon surface and not of the metal or interfacial layer. The figure legend shows the symbols representing the relevant interface

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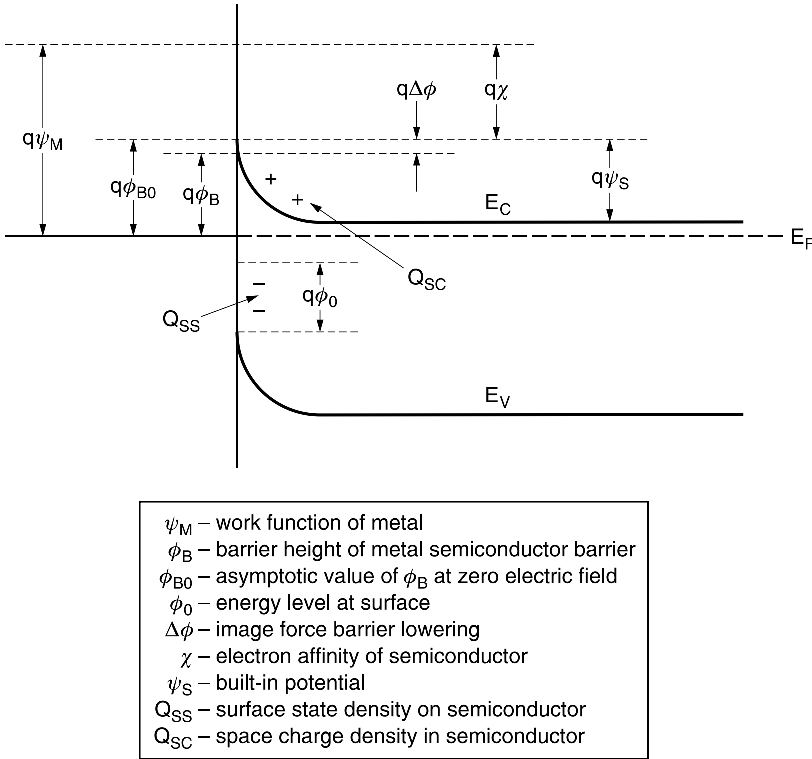

Figure 3.4 Energy band diagram for n-type Si in contact with a metal layer. (From Crowley, A.M. and S.M. Sze, *J. Appl. Phys.*, 36, 3212, 1965.)

energies (Crowley and Sze, 1965). Nicollian and Sinha (1978) have shown that the barrier height can be given by the following two expressions.

(A) True Schottky barrier ($N_{ss} = 0$, that is, no semiconductor interface states):

$$\phi_B = \phi_m - \chi - \Delta D\phi \tag{3.1}$$

For this case, the barrier height depends on the work function of the metal, ϕf_m, the electron affinity of the semiconductor χc, and $\Delta D\phi f$ is the image force barrier lowering. Since χc depends on the Fermi level, E_F, which in turn depends on the doping level, N_D, then barrier height in this regime should also depend on the doping level.

(B) Bardeen barrier ($N_{ss} = \infty$, that is, semiconductor interface states dominate):

$$\phi_B = E_g/q - \phi_0 - \Delta D\phi \tag{3.2}$$

This corresponds to most cases encountered in silicon contact technology in which the Fermi level is pinned by interface states at a level of $q\phi_0$ above the valence band edge. It should be noted that the work function of the metal does not appear here but the barrier height is also weakly dependent on doping level because ϕ_0 depends on χ, etc., as described for case (A) above. E_g, the remaining undefined parameter in the above expression, stands for the semiconductor (e.g., Si) band gap. For circuit applications, values of the diode barrier heights are either high, such as PtSi at ~0.9 eV, or low (actually mid-gap) such as TiW at ~0.5 eV. In the first instance, the application is

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typically a clamp to prevent a bipolar transistor from going into saturation, and in the second, it is a diode element in a logic circuit where its lower barrier height permits the diode to turn on at lower forward bias and, for the same reason, conduct higher currents through smaller contacts, i.e., use less Si real estate.

3.3.1.1 Data Analysis

Typically, experimental data are interpreted according to the expression:

$$J_f = A^{**}T^2\exp(-q\phi_B/kT)\exp(qV_f/nkT) \tag{3.3}$$

where J_f is the forward current density, A^{**} the effective Richardson constant, T the temperature, k the Boltzmann constant, q the electronic charge, V_f the forward applied voltage, and n the ideality (see below). The effective Richardson constant depends on the effective mass of the majority charge carrier and will therefore vary with dopant type, crystallographic orientation, type of semiconductor, etc. A typical value for A^{**} for electrons in metal–silicon systems is 110 A/cm^2/K^2 (Sze, 1969b). Measurements of I_f vs. V_f plotted as log I_f vs. V_f, typically yield two parameters, ϕ_B and n, according to the expressions

$$\phi_B = (kT/q)\ln(A^{**}T^2/J_0) \tag{3.4}$$

and

$$n = (q/kT)\partial V_f/\partial(\log I_f) \tag{3.5}$$

The barrier height is determined by finding the saturation current density, J_0, by extrapolating the linear portion of the log I_f vs. V_f plot to its intercept at zero forward voltage. The ideality, n, is introduced into Equation 3.3 to allow for a deviation from purely thermionic emission such as tunneling, bias dependence on ϕ_B, or recombination currents. The presence of any of these factors can increase n beyond its ideal value of unity. The ideality is determined from the inverse of the slope of a plot of log I_f vs. V_f as indicated by Equation 3.5.

A plot of barrier height vs. a weighted average of the work functions of Si and the metal overlayer, as initially calculated and reported by Freeouf (1981), is shown in Figure 3.5. Freeouf used the quantity $\phi_s \approx (\Psi_M\Psi_{Si}{}^4)^{1/5}$ to represent the barrier height of a hypothetical interfacial silicide layer presumed to exist between the indicated silicide phase and the single-crystal Si. Here ϕ_s is the barrier height of the silicide layer in contact with Si and Ψ_M and Ψ_{Si} are the metal and silicon work functions, respectively. This layer is intended to represent the interfacial layer structure and provides a reasonable fit to the data with the possible exception of the IrSi phase, which is somewhat more above the theoretical prediction, although it appears to lie within a few standard deviations of the trend line. Other authors, notably Andrews and Phillips (1975) and Ottaviani et al. (1980), have made similar correlations with structure–bonding characteristics such as the heat of formation of the silicide and the melting points of compositionally similar eutectic phases, respectively.

3.3.2 Contact Resistance

It is appropriate to start our discussion of contact resistance by examining the doping level (N_D) dependence of the conduction of the forward biased metal and n-type semiconductor interfaces. As shown in Figure 3.6, there are three distinct regimes corresponding to three mechanisms. In descending order of doping level, they are: (1) field emission or tunneling, where the excitation is

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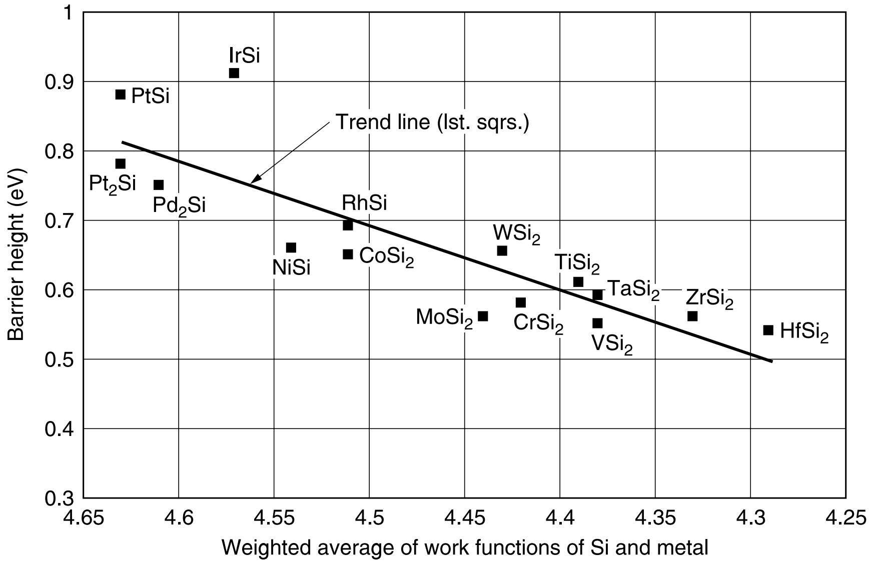

Figure 3.5 Plot of barrier height, ϕ_{bn}, vs. ~$(\Psi_M \Psi_{Si}^4)^{1/5}$, a weighted average of work functions of Si and the metal overlayer (indicated by subscript M). (From Freeouf, J.L., *J. Vac. Sci. Technol.*, 18, 910, 1981.)

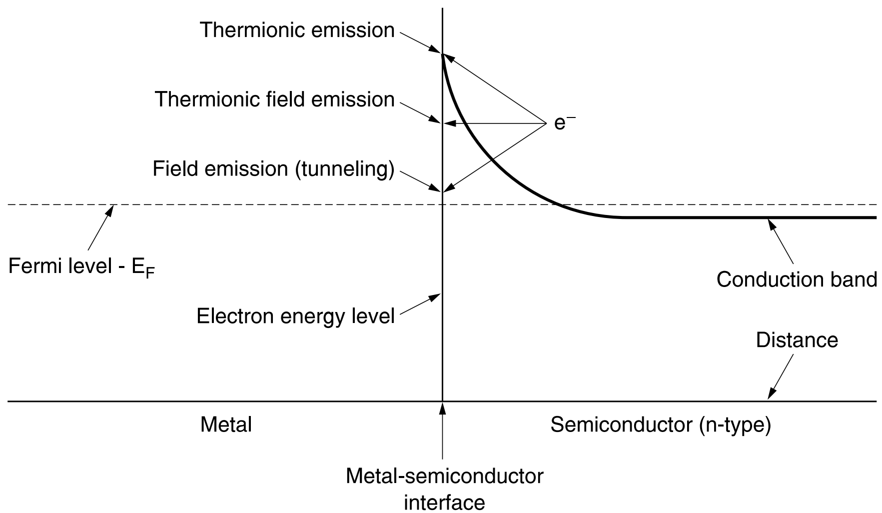

Figure 3.6 Three regimes of specific contact resistance (F, field emission; T-F, thermionic field emission; T, thermionic emission). (From Nicollian, E.H. and A.K. Sinha, *Thin Films: Interdiffusion and Reactions*, Poate, J.M., Tu, K.N., and Mayer, J.W., Eds., Wiley-Interscience, New York, 1978, p. 481.)

due to the electric field alone; (2) thermionic field emission, where conduction takes place by a combination of thermionic emission and tunneling; and (3) thermionic emission, where thermal excitation of electrons over the barrier is the predominant process. The silicon doping level controls which regime dominates, by determining the barrier width. Figure 3.7 shows the case of the field emission region, corresponding to high doping levels, as well as the two other regimes indicated above (Yu, 1970).

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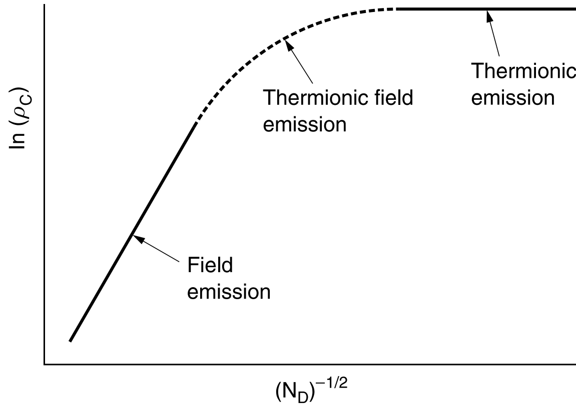

Figure 3.7 Specific contact resistance ρ_c as a function of doping level $N_D^{-1/2}$. Note that in the field emission regime, ρ_c has a linear dependence on $N_D^{-1/2}$, and in the thermionic emission regime, ρ_c is independent of $N_D^{-1/2}$. (From Yu, A.Y.C., *Solid State Electron.*, 13, 1189, 1970.)

The expression for specific contact resistance ρ_c is

$$\rho_c = (\partial V/\partial J)_{V\to 0} \tag{3.6}$$

where V is the applied bias and J is the forced current density. The units of ρ_c are Ω cm^2.

The corresponding expressions for the three regimes discussed above are as follows.

(1) Field emission (tunneling; highest N_D):

$$\rho_c \approx \exp(\phi_B/\hat{u}N_D) \tag{3.7}$$

where N_D is the doping concentration at the contact. In this case, conduction is entirely through the narrow barrier by quantum mechanical tunneling. This corresponds to the linear region of the curve at low values of $(N_D)^{-1/2}$ as plotted in Figure 3.7.

(2) Thermionic field emission (intermediate N_D):

$$\rho_c \approx \exp\{\phi B/vN_D[\coth(E_8/kT) - 1]\} \tag{3.8}$$

where E_8 is defined by the expression

$$E_8 = (qh/2)(N_D/m\varepsilon)^{1/2} \tag{3.9}$$

and q is the electron charge, h is Planck's constant, m^* is the effective mass of the charge carriers, and ε is the dielectric constant. In this regime, carriers flow past the barrier by a two-step process consisting of: (1) thermal excitation from the band level up to a higher energy level where the barrier width is narrow enough to support tunnel currents; and (2) tunneling through this narrower portion of the barrier. This corresponds to the dotted portion of the curve in Figure 3.7.

(3) Thermionic emission (lowest N_D)

$$\rho_c \approx \exp(\Phi B/kT) \tag{3.10}$$

Thermionic emission occurs when carriers fully surmount the energy barrier by thermal excitation. The progression of ρ_c behavior indicated by cases (1) to (3) above corresponds to decreasing

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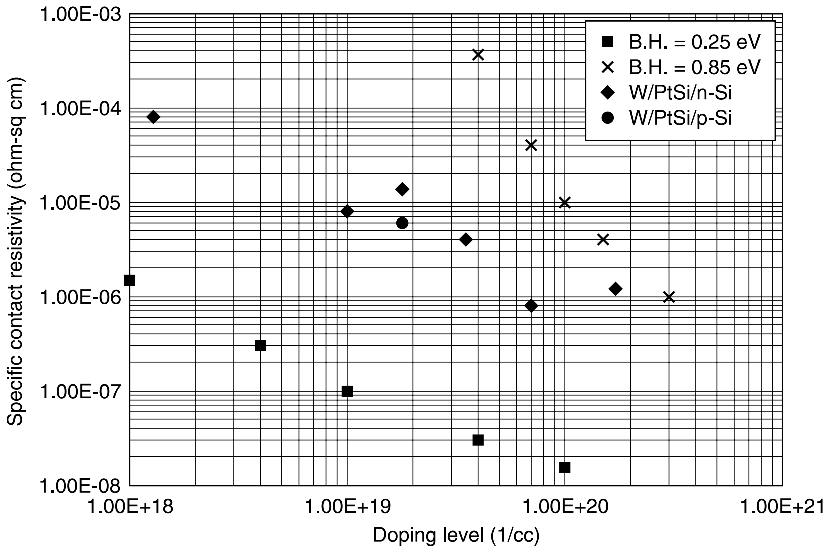

Figure 3.8 Plot of log(ρ_c) vs. log(N_D). Data points plotted as solid squares represent calculations from a tunneling model assuming a PtSi/p-Si contact, and crosses represent the calculations for PtSi/n-Si contacts. The experimental data are plotted as solid diamonds for W/PtSi/n-Si and as solid circles for W/PtSi/p-Si. Experimental measurements are much less sensitive to barrier height (0.25 eV on p-Si and 0.85eV on n-Si) than are model calculations because of the redistribution of dopants during silicide formation. The axes are labeled using scientific notation where, for example, 1E-08 is equivalent to 1×10^{-8}. (From Chang, P.H., *Heteroepitaxy on Silicon, Fundamentals, Structures and Devices,* H.K. Choi, H. Ishiwara, R. Hull, R.J. Nemanich, Eds., *Materials Research Soc. Symp. Proc,* 116, 471, 1988.)

concentration of dopant in Si, i.e., for case (1), the doping is heavy (N_D ~ 1020/cm^3), for case (3) it is lighter (N_D ~ 1017 to 1015/cm^3). In this instance, ρ_c is independent of N_D and corresponds to a constant value of ρ_c as indicated in Figure 3.7.

The values of ρ_c are typically determined at the highest obtainable dopant concentrations, that is, at the dopant solubility limit in Si, as the lowest possible ρ_c values are sought for optimal circuit operation. This corresponds to case (1) above and therefore ρ_c will depend strongly on the doping level. Consequently, concentration levels of dopants are usually reported along with the measured values of ρ_c. Another notable characteristic of the field emission regime is the absence of any significant temperature dependence. A plot of ln ρ_c vs. log N_D is shown in Figure 3.8 that includes both calculated and experimental values of contact resistivity vs. doping concentration for PtSi/Si interfaces (Nicollian and Sinha, 1978). Due to the large differences in the barrier heights of PtSi to n-Si (0.85eV) and p-Si (0.25eV), one anticipates a large difference in ρ_c, as indicated by the tunneling calculations. However, the actual data indicate the ρ_c values for n-Si and p-Si are nearly the same, that is, Equation 3.7 is not strictly obeyed.

It was eventually discovered (e.g., Witmer et al., 1982, 1983) that this occurs due to dopant redistribution or so-called "snow plow" effect that increases the effective dopant level in the immediate vicinity of the contact, thereby lowering ρ_c below the anticipated value. This is discussed again in a later section.

3.3.3 Berger Test Site

A Berger test structure (Berger, 1972) used for contact resistance measurements is shown in Figure 3.9. There are several ways to use this structure to determine contact resistance. Fortunately, for the DC case and where all contacts are physically identical, the method is relatively simple.

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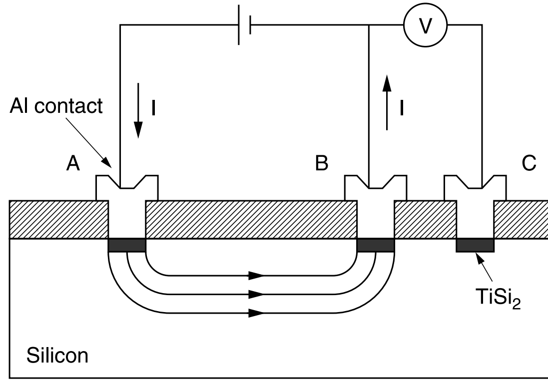

Figure 3.9 Berger test site for evaluating specific contact resistance. (From Berger, H.H., *Solid State Electron.* 15, 145, 1972.)

A reasonably good estimate of R_c can be obtained by measuring the resistance between contacts (a) and (b), R_{ab}, and between contacts (b) and (c), R_{bc}. Then the contact resistance of any one of the contacts is approximately given by

$$R_c = (R_{bc}L_{ab} - R_{ab}L_{bc})/2(L_{ab} - L_{bc}) \tag{3.11}$$

where L_{ab} is the distance between contacts (a) and (b) and likewise L_{bc} is that between (b) and (c).

However, due to the horizontal geometry of the test site, the value of R_c determined from Equation 3.11 will be somewhat exaggerated relative to a vertical geometry, e.g., a bipolar emitter contact, because of current crowding at the leading edge of the contacts. In the circuit configuration shown in Figure 3.9, the contact labeled "C" is shown being used to measure the potential of the trailing edge of contact "B." This quantity, referred to as the end resistance, R_e, provides another measure of the contact resistance but at a different, lower, current density. According to Berger, R_e is given by

$$R_e = V_{bc}/I_{ab}\ (I_{bc} = 0) \tag{3.12}$$

where V_{bc} is the voltage measured between contacts (b) and (c) under the condition of no or negligible current flowing between (b) and (c). I_{ab} is the current flowing between (a) and (b). Using transmission line theory, Berger showed that R_e is also given by

$$R_e = Z/\sinh(\alpha d) \qquad (3.12)$$

where α is

$$\alpha = \sqrt{(R_s/\rho_c)} \tag{3.13}$$

and Z, the characteristic impedance, is

$$Z = (1/w)\sqrt{(R_s\rho_c)} \tag{3.14}$$

Here, R_s is defined in terms of measurable quantities by the expression

$$R_s = w(R_{ab} - R_{bc})/(L_{ab} - L_{bc}) \tag{3.15}$$

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where w is the length of the contact, i.e., the dimension into the plane of Figure 3.9 (not shown). By using an iterative approach, these expressions allow one to calculate the specific contact resistivity ρ_c.

3.4 MATERIAL ASPECTS

Proper selection and control of material properties are essential for a successful contact technology, that is, for forming an electrical contact with acceptable electrical characteristics. Relative to the more refractory semiconductors (Si, polysilicon (poly-Si)) and inorganic dielectrics (SiO_2 and Si_3N_4) used to build Si devices, the metals used for contacts and interconnections are quite reactive at BEOL processing temperatures of 400 to 450°C. Strategies that enhance the stability of contacts include alloying, layering of materials in a particular sequence, utilizing diffusion barriers, etc. These strategies are employed to retard rates of reactions and interdiffusion between the contact metals and Si to suitably low values, so that Si contacts and the contacted devices remain functional over the projected lifetime of the chip. Control of the kinetics of metallurgical reactions is therefore key to building high yielding and reliable circuits. A typical FET contact structure that might be used in modern integrated circuits is shown in Figure 3.10. This structure includes many advanced features such as self-aligned silicide (so-called “salicide”) device contacts and also self-aligned TiN barriers formed by nitrogen implantation into $TiSi_2$.

3.4.1 Aluminum–Silicon Metallurgical Reactions and Effect on Barrier Heights, Contact Resistance, and Leakage

Earlier reviews (Rosenberg et al., 1978; Lau et al., 1978) discussed the related phenomena of Al spiking or penetration and solid-state epitaxial regrowth of Si in contact regions. Because of the appreciable solid-state solubility of Si into Al, as evident from the Al–Si phase diagram in Figure 3.11 (Murray and McAlister, 1984), sintering of pure Al in contact with Si will cause dissolution of Si into Al until the solid solubility requirement is met. Si reacts with Al locally, at weak points in a residual oxide film on the Si surface. As Si dissolves and migrates into Al, Al stays in contact with the recessing Si surface to maintain minimal interfacial energy. This results in penetration of Al, taking the form of a spike or inverted pyramid. The detailed morphology will depend on the crystallographic orientation of the Si wafer. Both Totta and Sopher (1967) and Lane (1970)

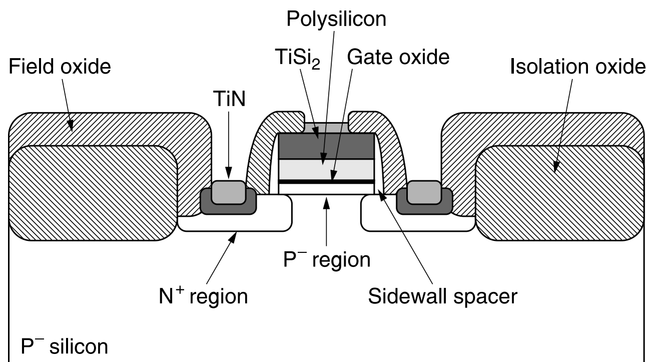

Figure 3.10 Advanced contact structure featuring self-aligned source and drain, self-aligned silicide ($TiSi_2$) for ohmic contacts, and self-aligned TiN diffusion barriers to prevent Al spiking. The TiN barriers are formed by ion implantation of N into $TiSi_2$. (From Chin, M.-R., G. Warren, and K.Y. Liso, U.S. Patent 5,389,575, 1995.)

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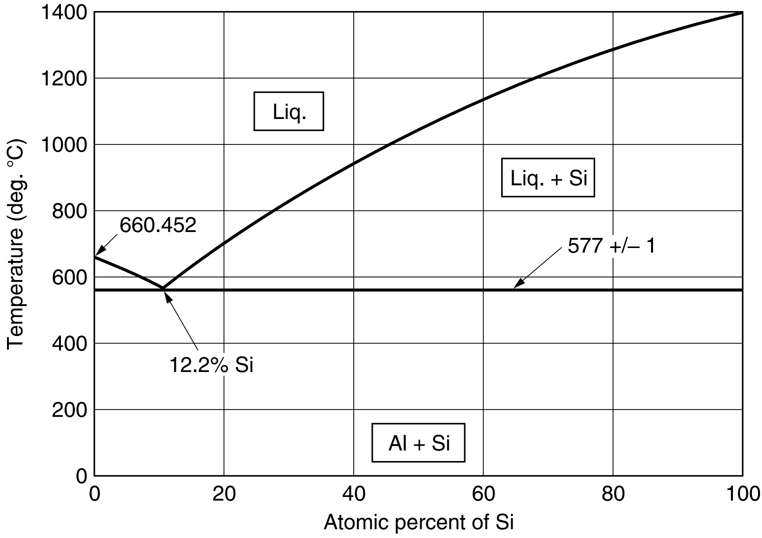

Figure 3.11 Aluminum–silicon phase diagram. (From Murray, J.L. and A.J. McAlister, *Bull. Alloy Phase Diagrams*, 5, 74, 1984.)

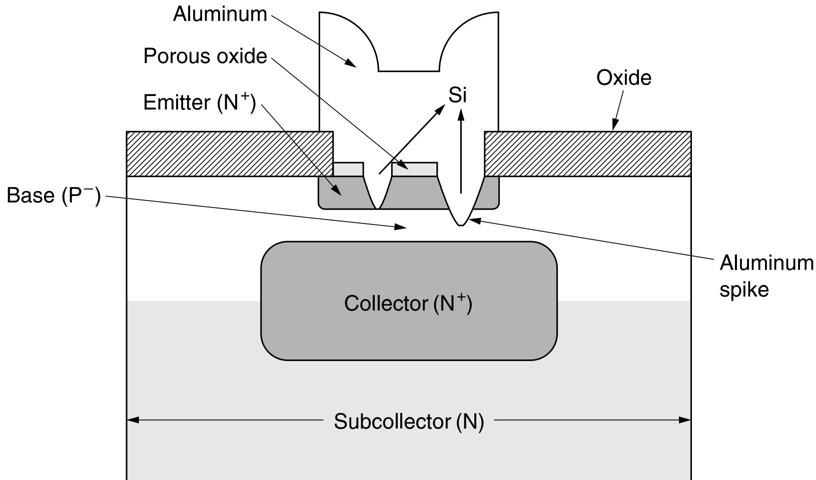

Figure 3.12 Incipient shorting of emitter to collector by penetration of Al spike through base.

have given early accounts of Al penetration. A schematic of these effects on an early device structure is shown in Figure 3.12.

One example of the serious consequences of penetration for bipolar devices is shorting of the emitter to the collector, that is, penetration of the metallic element through the base region of a bipolar transistor, as shown in Figure 3.12. Also, upon cooling of a sintered contact, Si can regrow on the contact surface as hillock-like structures, because the amount of Si dissolved in Al at sintering temperatures exceeds the solubility limit upon cooling. With reference to Figure 3.13, it is instructive to consider the Al contact as divided into two regions: (1) the Al volume that lies at or within one diffusion length from the Si interface, that is, within $\sqrt{D_{Si}t}$, where D_{Si} is the diffusivity of Si in

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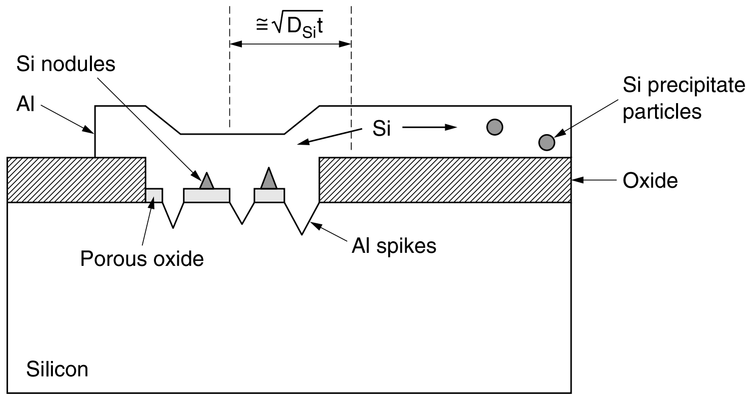

Figure 3.13 Formation of Si nodules and precipitates in Al metal lines. For distances of less than one diffusion length (of Si in Al), the preferred nucleation morphology is as nodules of Si at the Al/Si interface. For distances greater than one diffusion length, the preferred nucleation morphology is as Si precipitate particles within the Al metal.

Al at the sintering temperature and t is the duration of the sintering, and (2) the remainder of the Al land that lies beyond $\sqrt{D_{Si}t}$.

In region (1), excess Si was observed to precipitate into epitaxial, Al-doped, rectifying structures of p-type Si on n-type Si surfaces, but in region (2), Si precipitates within the Al as small crystallites, and preferably near a free surface (McCaldin and Sankur, 1972). The presence of this Al-doped, p-type Si on the contact surface in region (1) increases the barrier height and therefore the I–V behavior of Schottky diodes. Early reports of these electrical effects are Chino (1973), Basterfield et al. (1975), Card and Singer (1975), Card (1976), and Reith et al. (1976). Rosenberg et al. (1978) reviewed the effects of the duration of sintering and of aging of sintered diodes. Sintering produced changes in barrier height and ideality, as shown in Figure 3.14 and Figure 3.15.

The changes were interpreted as due to the formation of penetration pits followed by the formation of a p-type layer on the contact. And as noted earlier, the p-type layer caused the observed increase in the barrier height. Aging of contacts at temperatures lower than the sintering temperature lowered the barrier height because aging causes migration of the Al dopant in the regrown Si to internal sinks such as dislocations where they were no longer electrically active.

Inoue et al. (1976) observed the migration of Si into overlying Al lands directly by using the methods of electron microprobe analysis combined with Auger spectroscopy to investigate both lateral and through-the-thickness distributions of Si in the Al. They found a Si-rich Al layer within the Al immediately above the contact area. They also found that Si within the Al lying over SiO_2 (outside the contact region) had relatively constant concentration of Si (using through-the-thickness profiling). Lateral profiling showed a high Si concentration at the edges of the contact holes. Increased sintering time increased penetration, as expected. Blair and Ghate (1977) conducted subsequent studies of the influence of vacuum ambients on Si contacts. They concluded that common vacuum chamber contaminants such as H_2O, O_2, and CO, at pressures up to 5×10^{-7} torr (6.7×10^{-5} Pa), did not degrade the electrical characteristics of evaporated Al/Si contacts. A comparison of several methods for reducing poly-Si dissolution and contact resistance at Al/poly-Si interfaces led Naguib and Hobbs (1978) to advocate use of Al–2 wt% Si metallization to saturate the Al sink, as it were, with Si solute. They suggested that alloying was the most practical technique to minimize the undesired effects.

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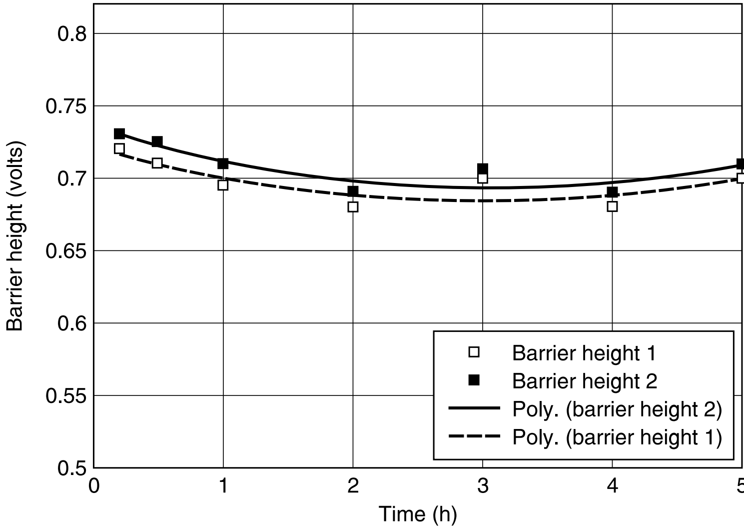

Figure 3.14 Effect of sintering time on barrier height of a Schottky barrier diode device. There are two sets of data displayed, indicated as 1 and 2 in the legend. The "poly" labels in the legend indicate that the drawn curves are least squares fit to second-order polynomials. (From Reith, T.M., *Appl. Phys. Lett.*, 28, 152, 1976.)

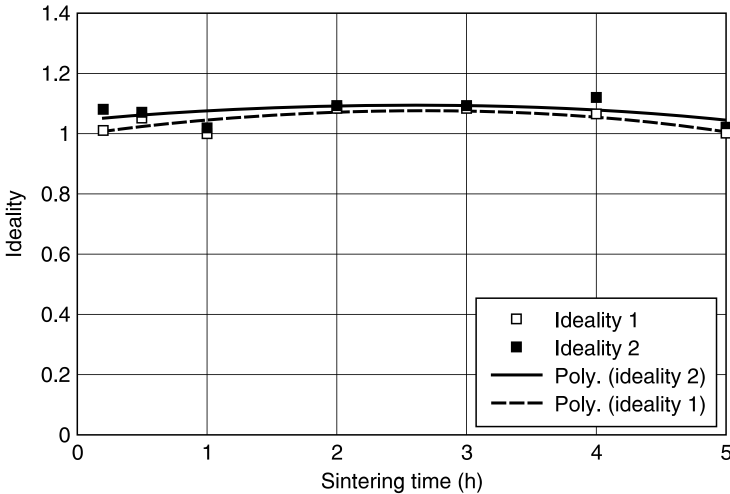

Figure 3.15 Effect of sintering time on ideality of a Schottky barrier diode device There are two sets of data displayed, indicated as 1 and 2 in the legend. The "poly" labels in the legend indicate that the drawn curves are least squares fit to second-order polynomials. (From Reith, T.M., *Appl. Phys. Lett.*, 28, 152, 1976.)

Faith and Wu (1984) undertook to eliminate hillocks on the metal surfaces by using fast heat pulses. They sintered Al–1% Si metallizations using 5-second pulses at 490 to 540°C and compared the results with those obtained by annealing in a furnace at 425°C for 30 minutes. Depending on the temperature of the heat pulse, the contact resistances and diode leakages were comparable to those obtained using standard furnace annealing, but did not result in undesired hillocks. Wu (1985) also claimed to achieve reduced penetration and provide diodes with excellent characteristics by using rapid pulse heating. Sintering resulted in two orientations for the epitaxial growth of

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Al spikes in the metallurgical system consisting of Al–1% Si/TiW/Si (Chang, 1988). These were: (1) Al[011]//Si[*1*23] and Al(200)//Si(1*1*1); and (2) Al[001]//Si[*1*12] and Al(200)//Si(1*1*1) (italics indicate the negative indices). Using finite element methods, Ohdomari and Takahashi (1990) have calculated the spatial distribution of compressive stress occurring in the Al in contact regions. Upon simulated heating, they found the stress to be highest at corners, i.e., at the contact openings and edges, due largely to thermal expansion mismatch between Al, SiO_2, and Si. The authors then argued that these compressed areas will be sites for greater Si precipitation upon cycling back to room temperature. They based this prediction on a model of Si particle precipitation that was derived from classical nucleation theory and incorporated the Gibbs–Thompson effect. The results of the model were that the Si solubility was higher in the compressive stress field existing at sintering temperature, but as the sample cooled and the stress reduced, the Si accumulated in the compressive field could migrate elsewhere and cause a higher growth rate of precipitates.

Hirashita et al. (1988) observed the solid-phase epitaxial growth of Si at contact holes through an Al–Si alloy directly by transmission electron microscopy. They obtained clear analytical evidence for the mechanisms previously inferred from electrical and postsintering structural analysis. Since attempts to remove native oxides from the bottom of contact holes are never totally successful, Nogami et al. (1994) suggested an alternative procedure based on their observation that a very thin silicon oxide film can actually prevent Si solid-phase epitaxial growth onto the Si contact. They could obtain low contact resistance for both p- and n-type Si by sputtering AlSi onto the thin oxide surface. Apparently, the oxide film was thin enough to allow sufficient tunneling current necessary for an acceptable contact resistance. A difficulty of this process is the ability to form, consistently, native oxides that are sufficiently thin for the tunneling currents but at the same time thick enough to suppress Si(Al) regrowth. Additionally, if the oxide layer is *too* thick it will form a current-blocking interface.

A novel method of reducing the formation of Si nodules at the Al/Si interface was patented by Wong (1992); this involved modification of grain size within the thickness of the contacting metallization by changing sputtering conditions. In the simplest embodiment, a bilayer of Al was formed that had relatively large grains for the portion directly on Si, and smaller grains in the next Al layer. This structure created a divergence in the diffusion flux of Si in Al by abruptly reducing the density of high-diffusivity paths in the layer next to Si. The flux divergence was responsible for Si precipitation on this interface, instead of at the Si surface. Also, a thin layer of interfacial oxide between the two Al layers created by the interrupted deposition would have a similar effect.

Jaffe and Penton (1979) patented a method of contact formation that involved amorphizing the c-Si layer by ion implantation. An Al layer could then be deposited on the a-Si to form the contact structure. The amorphization and doping of the Si could be accomplished in one step by using ion implantation of As at an energy of 180 keV and a dosage of $1015/cm^2$. An advantage cited for this approach is the reduction of pitting because of the lower accumulation of Si in Al due to the amorphization of Si. It appears likely that the success of this approach stems from a decreased rate of dissolution of Si, since, from a thermodynamic viewpoint, the higher energy state of amorphous Si vs. crystalline Si would favor more dissolution into Al instead of less.

Chen et al. (1981) described two ways to improve contact stability to submicrometer poly-Si which involved: (1) use of W/Ti contact metallization; and (2) use of laser annealing to sinter Al/poly-Si contacts. The ρ_c values of the W/Ti contacts were comparable to furnace-annealed Al/poly-Si but interdiffusion was avoided. Resistance values for the laser-annealed Al/poly-Si were the lowest of all and there was essentially no atomic intermixing. For both the furnace-annealed Al and W:Ti contacts, ρc values of 2.4×10^{-5} Ω cm^2 were obtained, but for the laser-annealed Al contacts, the much lower value of 3.6×10^{-6} Ω cm^2 was obtained. The P-doping level in the poly-Si film was approximately $10^{19}/cm^3$.

With respect to Schottky contacts, Bhatia et al. (1976) patented a novel method of increasing ϕ_B. They produced Si-rich structures with improved electrical characteristics by reacting the metal film

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with a poly-Si layer at an elevated temperature and then cooling quickly (quenching) from the reaction temperature back to room temperature. In the example given, AlCu/poly-Si/Si diodes yielded a ϕ_B value varying from 0.72 to 0.84 eV, depending on the quench rates. Typical AlCu/Si diodes on n-type Si have values of ϕ_B ranging from 0.68 to 0.72 eV.

In the same vein, Ar^+ ion bombardment of Al/Si contacts redistributes residual SiO_x and this reduces spiking of Al into Si by creating a uniformly reacting surface. Thermal annealing at 350°C increased the average value of ϕ_B from 0.49 eV, postimplant, to 0.64 eV after annealing, which is close to the undamaged value of 0.69 eV. Alpha particle channeling provided direct evidence that very little damage remained after annealing. Ohta et al. (1989) used DLTS to investigate defects associated with evaporated metal contacts to Schottky diodes. They discovered defect levels at 0.16, 0.14, and 0.12 eV below the conduction band and identified wet chemical etching as the origin of the defects. Supporting evidence came in the form of: (1) an increase in the concentration of defects with the amount of Si removed by chemical etching; and (2) a decrease in one of the levels (0.14 eV) with increasing etch rate.

Observations made by Card (1976) showed that measured values of ϕ_B of Al on Si depended on the details of the surface conditions and the heat treatments. For example, if oxides of 20 Å thickness are present, then the value of ϕ_B on p-type Si can be as high as 0.7 eV and on n-type Si as low as 0.5 eV. Card further showed that heat treatments of at least 300°C are required for reproducible values of ϕ_B of 0.7 and 0.5 eV for n- and p-type Si, respectively. With increasing temperature of sintering (up to 550°C), the value of ϕ_B of n-type Si could reach 0.9 eV and that of p-type could drop to 0.35 eV. The changes in ϕ_B were ascribed to two mechanisms: (1) the removal of positive charges from the oxide; and (2) the metallurgical reactions between Al and Si.

Yaspir et al. (1988) used a novel partially ionized beam (PIB) technique to deposit Al on n-Si to form Schottky contacts. Highly uniform characteristics of diodes across a 3 inch wafer were found together with a much reduced pit formation on Si. The energetic Al flux created by the accelerating potentials in the PIB deposition system was assumed to help remove native oxide from the Si surface, thus creating a more intimate Al/Si interface.

3.4.2 Silicide Formation

Silicides are important for forming Si contacts largely due to their ability to (1) reduce residual oxides on Si, thereby providing the contact area with spatially uniform electrical properties, (2) form discrete, intermetallic phases that bind metallic components in thermally stable compounds, thereby preventing junction poisoning from metal diffusion, and (3) provide a better conductor than doped c-Si or poly-Si. Summary accounts of the kinetics of silicide formation appeared in earlier reviews (Tu and Mayer, 1978; Murarka, 1983). Among the popular silicides formed by metal–silicon reaction, discussed here, they can be divided into two groups as shown in Figure 3.16.

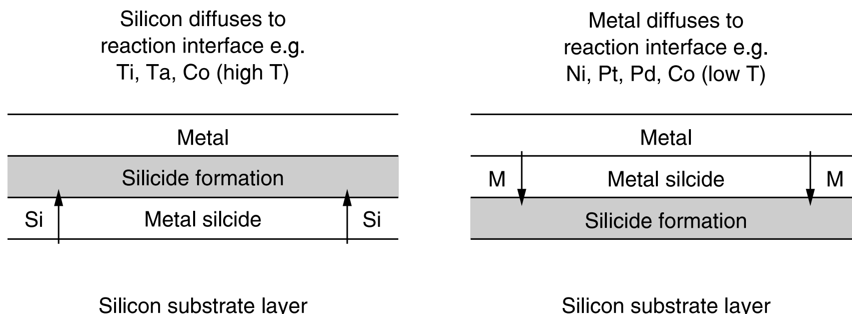

Figure 3.16 Silicide formation mechanism: metal diffusing to reaction interface, Si diffusing to interface.

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The silicide formation mechanism either by dominant metal diffusion or Si diffusion influences the process details (e.g., avoid encroachment). The reader may consult the sources mentioned above for excellent fundamental treatments of the silicide phase formation process. Included here is a brief discussion of silicide formation, but mainly in the context of contact formation.

3.4.2.1 Platinum Silicide

Amouroux and Pestie, 1971, provided one of the early accounts of the use of PtSi for device contacts by observing the formation of these layers on Si semiconducting devices. The study was part of the development of a PtSi/Mo/Au contact metallization for a microwave transistor. They pre-sputtered the Si surface to remove contamination, deposited a 100 to 500 Å layer of platinum by sputtering, and formed the PtSi layer by annealing at 450 to 550°C, which was below the Si–Pt eutectic point. Then they etched (away) the unreacted Pt using aqua regia. Rand and Roberts (1974) pointed out that the resistance of PtSi to the etch was provided by a thin, approximately 100 Å, layer of SiO_2 that forms on the surface of the silicide during annealing (Figure 3.17). Removal of this oxide would expose the PtSi to an etchant that could readily dissolve it, so its existence is essential to the process.

3.4.2.1.1 PtSi Application: Bipolar Emitter Contacts

Emitter contacts (unlike base or collector contacts) are designed to minimum features and typically have the smallest areas. It is important to avoid any disruption of the dopant profiles and emitter–base junction during emitter contact formation. For these and other reasons, most of the contact research for bipolar devices has been on emitter contacts.

Partly for historical reasons, and partly for its relatively low formation temperature, which would not alter the precisely tailored base widths of npn bipolar transistors, PtSi phases have been extensively used as contacts to bipolar devices. This practice continued with the introduction of poly-Si emitters which were poly-Si films that overlaid the c-Si contacts. They were used as solid-state diffusion sources for forming the emitter concentration profile. This involved the sequence of As ion implantation into the poly-Si followed by a thermal drive-in of As into the underlying c-Si. To better quantify the properties of the PtSi/poly-Si interface, Huang et al. (1988) did a detailed study of the contact resistance of PtSi to As-doped poly-Si in which they correlated the value of ρ_c to the fraction of As dopant that was electrically active. Hall measurements determined the carrier concentrations and established correlations between ion implant dose parameters

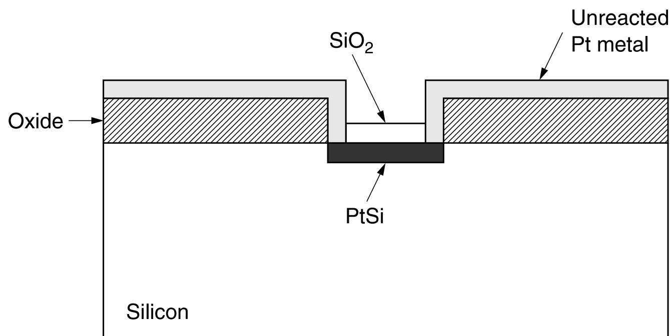

Figure 3.17 Formation of PtSi by blanket deposition and sintering of Pt on a contact structure. A layer of SiO_2 protects the silicide from removal during strip of unreacted Pt in aqua regia etch.

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and SIMS determined the As doping level. Postimplant annealing varied the fraction of carriers that were electrically active. Their experimental data are shown in Figure 3.18, where, though convoluted with other contact physics-related phenomena, the ability to increase ρ_c by charge carrier trapping at grain boundaries is evident through comparison with c-Si data.

The As concentration used in this study ranged from 8×10^{19} to $2 \times 10^{21}/cm^3$. Rapid thermal annealing (RTA) activated a higher fraction of the implanted As, producing ρ_c values as low as $7.5 \times 10^{-8}\ \Omega\ cm^2$ for samples annealed at 1050°C, as compared to $8.4 \times 10^{-7}\ \Omega\ cm^2$ for conventional furnace annealing.

3.4.2.1.2 PtSi Application: Schottky Barrier Diode (SBD)

An early SBD process patent cited the use of Pt_2Al as a Schottky barrier, and not one of the three ports of a transistor, but as an independent device for incorporation in a circuit as a diode (Magdo, 1975). The structure (not shown) contained a doped Si region of 1018 atoms/cm^3, a deposited layer of Pt that was heated to form PtSi, and a layer of Al on the PtSi which was sintered at 400 to 550°C for 1 hour. The latter sintering step reacted Al and PtSi to form the intermetallic Pt_2Al phase. The patent also cited using PtSi as an ohmic contact but with the necessary higher doping level ($> 10^{18}$ atoms/cm^3). In a subsequent and related patent, Magdo and Magdo (1976) described a dielectrically isolated Schottky barrier structure. Pockets of Si surrounded by electrically isolating regions of SiO_2 were covered by a second dielectric. This can be a composite layer of Si_3N_4 and SiO_2 or Si_3N_4 which is then opened to expose the Si islands. Pt deposited on the Si was then sintered to form PtSi and overcoated with Al to provide an interconnection. The resulting structure is shown in Figure 3.19.

Figure 3.18 Effect of charge carrier trapping by grain boundaries in poly-Si. PtSi contact resistivity is plotted as a function of As-doping concentration for both single-crystal Si and poly-Si. The increased resisitivity of the PtSi/poly-Si structures is attributed to charge carrier trapping by grain boundaries. Rapid thermal anneals of PtSi/poly-Si samples were as follows: △, 1000°C for 10 min; □, 1050°C for 30 sec; ○, 1200°C for 10 sec. The axes are labeled using scientific notation where, for example, 1E-08 is equivalent to 1×10^{-8}. (From Huang, H.-C.W., R. Cook, D.R. Campbell, P. Ronsheim, W. Rausch, and B. Cunningham, *J. Appl. Phys.* 63, 1111, 1988.)

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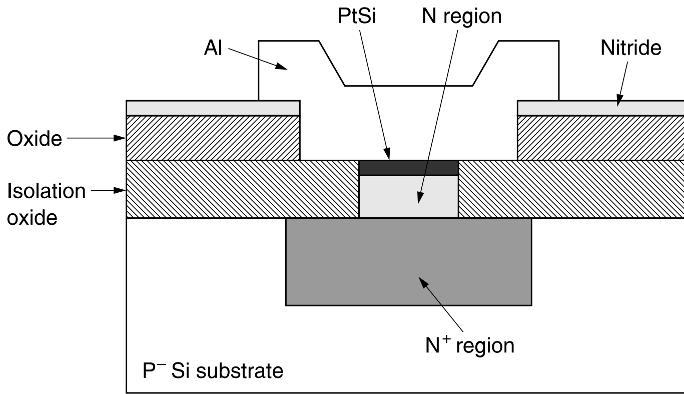

Figure 3.19 Dielectrically isolated Schottky barrier diode formed with PtSi. Note the PtSi region covers the N region completely, to prevent a parasitic Al/Si contact forming at the periphery. (From Magdo, I.E. and S. Magdo, U.S. Patent 3,956,527, 1976.)

3.4.2.2 Palladium Silicide

Ho et al. (1982) investigated the metallurgical stability of Al/Pd_2Si/Si contacts by mapping the phase diagram of Al–Pd–Si at 400°C. Reaction kinetics relating to rates of Pd_2Si decomposition and Al reaction and penetration were examined for both polycrystalline and epitaxial Pd_2Si. Changes in the electrical characteristics were explained by Si regrowth from silicide dissociation. The contact resistance of Mo/Pd_2Si/Si structures to both pn^+ and np^+ junctions using a Kelvin four-terminal method was reported by Singh et al. (1986). They reported values of ρ_c of 0.28×10^{-6} to 0.31×10^{-6} Ω cm^2 for p^+ contacts that were 1.3 μm in diameter and the corresponding n^+ contacts had ρ_c values ranging from 0.15×10^{-6} to 0.19×10^{-6} Ω cm^2. The authors further studied the thermal stability of these values and suggest the use of these contacts for VLSI provided temperatures of 475°C are not exceeded.

3.4.2.3 Titanium Silicide/Titanium Nitride

$TiSi_2$, $CoSi_2$, and NiSi are silcides that are predominantly used or being considered for CMOS applications. From an electrical point of view, contact resistivity and sheet resistivity (gate electrode) are important in the choice of a silicide. From a process/physical point of view, low Si consumption (for shallow devices) and reaction temperature to achieve desired phases (low resistance) and stability of phases in the presence of Si and oxygen are important. $TiSi_2$ was once undisputed as the contacting metal for MOSFET structures because of its high-temperature stability, its compatibility with self-aligned processing, its relatively high conductivity when compared to other silicides, and its compatibility with TiN barriers. $CoSi_2$, considered promising by Murarka as early as 1998, is increasingly used in CMOS logic applications at 250 nm and below. This stems from less sensitivity to processing conditions below 900°C and greater thermodynamic stability relative to $TiSi_2$. $CoSi_2$ is discussed more fully in Section 3.4.2.4.

The two most common phases of $TiSi_2$ are C49 (low temperature (625 to 675°C), higher resistivity (60 to 65 μΩ cm)) and C54 (high temperature ($\geq$800°C), lower resistivity (10 to 15 μΩ cm)) In addition, it is possible to convert a portion of the silicide layer to the nitride, providing a barrier against reaction with Al. A relatively common method for doing this is annealing of a $TiSi_2$ layer in the presence of NH_4 vapor as shown schematically in Figure 3.20.

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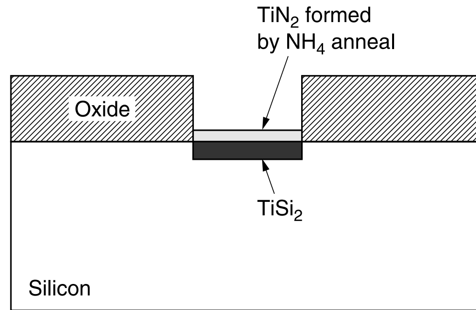

Figure 3.20 Nitriding of $TiSi_2$ contact by sintering in NH_4 atmosphere.

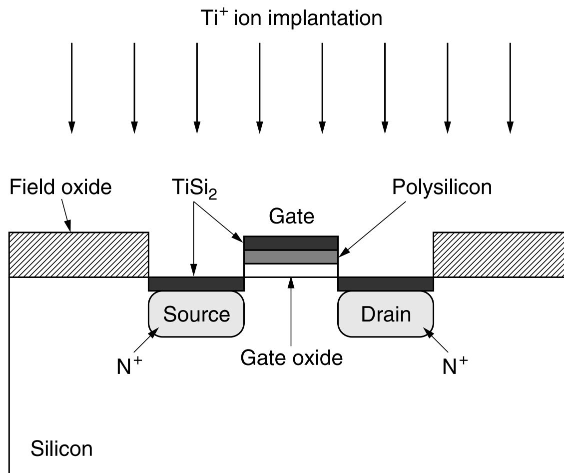

Figure 3.21 Self-aligned $TiSi_2$ contact structure formed by ion mixing. (From Ye, M., H. Lin, G. Fei, P. Tsien, J. Zhang, and S. Yin, *Vacuum*, 39, 231, 1989.)

Norstroem et al. (1983) showed that bilayers of TiN/Ti deposited by magnetron sputtering will react to form $TiSi_2$. In the same step, the TiN layer is transformed from its deposited composition to the true stoichiometric compound, TiN. The nitride layer is an effective diffusion barrier against Al up to 550°C. Ye et al. (1989) described a novel technique to form shallow junctions with low-resistance silicide contacts in MOSFETs for VLSI. It involved first siliciding the gate and source–drain region in a self-aligned manner and then implantation of Ti through the metal layer to transform the Si into $TiSi_2$ by ion mixing. Figure 3.21 shows schematically this self-aligned process. A more general discussion on self-aligned silicide formation (salicide) is presented in Section 3.5.2.

Mann and Clevenger (1994) studied the phase transformation from the orthorhombic base-centered C49 phase with 12 atoms per unit cell to the orthorhombic face-centered C54 phase with 24 atoms per unit cell. The lower surface energy C49 phase is transformed to the C54 phase due to the lower bulk free energy. Mann and Clevenger found that on a Si substrate the activation energy to transform from C49 to C54 phases was 5.6 to 5.7 eV and was influenced by factors such as surface energy of the starting material (i.e., dopants in the Si) and thickness of the C49 phase.

Rather than a two-step annealing process to form C54 $TiSi_2$ (Figure 3.22), Kal and Ryssel (1999) proposed a direct step annealing process aimed at alleviating the agglomeration of $TiSi_2$, which occurs in devices with subquarter-micrometer ground rules, i.e., those using shallow junctions

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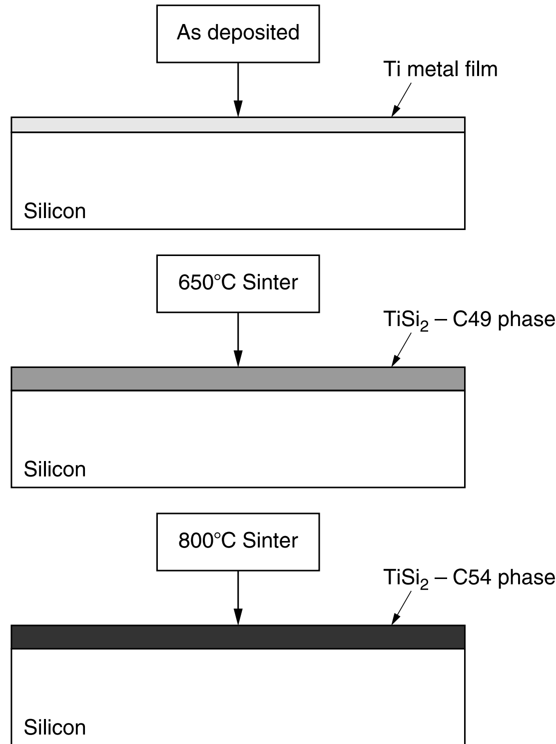

Figure 3.22 Schematic indicating annealing sequence needed to form C49 and C54 phases of $TiSi_2$.

and hence thinner silicides. The direct step technique entails a preamorphization of the Si surface, a thin (<30 nm) deposition of Ti, a high-temperature (850°C) anneal in a nitrogen ambient to form TiN, and selective etch. The premise of the direct step method is that by restricting the volume of Si which can react with Ti (i.e., by controlling the degree of preamorphization), the TiN formation reaction during the anneal will be favored over the $TiSi_2$ formation reaction, thereby limiting and controlling the overgrowth of $TiSi_2$. In the study comparing conventional two-step preparation and the direct step preparation of $TiSi_2$ films, Kal and Ryssel found comparable, if not better, results with the direct step method in terms of sheet resistivity, film thickness uniformity, and surface microroughness.

Yu and Drobny (1989) reported methods of optimizing the formation of TiS_2/poly-Si structures to improve the contact resistance; these included annealing at 800°C to form the low-resistivity C54 phase and ion implantation of As ions to mix the silicide/poly-Si interface before a second anneal. Arsenic implantation doses of $<10^{16}/cm^2$ into the poly-Si did not inhibit formation of the $TiSi_2$ layer. Perera and Krusius (1990) have characterized $TiSi_2$ contacts to n^+ and p^+ Si for contact sizes of 0.3 $\mu m \times 0.2$ μm and found well-behaved electrical and structural characteristics.

However, problems did arise because of the interaction of $TiSi_2$ with ion-implanted dopants. Georgiou et al. (1994) studied the effects of different dopants on $TiSi_2$ properties. Of the three implanted species (As, P, and BF_2), the As samples had the highest sheet resistances (Rs) and the roughest, thinnest films. In all cases of the dopants, an increase in Rs was seen with decreasing linewidth and silicide thickness. Georgiou et al. (1994) also found that the thermal stability of the silicide relied upon the thickness of the silicide, and therefore recommended using P and B or BF_2 to dope the n- and p-gates for 500A silicides on structures <0.4 μm.

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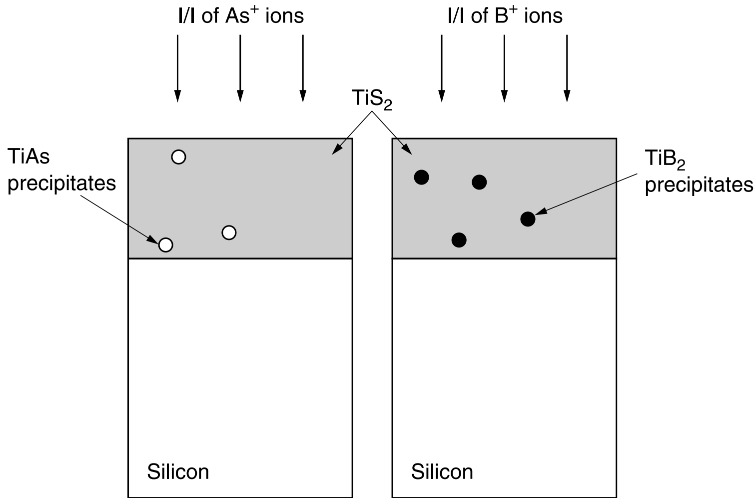

Figure 3.23 Schematic of the formation of intermetallic precipitates in ion-implanted $TiSi_2$. After implantation of dopant ions, a sintering step produces the intermetallic precipitates of TiAs and TiB_2, for As^+ and B^+ implants, respectively.

Mitwalsky et al. (1990) found that unacceptably high contact resistances occurred if B and As dopants were implanted into Si before $TiSi_2$ formation took place. They also implanted dopants into $TiSi_2$, annealed the film, and measured both the sizes of particles and depth distributions of precipitates of metal-dopant compounds of TiAs and TiB_2, as shown in Figure 3.23.

Mitwalsky et al. concluded that $TiSi_2$ is neither a good candidate to be in contact with implanted silicon that undergoes a high-temperature heat treatment to form $TiSi_2$, nor as a preformed silicide layer that receives ion-implanted dopants for subsequent out diffusion into Si. The reasons for this conclusion can be seen in Figure 3.24.

The out-diffusion of As and B ions from the implanted silicide sources are clearly suppressed with respect to the concentrations and diffusion depths achievable with poly-Si as a source; the resulting concentrations of dopants in Si are orders of magnitude less. This implies that the formation of intermetallics within the silicide layer is thermodynamically favored over dissolution of dopants into single-crystal Si.

Concerns for the potential problems created by intermetallic compounds have stimulated several recent investigations. Probst et al. (1991) investigated compound formation including TiAs, TiB_2, TaAs, and TaB_2 for both $TiSi_2$ and $TaSi_2$ films and assessed its impact on dopant diffusion and contact resistance. They noted several detrimental consequences which were: (1) reduction in the solubility of As and B; (2) retardation of the out-diffusion of dopant into Si or poly-Si; and (3) higher contact resistances since precipitation reduces the carrier concentration from the usual $10^{20}/cm^3$ range to only the 10^{18} to $10^{17}/cm^3$ range. Despite limitations of using $TiSi_2$ films in post-silicide ion-implant applications, this contacting material has been extensively investigated from both structural and electrical perspectives. Saito et al. (1993) used selective $TiSi_2$ to form ohmic contacts to very shallow junctions. Using XPS analysis, Lee et al. (1993) investigated these structures as potential ohmic contacts and barriers for submicrometer devices. *In situ* annealing in an atmosphere of NH_3 formed the TiN/$TiSi_2$ bilayer. Both TiN and $TiSi_2$ layers had stable, crystallographic structures when annealed at 800°C. Boron atoms redistributed within the TiN layer and at the silicide/Si interface. Liuah et al. (1993) investigated various physical and electrical characteristics of $TiSi_2$/(100)Si including microstructures, sheet resistance, Schottky barrier height, contact resistance, and junction current leakage. By focusing their investigation mainly on temperatures at

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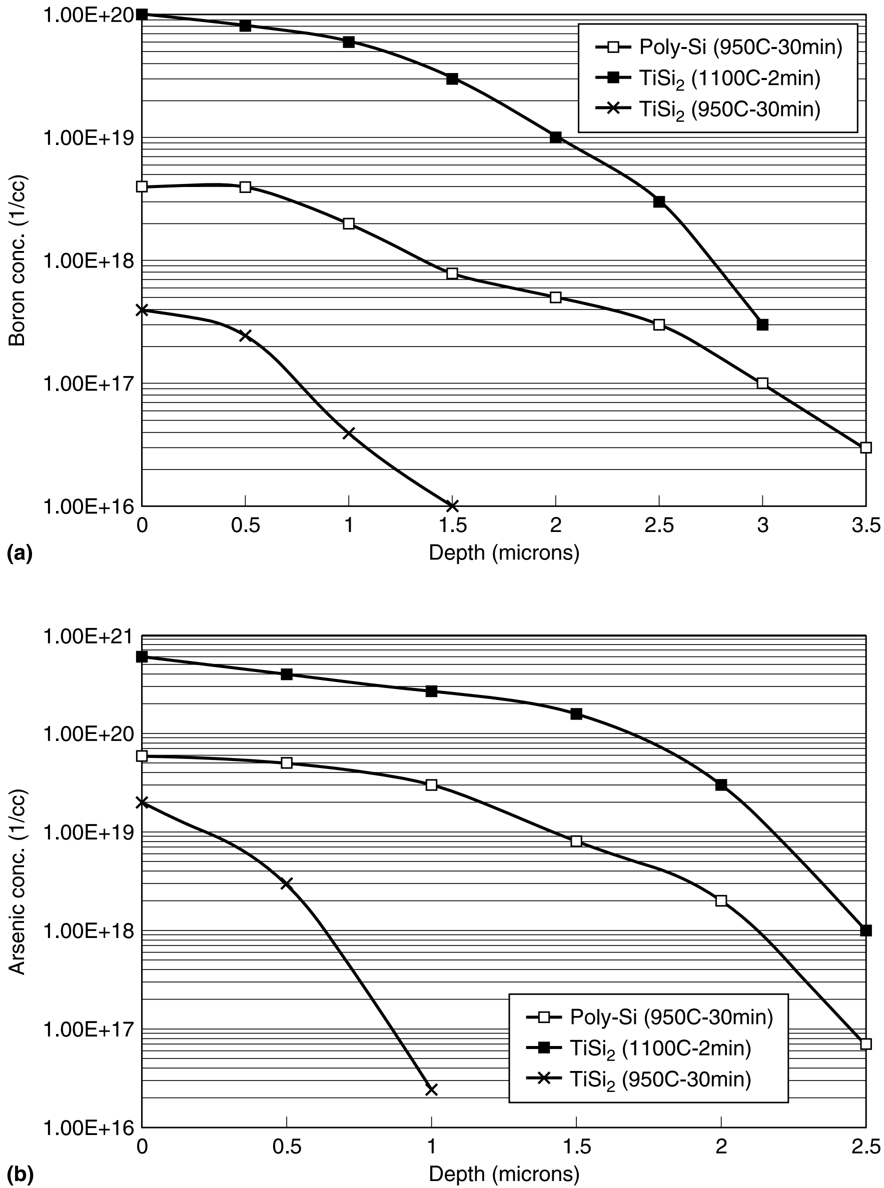

Figure 3.24 Out-diffusion profiles of dopants from poly-Si and $TiSi_2$: (a) boron profiles; (b) arsenic profiles. The anneals of poly-Si take place at 950°C for 30 min, and for $TiSi_2$ at either 950°C for 30 min or 1100°C for 2 min.

or below 450°C, they were able to measure SBD characteristics on silicide interfaces with a thin, amorphous interlayer of Si that was either As or B doped. The amorphous interlayer (α-Si) is formed by low-temperature diffusion between the silicide and monocrystalline Si (c-Si); it affects ρ_c measurably. Barrier heights were 0.52 to 0.54 eV for amorphous n-Si and 0.59 to 0.57 eV for amorphous p-Si. Values of ρ_c were lowest when an a-Si layer was present, and values were reported of $1.4 \times 10^{-7}\ \Omega\ cm^2$ for n-type a-Si and $3 \times 10^{-7}\ \Omega\ cm^2$ for p-type a-Si. The lowering of ρ_c from c-Si values might be caused by redistribution of atomic dopants from the thin a-Si layer to the c-Si interface as the a-Si layer formed. Chou and Chao (1993) also investigated the influence of

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B dopant on $TiSi_2$. They found that the C49 phase formed at 700°C and that almost all the film was transformed into the C54 phase at 800°C. As the concentration of impurities increased, the resistance of the silicides increased and the thickness decreased. Revva et al. (1994) deposited alternating layers of Ti and Si by electron beam evaporation and used them to form $TiSi_2$/Si contacts. They measured the barrier heights for these multilayered structures at progressively increasing sintering temperatures and compared them to conventional, single-layer structures. Although at low sintering temperatures the multilayered film structure had higher barrier heights, at higher temperatures, the ϕ_B values for single and multilayered structures are nearly identical.

3.4.2.3.1 RTA of Titanium Silicides

Mallardeau et al. (1989) used RTA to form the silicide in $TiSi_2$/Si structures, with n- and p-type Si forming both Schottky diode and ohmic contact structures. The values for Ω_s for TiS_2/n^+-Si and, for comparison, PtSi/n^+-Si were 9×10^{-8} and 8×10^{-8} Ω cm^2, respectively. Since the value of ϕ_B for $TiSi_2$ is much lower than for PtSi, the nearly identical ρ_c values suggest that the dopant, As in this case, is more effectively snow-plowed by PtSi than $TaSi_2$. For p_+-Si, ρ_c values for PtSi (2×10^{-7} Ω cm^2) are considerably lower than for $TiSi_2$ (10×10^{-7} Ω cm^2), which corresponds to the lower value of ϕ_B for PtSi. Finally, ϕ_B for $TiSi_2$/n-Si was 0.52 eV and n was 1.08.

RTA was used by Chung and Yao (1990) to evaluate TiW/Ti contact metallizations. They found that RTA had little effect on ρ_c but could convert the Ti in contact with the Si into silicide and, at the same time, formed a thin layer of TiN on the top of the TiW surface. By controlling RTA temperature and time, the interaction of TiW with Si was minimized.

Kubota et al. (1993, 1994) described a contact-formation process involving sputtering a $Ti_{>1}N_{<1}$ film onto a Si contact and by subsequent annealing simultaneously (1) to form Ti silicide by converting the portion of the film in contact with Si and (2) to convert the top portion into a stoichiometric TiN layer.

RTA was used by Uppili et al. (1994) to anneal $TiSi_2$ films used as contacts to emitter poly-Si structures in a double poly-Si bipolar process. They found that the shorter RTA cycle resulted in superior silicide morphology and low ρ_c between $TiSi_2$ and n^+ poly-Si layers. Implanted As increased the poly-Si conductivity upon RTA (Kalnitsky et al., 1994) which was attributed to a reaction between inactive As and lattice vacancies.

Collimated sputtering, which increases coverage of the bottoms of deep submicrometer contacts, was used by Sekine et al. (1995) to deposit Ti. Details about this relatively directional sputtering process can be found in Chapter 1 and Chapter 6; likewise, the concept is illustrated in Figure 1.23.

Collimated Ti, when used in combination with downstream etching using CF_4/O_2 to remove damaged Si layers, generally gave lower values for ρ_c for 0.4 μm contacts having an AR = 4. The magnitude of the improvement was as much as a factor of 2 for RTP temperatures of 600°C and thin Ti bottom layers ~100 Å thick. For thicker Ti layers of 600 Å and RTP temperatures of 700°C, the improvement was only 5 to 10%.

3.4.2.4 Cobalt Silicide

As mentioned previously, $CoSi_2$ is replacing $TiSi_2$ in subquarter-micrometer applications. This change stems from the lesser sensitivity of $CoSi_2$ to processing conditions below 900°C, greater thermodynamic stability relative to $TiSi_2$, comparably low resistivity (14 to 18 μΩ cm), its suitability for forming self-aligned silicides (salicides) (Murarka, 1986, 1993b; Murarka et al., 1987), and scaling factors which are elaborated upon below.

In subquarter-micrometer designs, the reduced lateral dimensions makes it difficult to form the low-resistance phase of $TiSi_2$ (C54) without increasing the anneal temperature. An additional requirement of shallow junctions requires thinner $TiSi_2$ which, unfortunately, is more susceptible to

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agglomeration. Fortunately, however, both Co and Ni silicides can form their respective low-resistive phases without regard to contact dimension (Tas et al., 2003). The remainder of this Section discusses the evolution of the Co silicide process integration. The next Section discusses Ni silicide.

A sputter deposited thin film of Co reacts readily with Si or poly-Si but negligibly with SiO_2; hence oxide or nitride can be used as a masking layer for Co salicides. Based in part on this property, Murarka et al. (1987) developed a two-step annealing process which is the basis of our discussion of all further process integration refinements of $CoSi_2$. The process involved (1) lithographically defining the area, (2) deposition of Co, (3) heating to form a metal-rich silicide at a temperature below 450°C, (4) removal of the unreacted metal in a wet etchant (H_2SO_4, HNO_3, or HCl), and (5) subsequently heating the silicide to over 600°C to form the low-resistance disilicide ($CoSi_2$) layer.

Though the two-step anneal process is widely used, other ways to form $CoSi_2$ layers have been investigated and are included here for completeness. Broadbent et al. (1989) used RTA to form $CoSi_2$. Werner and Güttler (1993) investigated the interface structure and the Schottky barrier heights of buried $CoSi_2$/Si(001) produced by high-dose ion implantation of Co^+ ions followed by RTA. The layers so formed showed excellent epitaxy and smooth {001} interfaces. Both sixfold- and eightfold-coordinated Co atoms existed at the interfaces. Barrier height measurements indicated higher values for the lower or more deeply implanted layers of $CoSi_2$/n-Si(001) than for the shallower layers. Stress induced the precipitation of dopants diffused into Si from both $CoSi_2$ and $TiSi_2$ layers according to La Via et al. (1993). Both RTA and conventional annealing of As, P, and B ions, implanted through the silicide layer, resulted in precipitation of the dopants at the silicide/Si interface. The authors speculated that the high tensile stress, induced by the silicide layer on the surface Si region, and its subsequent influence on the solid solubility of the dopant, caused the precipitation. Alternatively, though not practical for volume production, advanced molecular beam epitaxial film growth techniques for Co silicides were utilized by Fathauer et al. (1988) to produce $CoSi_2$ layers on p^+-doped Si (111). Prior to growing the $CoSi_2$ layer, a fresh Si surface was created by *in situ* epitaxial growth of p^+ Si on to the Si(111) wafer surface. Measured values of ϕ_B ranged from 0.61 to 0.89 eV, depending on the thicknesses of the epitaxially grown p^+ layer.

As stated earlier, a thin film of Co reacts readily with Si or poly-Si but negligibly with SiO_2. That fact has two impacts on $CoSi_2$ integration. First, the lack of Co reaction with oxides or nitrides means those materials can be used as a masking layer for Co salicides. However, in order to reduce damage to the substrate, which can be caused by overetching when creating the contact openings through the oxide or nitride, the etchant and reactive ion etching (RIE) process conditions must be highly selective to the substrate. To achieve adequate etch control, an etch-stop layer can be used and/or the etch process can be controlled by an endpoint detection system. The second integration implication of Co not reacting with oxides or nitrides is the need for good oxide and/or oxygen control both prior to and during silicide formation. Prior to Co deposition, the etched Si surface must be thoroughly cleaned. HF is commonly used. A low-energy Ar^+ sputter etch prior to cobalt deposition is sometimes used as well, but it can lead to damage, resulting in a rough interface. A rough interface, whether the result of a damaged surface or insufficient cleaning of thin oxide layers, can lead to junction leakage. Junction leakage can also be altered by choice of dopant. By changing the n^+ dopant from As to P, Agnello (1999) observed an improvement in the leakage tail of smooth $CoSi_2$ films.

Another place to address thin oxide layers is during the silicide formation. To address oxide at the surface of the Si, Ku et al. (1999) studied the effect of Ti or TiN capping layers deposited directly after Co deposition onto an uncleaned Si surface. By SIMS measurements, Ku et al. determined that during a first anneal Ti migrated to the Co/Si interface and dissociated oxygen residing at the interface whereas TiN showed no change at the Co/Si interface. After a second anneal Rs measurements indicated the Ti-capped sample had converted to $CoSi_2$, whereas the TiN did not. Ku et al. view Ti capping of Co films as a way to reduce the sensitivity of the Co salicide process to surface conditions.

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Giving a clean Si surface, oxygen can also have an impact on $CoSi_2$ formation by ambient oxygen reacting with deposited Co. Again, a capping layer (TiN) has been studied to shield the Co during a first anneal (Goto et al., 1994). After the first anneal, the capping layer and unreacted Co is removed. Then a second anneal is performed to form the disilicide. In addition, Chiou and Chieh (1994) studied the thermal stability of Cu–$CoSi_2$ contacts to p+n shallow junctions and concluded that the structure had poor thermal stability and a TiW diffusion barrier was highly desirable.

The incorporation of a Ti capping layer, however, brings on other issues. First, the Ti gettering of oxygen forms an upper layer of Ti_xO_y which is not etched by the standard H_2SO_4 etch. Therefore, the Ti is deposited in a nitrogen ambient which results in the upper layer of TiN that can be etched with $NH_4OH/H_2O_2/H_2O$. Any remaining unreacted metal is then etched with H_2SO_4. The second implication of a Ti capping layer is that the temperature required to form the silicide increases, and increases with the thickness of the capping layer (Detavernier et al., 2001). Additionally, the Ti layer can be deposited prior to Co deposition (Ho et al., 2002). The Ho patent proposes a multilayer deposition of Ti, Co, and Ti and a two-step anneal to form a Co salicide layer. Byun et al. (1997) tried to avoid capping layers by sputtering the Co film in 1 to 10% by volume nitrogen ambient at high temperatures (500°C). Byun et al. observed a polymorphic change in the as-deposited Co from the hcp (110) orientation, large-grained (300 nm) α-phase at 0% nitrogen to the fcc (111) orientation, small-grained (30 nm) β-phase Co at greater (5 to 10% by volume) amounts of nitrogen. With increasing nitrogen content, it was observed that nitrogen accumulated at the CoSi/Si interface resulting in thinner CoSi films and a more uniform CoSi/Si interface. The sheet resistance from such a structure, while satisfactory, was not as low as that of a TiN-capped control structure. Finally, a novel method of combining both $CoSi_2$ Schottky barriers and TiN diffusion barriers was investigate by Gromov et al. (1995), who utilized a TiCo alloy which was sintered in contact with Si at temperatures of 800 to 850°C to form $CoSi_2$/Si contacts (Schottky and ohmic) together with a TiN barrier layer. On n-type Si, the value of ϕ_B and the ideality (n) for an annealed $Ti_{73}Co_{27}$/n-Si contact were 0.64 eV and 1.06, respectively. Ohmic contacts to n-type Si had a value of ρ_c of 5×10^{-7} Ω cm^2 and to p-type Si, 1×10^{-6} Ω cm^2.

The capping layers, cleaning schemes, and two-step anneals made Co silicides successful contacts for 180, 130, and 90 nm products. However, for 65 nm designs and below, Co silicide encounters some problems. The first problem is gate length extendability. Scaling requires both reduced junction depth and a reduced area for forming the silicide. At sub-40 nm gates, it is difficult to form $CoSi_2$, which results in voids and high resistance. It has been found that a lower temperature and a shorter time for annealing reduces the resistance (Besser et al., 2003). However, the junction leakage increases with decreasing temperature of the formation anneal. Therefore, the Co silicide process window shrinks, unacceptably, with 65 nm designs. One proposed solution is to alloy the Co with Ni which reduces the formation temperature of the $CoSi_2$ (Kittl et al., 2003).

A second potential problem is the proposed use of strained Si films in some applications at 65 nm and below. A strained Si film increases the speed of the transistor with increased electron mobility. The strain is created by the addition of germanium (Ge) to the Si. However, Ge is not soluble in $CoSi_2$. In addition, Ge increases the formation temperature of $CoSi_2$ (Kittl et al., 2003).

A third problem with $CoSi_2$ at 65 nm is Si consumption. Cobalt silicide formation, like Ti silicide formation is due to Si diffusion rather than metal diffusion. Silicon can be consumed/migrate both horizontally and vertically. As Si migrates horizontally, the metal is left behind which can lead to bridging of silicide between that source or drain and gate (Berti and Baranowski, 1998).

At advanced ground rules, the junctions become very shallow and the vertical consumption of Si by the silicide consumes an increasing percentage of the junction silicon which thereby increases the leakage. Therefore, for advanced ground rules, Co will likely be replaced by Ni. The main attractions of Ni over Co is that NiSi consumes 35% less Si than Co for a given sheet resistance (Lauwers et al., 2001). The Ni consumption of Si and can be expressed as: 1A Ni + 1.84A Si $\rightarrow$ 2.2A NiSi (Fromet et al., 2003).

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3.4.2.5 Nickel Silicides

One of the earlier studies of nickel silicide was by Hoekelek and Robinson (1978), in which an Al/NiSi/Si structure on n-type (111)Si was studied. The diodes consisted mainly of the NiSi phase that formed a Schottky diode with a barrier height of 0.62 eV. Upon heating in contact with a thin Al overlayer, the NiSi layer was transformed into $NiAl_3$, with a consequent increase in the barrier height to 0.76 eV. They observed stable electrical characteristics and an absence of penetration for this layer up to 500°C.

Interfaces between single-crystal $NiSi_2$ and Si, of both (100) and (111) orientations, produced by codeposition of Ni and Si on the appropriately oriented Si substrate were analyzed by Kikuchi et al. (1988). For $NiSi_2$/Si(100), ϕ_B was 0.65 eV, independent of the silicide thickness. For type-B $NiSi_2$/Si(111), where the term "type-B" refers to a twinned structure, resulting from a 180° rotation about the surface normal to the orientation of the Si(111) substrate, ϕ_B was found to be dependent on $NiSi_2$ thickness, becoming constant at 0.65 eV for silicide thicknesses at or exceeding 50 nm. A value for ϕ_B of 0.78 to 0.79 eV was estimated by extrapolation to a thickness of $NiSi_2$ of 1 to 2 atomic layers.

The temperature and pressure dependencies of Schottky barrier heights on Si for a variety of contacts (Ti, W/Ti, PtSi, Pd_2Si, IrSi, $CoSi_2$, $TiSi_2$, Sm, and $NiSi_2$), some of which were epitaxial ($NiSi_2$/Si(111), types A and B) or faceted ($NiSi_2$/Si(100)), were investigated by Werner et al. (1993). In contrast to the type-B twinned epitaxial relationship between $NiSi_2$ and Si(111) described above, type-A refers to a $NiSi_2$ that is identical in orientation to the underlying Si(111). From the analysis of epitaxial $NiSi_2$/Si diodes, the authors concluded that there is a direct correlation between interface crystallinity and both the value of ϕ_B and its temperature dependence. Additionally, both pressure and temperature coefficients of the polycrystalline Schottky contacts correlated with the same coefficients for the band gap, indicating that the thermal emission model fully accounted for the observations of ϕ_B.

Due to the enumerated problems of $CoSi_2$ at the 65 nm node, more recent studies of Ni silicide formation address it as a replacement for $CoSi_2$. Nickel silicide has a lower temperature of formation, lower sheet resistance, reduced silicon consumption, and integrates well with Ge. This Section discusses NiSi formation and integration.

Nickel silicide is formed by migration of Ni into the Si, rather than Si into the metal which is the case for Ti and for Co. The first phase formed during the silicide process is Ni_2Si, followed by NiSi (400 to 600 C) and $NiSi_2$ (700°C) (Lauwers et al., 2001). NiSi is the desired low-resistivity phase. Nickel-rich phases have a narrow range at which they exist and easily transform to other phases. Which phase(s) exist(s) depends upon the temperature and the ramping rate (Besser et al., 2003). However, if the Si surface has a thin oxide layer, then $NiSi_2$ can form directly on the substrate. Hence, surface preparation is key, as it is for all silicide processes (Kittl et al., 2003).

There is a distinct advantage in the fact that nickel is the dominant diffusing species rather than Si. First, there is little likelihood of the bridging of the silicide from source/drain over the spacer dielectric to the gate. Second, diffusion of Ni leads to smoother interfaces resulting in better electrical properties (Zhang and Ostling, 2003).

Both two- and single-step anneals for the formation of NiSi are being investigated. The annealing step must achieve two things. First, it must convert the Ni and Si layers to NiSi without onset of the higher resistance disilicide phase. Second, the anneal must not induce lateral Ni silicide growth in confined areas. Single-step anneals are adequate for forming the NiSi phase. However, Lauwers et al. report lateral growth of NiSi on As- and B-doped Si for a single-step anneal. It was reported that the higher the temperature, the longer the anneal, or the thicker the Ni film, the more likely lateral growth. Therefore, a two-step anneal was proposed with a first anneal at 350°C or lower to limit lateral growth, and a second anneal completing the transformation to NiSi at 450°C (Lauwers et al., 2001; Fromet et al., 2003).

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With respect to doping, the NiSi film formation temperature only increases slightly, 40°C for As- and 20°C for B-doped substrates, compared to undoped Si (Lauwers et al., 2001).

It was found that heating (550 to 900°C) a NiSi film increased its sheet resistance. The sheet resistance increase, for thin films and lower temperatures, was due to agglomeration of the NiSi films. The driving force for the agglomeration is reduction of the NiSi grain boundary energy. For high-temperature heat treatment and thicker films the sheet resistance also increased; however, it was found that the increase was due to $NiSi_2$ formation rather than agglomeration. It was also reported that NiS_2 transformation occurred more readily (i.e., at lower temperatures) on poly-Si surfaces than on (100)Si (Kittl et al., 2003).

However, Ni is not without its problems, too. One problem is that NiSi films can grow thicker on smaller features (opposite problem of Co) which can result in junction leakage at small active area contacts and gate poly consumption (Kittl et al., 2003). Nickel silicides also form the higher resistivity $NiSi_2$ phase at relatively low temperature, and therefore all processing steps after and including silicidation must be at low enough temperature to avoid the high-resistivity phase. The addition of Pt can help alleviate this problem by increasing the temperature at which a high-resistive film forms to something above 850°C. However, the resistivity of NiPtSi films annealed at temperatures of 900°C increase due to agglomeration of NiSi, rather than formation of $NiSi_2$ (Chi et al., 2001).

Although Ge is soluble in NiSi, it lowers the formation temperature of the higher resistance $NiSi_2$ film and agglomeration onset temperature. The temperature of agglomeration set decreases with increasing Ge content (Besser et al., 2003). Even with the lowering of agglomeration onset temperature, the process window of NiSi films on $Si_{0.8}Ge_{0.2}$/Si(100) is wide enough to be of practical use (Isheden et al., 2003).

For the near future, an alternative to the traditional, planar salicide process is being proposed; it uses a selective epitaxial Si layer which reacts with a subsequently deposited metal to form the silicide. The advantage to this raised source/drain technique is that it provides extra Si which can be consumed, an important consideration in abrupt ultrashallow junction devices, since the silicide must be half the depth of the junction in order to avoid contact leakage. The disadvantage to a raised source/drain system is the increased likelihood of bridging between the source/drain and gate due to the selective nature of the epi-Si and the combination of decreased feature sizes (International Technology Roadmap for Semiconductors, 2003).

Beyond raised source/drain NiSi, the future of contact material systems is not clear. What is clear is that the future material system must be compatible with metal gates (two metals, one for P and one for N to achieve acceptable threshold voltages for the near valence band Fermi level of the P transistor and near conduction band Fermi level of the N), with low-temperature requirements of high-ε gate dielectrics, and perhaps with carbon-doped SiGe channels.

3.4.2.6 Snow Plow Effect

Specific contact resistance values for various silicides do not correlate well with Equation 3.7, because of low-temperature diffusion of dopants during silicide formation. Witmer et al. (1983) electrically analyzed the profile of implanted As and then the redistribution of As which was caused by the formation of Pd_2Si. Witmer and co-workers correlated these measurements with previous ion channeling observations made by Witmer et al. (1982) of this same effect. "Snow plow effect" is the name typically applied to this phenomenon. The increase in As concentration beneath the silicide/Si interface that is shown schematically in Figure 3.25 reduced the contact resistance, and was suggested as a way to adjust barrier heights. One obvious benefit this has is compensation for the anticipated increase in ρ_c if a contacting silicide or metal layer with a high ϕ_B needs to be used, because of a reduction in the ratio $(\Phi_B/\sqrt{N_D})$, as predicted by Equation 3.7. Rejection of dopants, in this case As, from the region transformed to silicide will increase N_D from initial implanted levels thereby lowering this ratio and ρ_c values.

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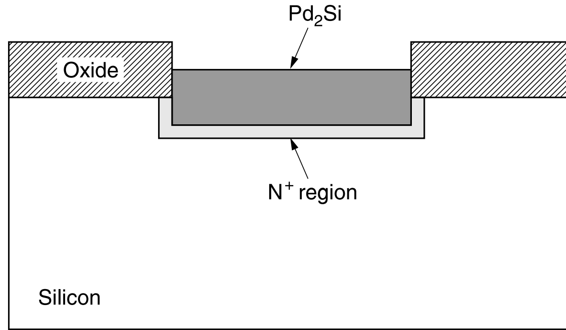

Figure 3.25 Snow plow effect indicating accumulation of N^+ dopant occurring during formation of Pd_2Si phase.

3.4.3 Diffusion Barriers

3.4.3.1 TiW Films

Diffusion barriers are an indispensable part of a reliable contact structure; they prevent junction penetration by Al or poisoning by Cu. Fortunately, effective barriers were found nearly in concert with the recognized needs, and several of these barrier concepts and related material properties are described in this section.

Ghate et al. (1978) reported the earliest study pointing out the merits of TiW as a diffusion barrier for Al metallization. They used a pseudo-alloy of TiW (10:90 wt%) in structures of Al/TiW/Si and looked for sheet resistance changes upon annealing as evidence for metallurgical reactions. After annealing, the resistivity of the Al layer had increased less than 10%. This relatively small change is most likely due to limited diffusion of Ti and/or W into the Al. Auger profiling of Si/TiW/Al structures indicated that the barrier remained intact, i.e., there was no penetration of Al to the TiW/Si interface after annealing at temperatures of 450, 500, and 550°C, which suggested application to Al/TiW/PtSi contact structures in integrated circuits.

The reaction kinetics of Al/$Ti_{22}W_{78}$ and Al–2% Cu/$Ti_{22}W_{78}$ thin-film couples were measured by Olowolafe et al. (1985) using Rutherford backscattering. The TiW samples were sputter deposited and the Al and Al–2% Cu layers were evaporated in a separate system. The surface of the $Ti_{22}W_{78}$ was either sputter cleaned or intentionally contaminated with air to produce an interfacial oxide. The accumulation of Ti on the surface of the overlying Al or Al–2% Cu film provided a measure of the extent of the reaction with the sputter-cleaned $Ti_{22}W_{78}$ barriers. The quantity of accumulated Ti had a linear dependence on the square root of the reaction time for the four temperatures investigated (530, 500, 475, and 450°C), indicating a diffusion-controlled process. The barriers that were exposed to air prior to deposition of Al or Al–2% Cu resisted any reaction when heated at 500 or 550°C for 10 hours but did eventually react at 600°C. The activation energy derived from these data was 2.4 eV and was the same for both Al and Al–2% Cu. Although it is not possible to determine the rate-limiting mechanism definitively, one can argue that this energy is much too high to be the diffusion of Ti through Al (or Al–2% Cu) which should be in the range 1.0 to 1.5 eV. The relatively high energy observed suggests grain boundary diffusion within the refractory barrier. As it turns out, this is more than an idle speculation because, in a companion study, Palmstrom et al. (1985) used TEM to show that the $Ti_{22}W_{78}$ film was penetrated by Al at grain boundaries. Therefore the activation energy observed by Olowolafe et al. (1985) is very likely the diffusion energy for Al along grain boundaries in the $Ti_{22}W_{78}$ film. Once Al penetrates the barrier film, Ti can easily migrate to the surface with its much lower energy. This lower energy should not be rate limiting and therefore

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not detectable by the measurements used. Palmstrom et al. (1985) also detected the intermetallics $TiAl_3$ and WAl_{12} in the reacted films.

Babcock and Tu (1986) investigated Al penetration into TiW contacts on Si. They determined a barrier height of 0.51 eV to n-Si and showed that structures with 20 at% Ti were stable up to 500°C and 30 min. Increasing the Ti content to 30 at% made them stable up to 600°C. The barrier properties of TiW were improved by sputtering it in an Ar–N_2 atmosphere; a reduced reaction of W with overlying Al layers was also noted. The investigation by Wolters and Nellissen (1986) covered both Al/TiW:N/Si contact structures and Si/Al–Si/TiW:N/Al multilevel structures. Although the incorporation of N in TiW increased the resistivity of this barrier film, the diffusion barrier properties were improved and the resulting structures still had acceptable dry etching and contact resistance characteristics.

Grove et al. (1989) annealed a W/Ti bilayer in a N_2 atmosphere to create structures such as Al/W/TiN_y/$TiSi_z$ on both n^+ Si and p^+ Si, thus forming a reliable contact diffusion barrier that was characterized by several profiling techniques. Auger profiles showed the stability of these structures after they were annealed at 650°C for 20 min. Thalapaneni (1993) patented the combination of Ti and TiW films for use as an improved barrier and electrical contact to Si. The Ti layer reduced the contact resistance and helped to block the diffusion of Al along TiW grain boundaries. Additionally, a plasma etch removed about 250 Å of Si from the contact surface and removed the damage created by the more energetic anisotropic etch as well The anisotropic etch was used initially to open the contacts and to access higher dopant concentration that occurs a few hundred angstroms beneath the Si surface. The barrier properties of TiW, applied to both Al- and Au-based conductors, have been generally reported to be satisfactory. A recent study by Evans and Leet (1994) has uncovered a potential problem for Au metallizations. Barrier properties of 3%Ti–W films sputtered in N_2 exhibited a catastrophic failure mode that correlates with the occurrence of an A15 structure or β structure in the TiW film. These structures are known to occur in thin films of several refractory b.c.c. metals (W, Ta) and are undesirable because of their metastability and high resistivity relative to the b.c.c. phases. They transform to the b.c.c. phase upon annealing creating high stress and loss of adhesion. However, addition of N to the TiW film to form TiW:N layers appeared to reduce the problem to negligible proportions.

3.4.3.2 TiN and TiN_xO_y Films

Kohlhase and Higelin (1987) investigated the electrical and barrier stability properties of Al–Si/TiN/Ti structures and reported promising attributes for application to 4 Meg DRAM memory circuits. Kumar et al. (1987) reported an extensive study of the barrier properties of TiN, in which a Ti target was sputtered in Ar–N_2, varying the applied bias during deposition. Without applied bias, films appeared dark brown; with bias they were gold. Using structures such as Al/TiN/$TiSi_2$, they found that the gold-colored films were superior as both diffusion barriers and had lower Rc values as compared to the brown films. Films were also sputtered in Ar–N_2–O_2 without bias; addition of O_2 to the gold-colored films increased Rc but decreased the failure rate due to penetration during sintering. The phenomena of the *in situ* growth of an Al_xO_y layer by reaction of Al with oxides present in the TiN:O film is likely responsible for the augmentation of the barrier properties by incorporation of oxygen into the TiN film. For this reason, barriers for Al particularly benefit from incorporation of oxygen or intentional contamination of the barrier surface by air exposure. Figure 3.26 illustrates the contact structure following Al_xO_y formation.

Inoue (1990) patented the use of the augmented barrier properties of TiN:O films to prevent the reaction between Al and Si. The barrier layers were 50 to 200 nm thick, fabricated by sputtering in gas mixtures that contained 1 to 5 vol% O_2, maintaining the Si substrate temperature at 350 to 550°C. The films had a resistivity of 100 $\mu\Omega$ cm, which is too high for wiring applications but quite suitable for barrier applications.

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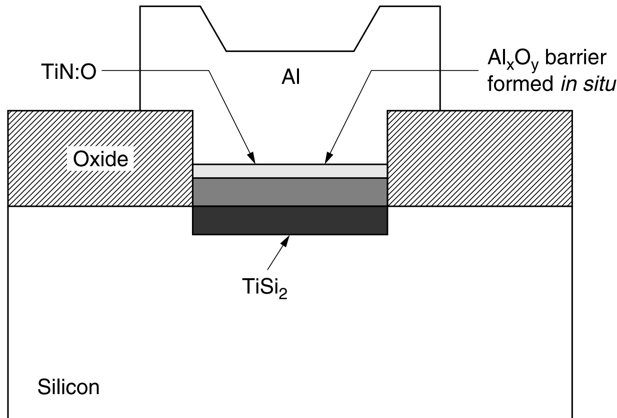

Figure 3.26 Formation of an Al_xO_y layer by reaction of Al with a TiN:O barrier. Barrier enhancement by incorporation of oxygen occurs due to the formation of the Al_xO_y layer upon sintering.

TiN barriers sputtered without collimation do not effectively protect contacts with high aspect ratios (i.e., AR > 1.0), according to Pintchovski and Travis (1992). The authors concluded that CVD TiN processes were necessary to address the higher ARs associated with 0.35 μm technologies. Yokoyama et al. (1991) investigated the barrier layer properties of TiN films formed by LPCVD, using $TiCl_4$ as the precursor, for application to high AR contact holes. These investigators found good step coverage in contact holes with AR = 1.8 and TiN films of nearly stoichiometric proportions. They also found that they could reduce the Cl content of the films from 5.7 at% at 500°C to < 1 at% at 700°C. Annealing in H_2 at 1000°C also reduced the Cl concentration of films deposited at 500°C by a factor of 2. Films formed at 700°C had resistivities of 80 μΩ cm, which is less than that of films formed at lower temperatures, leading to speculation that the resistivity may be sensitive to the Cl content.

Frahani et al. (1989) reported on the rapid thermal processing (RTP) of Ti films in the presence of NH_3 to form TiN barriers. They found that only relatively thin layers of TiN (200 to 240 Å) formed in a single-step nitridization process and that this occurred over the relatively narrow temperature range of 600 to 610°C. Effective diffusion barriers required nitridization and also the presence of $TiSi_2$ under the TiN.

The structural and electrical integrity of stacked electrodes consisting of W/TiN/poly-Si (n^+ and p^+)/SiO_2/Si which have high conductivity and provide dual work function capability, as required for CMOS circuits, was studied by Pan et al. (1989). The TiN films were thought to be effective barriers to diffusion because there was an absence of any silicide formation, even after annealing at 1000°C for 30 min and they detected very little dopant diffusion from the poly-Si into the overlying W film using Auger profiling. Moreover, the electrical properties of the 10 nm SiO_2 film that underlies the W/TiN/poly-Si stack were quite good. Evidence cited for this conclusion was stable flatband voltages, low interface state densities, and tightly distributed breakdown voltages.

3.4.3.3 $TaSi_2$

Neppl and Schwabe (1984) reported on the properties of $TaSi_2$ for Al interconnect metallization. They studied the properties of both cosputtered amorphous and polycrystalline films using Schottky and ohmic contacts. When the silicide films contained an excess of Ta, they served effectively as barriers up to 475°C. Singh et al. (1986) studied the reaction and interdiffusion between Al–Si and Mo films. Thermal annealing of the coupled films resulted in the formation of the $MoAl_{12}$ phase as

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a nonplanar front. The kinetics of the phase formation was diffusion-controlled, as shown by a parabolic time dependence; the activation energy E_a was 5.9 eV. The presence of Si precipitates at the Mo/Al–Si interface explained the high value of E_a and the occurrence of incubation periods before parabolic behavior. Kolawa et al. (1991) investigated the diffusion barrier properties of sputtered Ta-based films. These investigators showed that Ta films were relatively less effective as barriers for Cu since they failed at temperatures of 500°C. In comparison, amorphous binary ($Ta_{74}Si_{26}$) and ternary ($Ta_{36}Si_{14}N_{50}$) films prevented Cu migration up to temperatures of 650 and 900°C, respectively. Reverse diode characteristics were sensitive indicators of barrier effectiveness in this study.

3.4.3.4 Niobium

Farahani et al. (1994) evaluated the utility of Nb as a diffusion barrier to prevent Al–0.5% Cu migration into Si. They concluded that Nb was an effective diffusion barrier and that it also significantly enhanced the electromigration resistance of the conducting metallurgy. Structural analysis showed the presence of the $NbAl_{13}$ phase.

3.4.3.5 Titanium Carbide

Eizenberg et al. (1984) investigated titanium carbide films, with various carbon contents, for their suitability as diffusion barriers between Al and Si; the optimal film had the composition $Ti_{3.1}C$. The film was preannealed at 750°C to form a Ti_xC outer layer, and an inner layer (adjacent to Si) that was a mixture of several phases of titanium silicide (Ti_5Si_3, TiSi, $TiSi_2$). These structures were stable in the presence of Al films for heat treatments at 550°C for 30 min. At temperatures of 600°C, the barriers failed with the formation of Al_4C_3, suggesting that the TiC layer had effectively decomposed.

3.4.3.6 Palladium Tungsten Alloys

Eizenberg et al. (1985) also studied the thermal stability of Al/Pd_xW_{100-x}/Si contact systems using AES, RBS, XRD, and the *I–V* properties of Schottky diodes. They found that W-rich alloys, such as $Pd_{20}W_{80}$, provided contact stability even after annealing at 550°C for 30 min. The Pd from the alloy migrated to the Si surface to form a thin Pd_2Si layer and to the interface with Al to form Al–Pd intermetallic compounds. The authors stated that the advantages of this structure were providing both a diffusion barrier and a shallow silicide contact. Takeyama et al. (1993) cited an even higher thermal stability, up to 600°C, in an investigation of Al/$Al_{12}W$/W_2N/Si structures. Part of the rationale for this structure was the commonality of at least one element across an interface for the two bordering film materials. The intention was to create a lower free energy state and consequently reduce the driving force for metallurgical reactions. Wang et al. (1994) have favored the use of a bilayer structure of $TaSi_xN_y$/$TaSi_x$ in Si contacts. They showed that the upper layer provided an effective diffusion barrier against Al penetration, while the bottom layer provided low sheet resistance R_s and a low ρ_c.

3.5 OHMIC CONTACTS

3.5.1 Metal/Silicon

Ohmic contacts are usually characterized by a value of ρ_c (in, as stated earlier, units of Ω cm^2). Contact resistance, R_c, is expressed in units of Ω, and given, therefore, by the expression

$$R_c = \rho_c / A \tag{3.11}$$

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where A is the area of a contact device port, such as the emitter, base, or collector of a bipolar transistor or perhaps the source or drain of a field effect transistor. For those contacts that carry the highest current in a circuit, designers seek the lowest possible resistance values. Examples are the emitter and collector in a bipolar logic circuit or the source and drain in a CMOS memory chip. It is common practice to implant these resistance-sensitive contacts with a dose that at least equals the solubility limit for the particular dopant in Si. This corresponds to As or P concentrations exceeding about 1×10^{20} to $2 \times 10^{20}/cm^3$, and similarly for p-type Si with B as the dopant. As Table 3.1 indicates, the lowest values of ρ_c attainable are approximately in the range of 1×10^{-7} to 3×10^{-7} Ω cm^2. For a 1 μm^2 contact, the corresponding R_c values are 10 to 30 Ω, and for 0.5 μm^2, the values are 40 to 120 Ω, etc. Due to its much lower current-carrying requirements and the higher resistance of the base structure of the transistor, the base contact can function with a lower doping level and, consequently, higher value of R_c. This circumstance is probably responsible for the general lack of experimentally determined values of ρ_c for these contacts. As shown in Figure 3.27, poly-Si is usually used as a circumferential base contact in bipolar transistors and as part of the defining structure of the emitter contact. Due to grain boundary segregation, B-doped poly-Si can have a carrier concentration of only 1/10 or so of the actual atomic doping level, N_D. This would tend to raise ρ_c, according to the expression $\rho_c \sim \exp(\phi_B / vN_D^*)$, where the asterisk is introduced here to indicate the electrically active dopant concentration. However, assuming ϕ_B to be ~0.2 eV (PtSi), the lower barrier height on the p-poly-Si contact will act to reduce ρ_c.

Section 3.4.1 and Section 3.4.2 discuss several of the silcides that are used to make ohmic contact to bipolar emitters and gate/source/drain contacts of an FET. Some of the commonly occurring contacts in a semiconductor device and frequently used nonsilicide materials are discussed in the following sections.

3.5.1.1 Resistor Contact

One of the early patents dealing with the formation of ohmic contacts (Martin, 1969) described a method for defining and making contact to a diffused resistor without the need for enlarging the resistor contact area beyond the width of the body of the resistor. This method, shown schematically in Figure 3.28 through a sequence of structures, utilizes the fact that the diffused region is wider than the masked opening because of the lateral diffusion of the dopant species.

Thus the enlarged diffusion region provides for metal contact only to the diffused region, in spite of the lateral etching of the field oxide for defining the contact opening, which exposes more of the diffused area. A metal processing patent assigned to RCA Corp. (RCA, 1967) cited the use of plasma etching to clean a Si surface prior to deposition of Al metal by evaporation. Annealing at 550°C formed the contacts to the source and drain regions of CMOS devices.

3.5.1.2 Wiring Level Contacts

Cunningham and Clark (1970a) described the use of Mo/Au/Mo structures to form, simultaneously, ohmic contacts to Si and the first level of interconnection wiring. Additionally, a second level of metal could be formed using the same metallization. Cunningham and Clark (1970b) provided additional refinements to their multilevel metallization scheme in a similar, subsequent patent. Additional details concerning these structures can be found in the original patents.

3.5.1.3 Cermet Barrier Contact

Beaudouin et al. (1971) patented a metallization structure for contacts employing a Cr–SiO_2 cermet as a contacting material to Si and as a diffusion barrier between Si and the Cu/Cr metallization. The

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Table 3.1 Values of Specific Contact Resistance

Specific Contact Resistance (μΩ cm)		Contact Structure			Conditions			Source	
High	Low	Metal	Silicon	Doping	T (°C)	Method	Note	Author	Year
0.12		Al	Si	n-type		e-beam		Chen	1983
0.15		Al	Si	p-type	950	RTA	B–1/1–4 × 10^{-5}	Hara	1983
0.15		Al	Si	p-type		e-beam		Chen	1983
0.70	0.60	Al–2% Cu/$MoSi_2$	Si		500			Yamamoto	1985
0.15		Al/Ti	Si					Ting	1982
0.6	0.2	CVD $TiSi_2$	Si					Saito	1993
0.10		Mo/Ti	Si	n-type				Kim	1985
0.19		Mo/Ti	Si	p-type				Kim	1985
0.84		PtSi	Si	n-type		furance		Huang	1988
0.075		PtSi	Si	n-type	1050	RTA		Huang	1988
0.08		PtSi	Si	n-type				Mallardeau	1989
0.2		PtSi	Si	p-type				Mallardeau	1989
0.19	0.15	Pd_2Si	Si	n-type				Singh	1986
0.31	0.28	Pd_2Si	Si	p-type				Singh	1986
2.0	0.8	Sel CVD W	Si	n-type				Mariya	1983
0.15		Si/Al/Ti	Si					Ting	1982
0.5	1.0	$Ti_{73}Co_{27}$	Si	n-type				Gromov	1995
0.14		$TiSi_2$	a-Si	n-type	450			Luiah	1993
0.30		$TiSi_2$	a-Si	p-type	450			Luiah	1993
0.09		$TiSi_2$	Si	n-type				Mallardeau	1989
1.0		$TiSi_2$	Si	p-type				Mallardeau	1989
24.0		W/Ti	Si	p-type		furance		Chen	1981
3.6		W/Ti	Si	p-type		laser	$p = 10^{19}$ cm^{-3}	Chen	1981

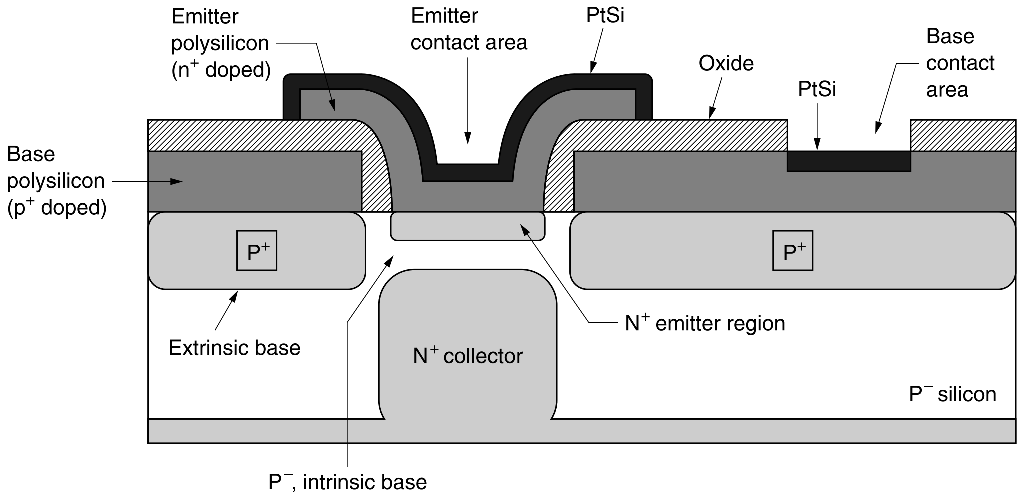

Figure 3.27 Cross-section of bipolar structure including poly-Si base, poly-Si emitter, and PtSi contacts.

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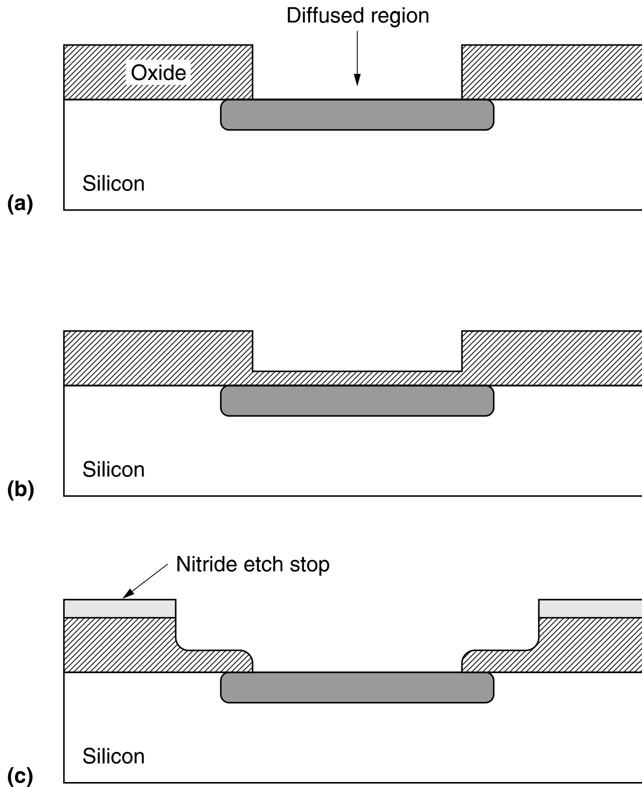

Figure 3.28 Method of forming a diffused resistor without enlargement of the resistor contact area. (a) A contact is opened in the oxide and the exposed Si diffused with an appropriate dopant. (b) The structure is oxidized to form a thin oxide coating on the diffused region. (c) A patterned nitride layer masks the field oxide while the oxide over the diffused region is etched, forming a structure for metallization that is confined to the resistor area. (From Martin, R.C., U.S. Patent 3,468,728, 1969.)

cermet also served as an adhesion layer to Cu. Additional material on cermet barriers can be found in Section 3.6.1.3 on the use of Cr–Cr_xO_y.

3.5.1.4 Metal-to-Metal Contacts

Lowry and Smith (1972) proposed using a three-layer structure consisting of Ni–Cr, followed by Ni–Cr–Ag, followed by a conductive layer of Ag for making ohmic contacts to Si. They chose materials in the stack so that one or more elements in each layer were common to those in adjoining layers, in the anticipation of providing good adhesion and low-resistance contacts from the uppermost conducting layer down to the Si surface. We presently recognize that Ag would not be considered an appropriate choice for BEOL applications because of its high susceptibility to corrosion and its degradation of dielectrics like SiO_2. It migrates freely through the glass network causing shifts in gate threshold voltages and promotes growth of dendritic Ag that shorts conductors through intervening dielectrics.

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3.5.1.5 Amorphization of Si

Jaffe and Penton (1979) patented a method of contact formation that involved amorphizing the c-Si layer by ion implantation. An Al layer could then be deposited on the a-Si to form the contact structure. The amorphization and doping of the Si could be accomplished in one step using ion implantation of As at an energy of 180 keV and a dosage of $10^{15}/cm^2$. An advantage cited for this approach is the reduction of pitting because of the lower accumulation of Si in Al due to the amorphization of Si. It appears likely that the utility of this approach stems from suppression of kinetics of dissolution of Si. From a thermodynamic viewpoint, the higher energy state of amorphous Si vs. crystalline Si would favor more dissolution into Al instead of less.

3.5.1.6 Laser Annealing

Chen et al. (1981) described two ways to improve contact stability to submicrometer poly-Si which involved: (1) use of W/Ti contact metallization; and (2) use of laser annealing to sinter Al/poly-Si contacts. The R_c values of the W/Ti contacts were comparable to furnace-annealed Al/poly-Si but interdiffusion was avoided. Resistance values for the laser-annealed Al/poly-Si were the lowest of all and there was essentially no atomic intermixing. For both the furnace-annealed Al and W:Ti contacts, ρ_c values of $2.4 \times 10^{-5}\ \Omega\ cm^2$ were obtained, but for the laser-annealed Al contacts, the much lower value of $3.6 \times 10^{-6}\ \Omega\ cm^2$ was obtained. The P-doping level in the poly-Si film was approximately $10^{19}/cm^3$.

3.5.1.7 TiN/Ti Contacts

Ting and Crowder (1982) investigated the electrical properties of Al/Ti and Si/Al/Ti metallizations on n^+-Si on contacts that were ~1 μm^2. They found that the value of ρ_c of these structures was much lower than that of Pd_2Si. The measured value of 15 Ω for R_c corresponds to a ρ_c value of $1.5 \times 10^{-7}\ \Omega\ cm^2$. A summary of their results is given in Table 3.1 together with those of other investigators.

Similar ρ_c values for Al/Si contacts were reported by Hara et al. (1983) using halogen lamp rapid heating to sinter the contacts. Their ρ_c values were $1.5 \times 10^{-7}\ \Omega\ cm^2$ for a heat treatment at 950°C and B-implant doses of $4 \times 10^{15}/cm^2$. In yet another rapid annealing technique, Chen and Rensch (1983) investigated electron-beam sintering for reducing R_c for VLSI applications. For contacts that were 1 μm^2, and metallized with refractory metals, the observed ρ_c values ranged from 1.2×10^{-7} to $1.5 \times 10^{-7}\ \Omega\ cm^2$ for p^+ and n^+ doped contacts, respectively. Forming gas was used to anneal out any electron beam-induced damage in MOS devices. No metal–Si interdiffusion was seen.

A Mo/Ti double-layer contact was used by Kim et al. (1985). The Ti layer was used as the contact to Si to reduce the native oxide and Mo was used as the interconnecting layer. The layers were sputtered in sequence in the same pump-down. The ρ_c values for contacts to n^+ and p^+ Si were 1.0×10^{-7} and $1.9 \times 10^{-7}\ \Omega\ cm^2$, respectively. The high temperatures needed to cause the onset of electrical degradation of n^+ contacts (650°C) and p^+ contacts (600°C) was evidence of the high thermal stability of the contacts. RTA of Ti and Ti–W metallization on Si was investigated by Mueller and Kalkur (1989) who used R_s, ρ_c, surface morphology, *I–V* properties, and x-ray diffraction measurements. The study concluded that both Ti and Ti–W metallization had good ohmic properties up to 900°C.

The structural and electrical integrity of stacked electrodes consisting of W/TiN/poly-Si (n^+ and p^+)/SiO_2/Si which have high conductivity and provide dual work function capability, as required for CMOS circuits, was studied by Pan et al. (1989). The TiN films were thought to be effective barriers to diffusion because there was an absence of any silicide formation, even after

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annealing at 1000°C for 30 min and they detected very little dopant diffusion from the poly-Si into the overlying W film using Auger profiling. Moreover, the electrical properties of the 10 nm SiO_2 film that underlies the W/TiN/poly-Si stack were quite good. Evidence cited for this conclusion was stable flatband voltages, low interface state densities, and tightly distributed breakdown voltages.

Onuki and Nihei (1995) used a switching bias sputtering, i.e., alternating between standard and bias sputtering, to improve step coverage for W metal deposition into contact holes that were 0.3 μm wide and 1.0 μm deep. The authors state that their process results in low values of ρ_c for both n^+ and p^+ Si and does not produce damage during deposition. They obtained values of 20 and 35 Ω for n^+ and p^+ Si, respectively, for a 0.6 μm contact hole.

Chin et al. (1995) described a self-aligned process for a contact diffusion barrier in which N_2 implantation converted a portion of the Ti to TiN which then served as a diffusion barrier. Figure 3.9 shows a conducting contact layer such as Ti patterned on a contact structure.

In a similar vein Hindman et al. (1993) deposited Ti into a BPSG S/D contact hole by sputtering and then introduced nitrogen into the sputter chamber to deposit a sputter TiN barrier layer onto the Ti layer. Liu et al. (2000) further refine the contact procedure by (1) substituting CVD TiN for the sputtered TiN and (2) adding a CVD SiON etch-stop layer at the bottom of the BPSG layer. The CVD TiN provides superior step coverage to the sputtered films. The SiON etch-stop layer minimizes damage to the substrate during contact etch and is more conformal than PECVD Si_3N_4

3.5.2 Self-Aligned Structures

A self-aligned method was highlighted in an early patent for fabricating transistors from Schottky contacts (Triebwasser, 1980). A MESFET structure, in which the gate is formed by a Schottky diode instead of a MOS field effect structure, was proposed for high-density integrated circuit applications. A schematic of this structure is shown in Figure 3.29 at an intermediate step prior to completion. It illustrates the novel feature of using a thermally grown oxide to space the source and drain equally from the gate. Evaporated poly-Si provided the source and drain contacts and any one of several metals or silicides could form the FET gate.

Self-alignment is highly advantageous since it avoids the additional area requirements for the overlay tolerances of the masking step. It also tests the creativity of the process designer to provide all necessary processing with one less masking level at his or her disposal. Selected sequential steps for a typical self-aligned structure used for present FET fabrication is shown in Figure 3.30. This process shows: (A) growth of the gate oxide defined by a field (or isolation) oxide; (B) masking of the source/drain ion implant by the gate stack to produce a self-aligned structure; (C) growth of

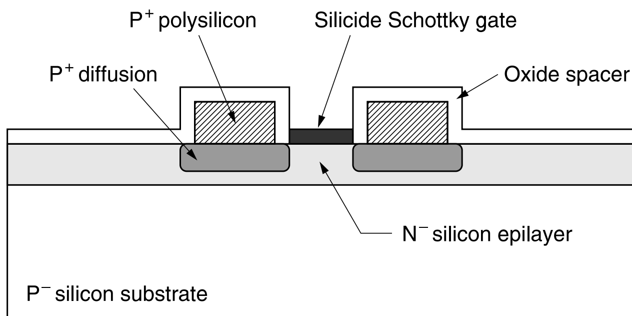

Figure 3.29 Self-aligned structure used for forming MESFETs for high-density integrated circuits. An oxide grown on poly-Si source and drain pads forms the spacer separating the gate from either the source or the drain. (From Triebwasser, S., U.S. Patent 4,222,164, 1980.)

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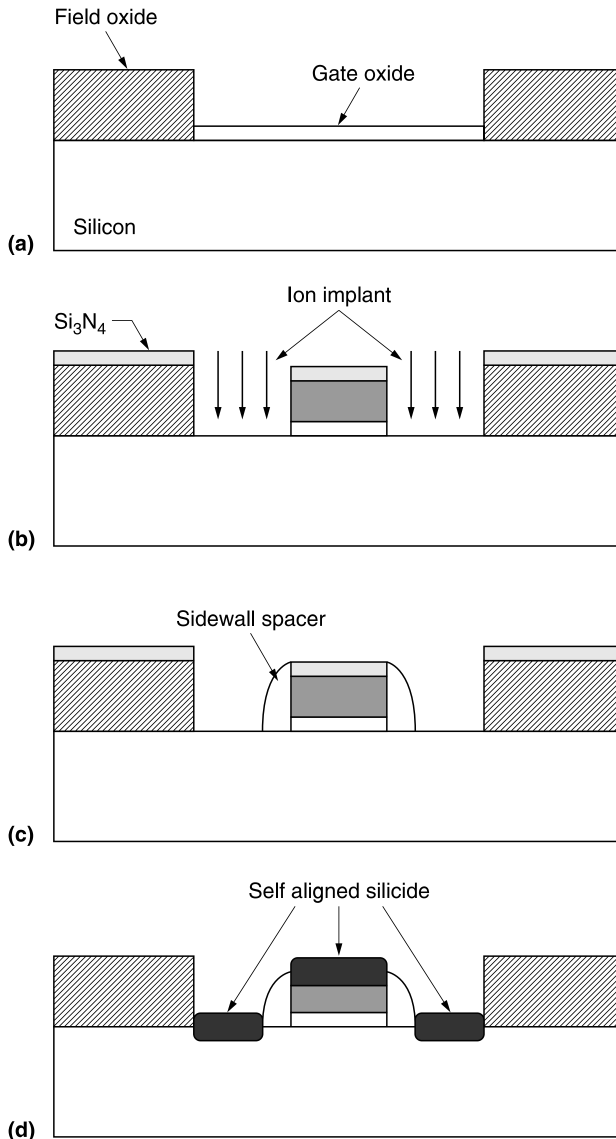

Figure 3.30 Typical self-aligned process for building FET devices. (A) A patterned opening to Si is oxidized to form a thin gate oxide. (B) The gate stack masks the gate area from ion implant of dopants, forming a source and drain that are self-aligned to the gate. (C) Vertical sidewalls are formed on the gate stack by a process of deposition of a conformal oxide film followed by a directional etch of the film from the horizontal surfaces using reactive ion etching. (D) Silicide is self-aligned to the exposed Si in the source and drain contacts and poly-Si in the gate contact by blanket deposition of Ti, sintering to form $TiSi_2$, and removal of the unreacted Ti.

sidewall spacers on the gate stack by conformal oxide deposition followed by RIE removal; (D) growth of self-aligned silicide (salicide) in the exposed poly-Si or silicon surface by a process of sputtered metal (Ti) deposition, sintering, and strip of unreacted metal.

Lavery et al. (1987) described another creative use of the different oxidation properties of doped vs. undoped Si and poly-Si. It provided a way of forming an insulating layer on the poly-Si gate without significant oxidation of the exposed source and drain regions. This is consistent with being a self-aligned process since it avoids the need for a separate contact opening masking step needed

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when a thick oxide develops on the source and drain. They used buried ion implants in the source and drain regions that were also self-aligned to a poly-Si gate contact that served as an implant mask (Figure 3.31a). The proper choice of the energy of the implanted ions placed their peak concentrations at the desired depth below the Si surface in the source and drain contact regions. The surface regions of the source and drain were thus lightly doped, but a P-diffusion step highly doped the gate region (Figure 3.31b). Since the thermal oxidation rate increases with doping, a thicker oxide grew on the gate poly-Si than on the source and drain when the structure was oxidized thermally. This effectively keeps the source and drain open while electrically isolating the gate from subsequent source and drain metallizations (Figure 3.31c). This ion implant process, in conjunction with other process changes, avoided the need for overlay tolerances and thus produced ROM structures requiring 25% less space. A schematic of the process appears in Figure 3.31.

Lin et al. (1994) also patented a method for forming self-aligned contacts for MOSFET structures by using endpoint detection layers of silicon nitride or silicon oxynitride for opening contacts by plasma etching. This allows for less loss of field oxide in etching, and for incorporating a lightly doped drain spacer etch process. Hodges and Sundaresan (1995) patented a process for forming self-aligned lightly doped drain (LDD) structures and low-resistance contacts. A low-resistance ohmic contact between n- and p-type poly-Si occurred because of the formation of an intervening refractory silicide. A $TiSi_2$ layer consumes a portion of both poly-Si layers, forming ohmic contacts with each type of poly-Si, thereby eliminating the rectifying p–n junction that would otherwise exist between the two poly-Si layers. This structure is shown in Figure 3.32 where Figure 3.32a shows overlapping n- and p-type poly-Si layers and Figure 3.32b shows $TiSi_2$ formation that consumes entirely the n-doped layer and a portion of the p-doped layer, effectively removing the rectifying junction.

3.5.3 Contact Processing

3.5.3.1 Etching

Contact processing starts with some sort of contact opening step, usually RIE. In this process the Si surface is bombarded with energetic ions once it is exposed after the overlying dielectric film is removed. These are implanted into the silicon lattice and create a wide variety of point defects that are electrically active, functioning primarily as recombination centers for electron–hole pairs. To form well-functioning contacts, it is important, therefore, to minimize induced damage and to anneal any remaining damage where possible. With the use of CMP for planarizing dielectrics and for defining "damascene" or embedded contacts and interconnections, mechanically induced damage can occur in Si or dielectric films as well as ion damage.

With CMP as the one possible exception, present integrated circuit processing avoids causing the overt, mechanical damage investigated by Johansson and Schweitz (1988). These investigators characterized various types of mechanical damage in c-Si using cross-sectional transmission electron microscopy. Damage resulted from indentation, controlled scribing, particle impact, grinding with fixed abrasive, and polishing with free abrasive, the latter being relevant to scratching by foreign or oversized (agglomerated) slurry particles during CMP. Even in the free abrasive case using 12 μm diamond particles, there was little observable damage and it extended only a few percent of the particle diameter into the substrate. The shallow depth of damage, 50 nm, precluded the authors from determining the precise defect type. The surface deformed plastically and without evidence of spalling that occurred, for example, with fixed abrasives. The inference here is that this extent of damage, though relatively small, is still sufficient to disrupt device and circuit operation. With the increasing use of CMP, problems relating to incidental damage to Si and/or SiO_2 by scratching become of paramount importance for achieving yield targets.

Misra and Heasell (1989) reported on damage created by reactive plasma-assisted etching of p^+–n diodes with CF_4–O_2 mixtures. Using p–n junctions as test devices, these authors showed that

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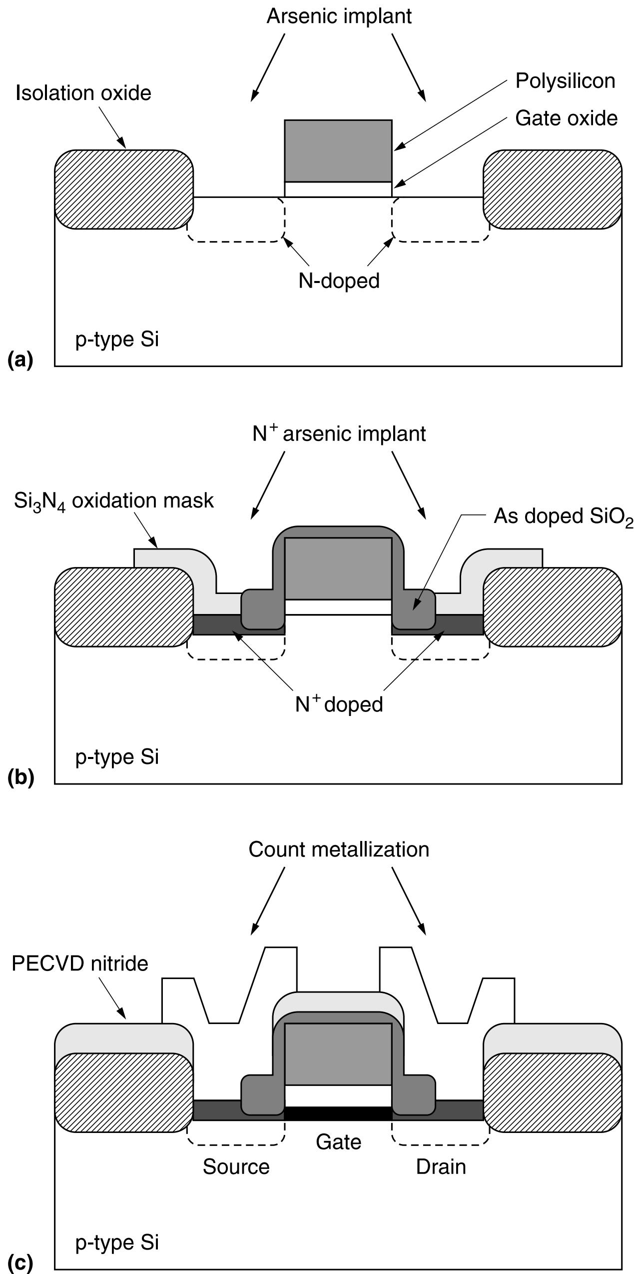

Figure 3.31 Use of oxidation properties of Si and poly-Si in a self-aligned process. (a) The gate stack masks the gate area from ion implant of dopants, forming a source and drain that are self-aligned to the gate. (b) A patterned nitride mask prevents oxidation of portions of the source and drain so that, following oxidation, a relatively thick oxide is formed immediately next to the gate stack. This oxide functions as a mask for an N^+ arsenic implant to reduce the source and drain doping close to the gate and allows more dopant elsewhere to reduce series resistance in the source and drain regions. (c) Nitride is stripped from the source and drain regions and contact metallization is applied. (From Lavery, J., M.B. Armstrong, and H.S. Gamble, IEEE *Trans. Electron Dev.*, ED-34, 1039, 1987.)

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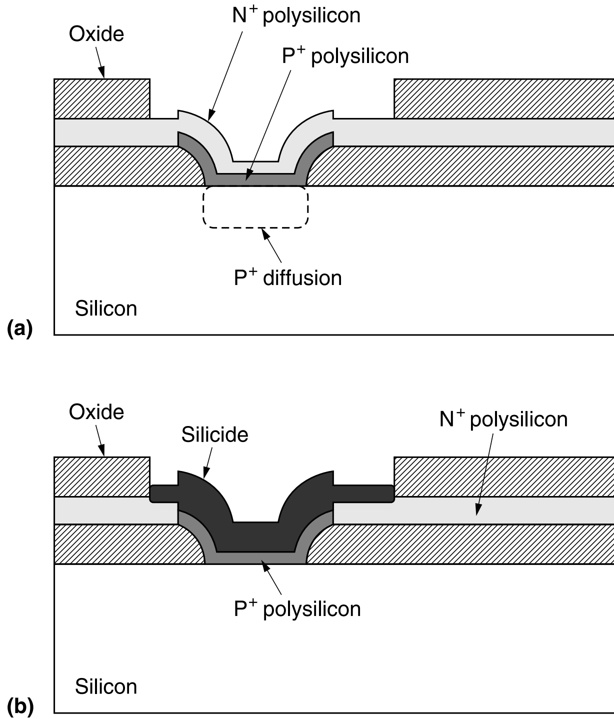

Figure 3.32 Low-resistance contact between n- and p-type poly-Si formed by an intervening layer of $TiSi_2$. (a) A structure with overlapped N^+ and P^+ poly-Si. (b) Silicide formation that fully consumes the top layer (N^+ poly-Si) and a portion of the bottom layer (P^+ poly-Si). This eliminates the rectifying junction that would otherwise exist, allowing an ohmic contact between the two layers. (From Hodges, R.L. and R. Sundaresan, EP Patent 0,632,492 A2, 1995.)

increased recombination currents and a degraded ideality factor altered the forward *I–V* characteristics. They used two types of test specimens, those with junctions exposed directly to the RIE and reference diodes with junctions covered by an oxide layer during RIE. These structures behaved altogether differently, the directly RIE-exposed junctions were highly degraded but the covered reference junctions were virtually unaffected. For the exposed junctions, the magnitude of the damage-induced recombination currents increased with increased bias voltages that ranged from 600 to 1000 V during RIE. Thermal annealing at 450°C did not fully recover their initial properties, although junctions experiencing the lowest RIE bias voltage of 600 V recovered substantially more than those etched at 800 and 1000 V. Reverse bias characteristics permanently changed except for the 600 V RIE bias samples that showed partial recovery after annealing, indicating that a typical BEOL annealing step can modify, but not eliminate the defect complexes. Facing similar concerns, Tsukada et al. (1993) studied the physical damage induced in Si by helicon-wave plasma etching. These authors exposed Si surfaces to helicon-wave O_2 plasma at different helicon-wave and bias powers. Their assessment of Si lattice damage involved RBS, TEM and photoacoustic displacement (PAD). They found that a low damage level occurred by using the combination of high helicon-wave and low bias powers, to produce low bias voltages on the sample.

In another example of damage due to contact etching, Awadelkarim et al. (1994) investigated damage in Si substrates resulting from high-selectivity etching processes. They compared magnetically enhanced RIE (MERIE) and conventional RIE using two combinations of etchants and

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substrates. Samples of SiO_2/Si were etched with CHF_3/O_2 and bare Si with CHF_3/Ar. Each etchant–substrate combination was processed in both the MERIE and RIE reactors. All four experimental conditions produced similar types of damage that were cited as: (1) electronic states in the band gap; (2) H permeation into Si; and (3) deactivation of B acceptors. They ascribed the gap states to interstitial-related defects. These arise from Si interstitials, e.g., Si knock-ions generated by the etching process. Simultaneously, during etching, H from the plasma-dissociated CHF_3 was postulated to permeate into and passivate deep levels in Si. In a controlled experiment, the passivation or deactivation of B acceptors increased with increasing magnetic field for the MERIE etch process using CHF_3/O_2 which was interpreted as evidence for H passivation, since the ion flux incident on the wafer increased with the field. DLTS measurements detected hole traps with activation energies of 0.40 and 0.65 eV for hole emission. The trap at 0.40 eV was identified as the carbon–interstitial oxygen–interstitial defect undergoing a +/0 charge transition and the trap at 0.65 eV as the Si di-interstitial.

Chien and Ashok (1986) employed a controlled damage study to investigate the influence of Si defects on Schottky behavior. Removal of the near-surface region, consisting of a few tens of nanometers, had no effect on the ϕ_B of the damaged Al/p-Si contact but removal of > 100 nm restored ϕ_B to its predamage value.

3.5.3.2 Contact Cleaning

Sung et al. (1995) analyzed, using TEM and thermal wave spectroscopy (TWS), the damage to Si surfaces caused by dry etching in a Cl_2 plasma in an ECR system and also measured the characteristics of Schottky diodes formed on the damaged Si surfaces. They found several correlations between the electrical measurements and the structural analysis such as an increase in the ideality of diodes from 1.08 to 1.90, a decrease in the breakdown voltage from 60 to 6 V, an increase in the defect density from 3.6×10^{10} to $1.0 \times 10^{11}/cm^2$, and a decrease in the damage layer thickness from 134 to 91 nm, all occurring as the power increased from 50 to 500 W. Nogami et al. (1994) observed that suboxides, i.e., Si-rich oxides, formed on the bottoms of contact holes in which the Si surfaces had been damaged by dry etching. Dilute HF could not remove these oxide layers and they also noted that a 1.3 nm thick oxide present at the poly-Si/Si interface increased the contact resistance.

3.5.3.3 Contact Metrics

Kado et al. (1993) successfully measured the detailed topography of contact holes with an AR = 1.5 using atomic force microscopy (AFM), in which a ZnO whisker probing tip was used in a hopping mode to obtain topographic data under a constant repulsive force at each measuring point.

3.5.4 Local Interconnection

3.5.4.1 Interconnection

Miller and Wei (1991) patented a method of producing low-resistance contacts in which patterning of the silicide and underlying adhesion layer defined the interconnection. Lee and Yu (1994) later patented a similar concept but applied it to the formation of contacts in source and drain regions. In the later process, Lee and Yu (1994) first formed a dielectric layer with an overlying poly-Si conductor and then patterned it to expose the semiconductor substrate. Next, they deposited a blanket silicide layer over the whole structure and again patterned it using an oxide hard-mask.

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3.5.4.2 Substrate Contacts

Jerome and Marazita (1992) patented a method of forming substrate contacts that involved the use of doped poly-Si to form a connection between a channel stop region and the substrate. Substrate contacts provide an electrical connection between the c-Si substrate and an external circuit that maintains the substrate at a constant potential. Substrate contacts are necessary because integrated circuit devices will not function properly unless the substrate is maintained at some predetermined potential. One of the processes described in the patent that produces a silicided substrate contact appears in Figure 3.33.

Chou and Chao (1993) described a method for forming transistor contacts that used poly-Si to form buried contacts, gate contacts, and as an implantation mask for the source and drain regions. Buried contacts are contacts to Si that, once formed, are no longer accessible for interconnection by subsequent layers of metallization. They provide circuit connections to the substrate to establish the reference potentials. Moreover, local wiring at the device level improves the density and/or speed of circuits. In the instance cited above, several possible applications stemming from the integration of two patterned levels of doped poly-Si were demonstrated.

3.6 ACTIVE DEVICE CONTACTS

The present use of Schottky diodes in integrated circuits includes discrete circuit elements such as: (1) clamps to prevent the emitter currents from reaching saturation levels; (2) protection for diodes in FETs; and (3) high-frequency circuit elements. Table 3.2 contains a summary of the SBD measurements reviewed here. There have been several attempts to utilize these rectifying contacts as one or more of the three ports of field effect or bipolar transistors. For example, in a patent assigned to A.G. Siemens Corp. (Siemens, 1973), Schottky contacts were tried as bipolar transistor elements, providing the function of collector and emitter, with an epitaxial semiconductor region, doped oppositely from the substrate, functioning as the base. The rectifying contacts could consist of Al, Ti, Pt, Rh, Pd, Co or a silicide thereof. In other examples with a different type of transistor, Drangeld et al. (1971) used Schottky diodes (i.e., Al/Si) as gates in field effect transistors. Use as Schottky diode contacts by PtSi, AlSi and TiW is discussed in Section 3.4. Some of the other materials that can be used for active device contact are presented here.

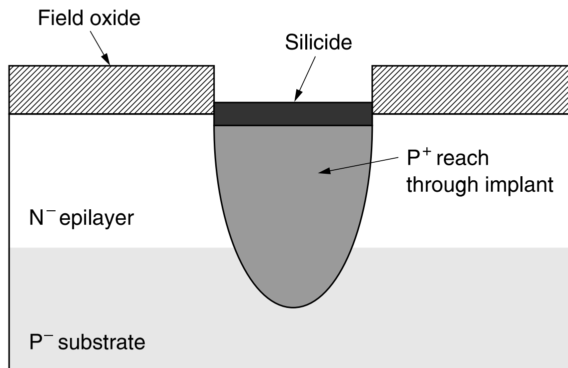

Figure 3.33 Silicided substrate contact. An implant of B reaches through the N^- epilayer to reach the P^- substrate.

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Table 3.2 Barrier Height Values

Barrier Height (eV)		Contact Structure			Conditions			Sources	
High	Low	Metal	Silicon	Doping	T (°C)	Method	Note	Author	Year
0.64	0.49	Al	Si				Ion/Impl't	Ohta	1989
0.70		Al	Si	n-type	300			Card	1976
0.90		Al	Si	n-type	550			Card	1976
0.50		Al	Si	p-type	300			Card	1976
0.35		Al	Si	p-type	550			Card	1976
0.62		Al	Si(111)	n-type				Hoekelek	1978
0.84	0.72	AlCu	Si	n-type		quenched		Bhatia	1976
0.65		B-$NiSi_2$	Si(111)	-type			>50 nm	Kikachi	1988
0.89	0.61	$CoSi_2$	Si(111)	p-type				Fathauer	1988
0.38		Gd	Si					Suu	1986
0.39	0.15	IrSi	Si	p-type				Tambe	1991
0.68		$MoSi_2$			550			Yamamoto	1985
0.76		$NiAl_3$	Si(111)	n-type				Hoekelek	1978
0.79	0.78	$NiSi_2$	Si(100)				<50 nm	Kikachi	1988
0.55		PtSi	Poly-Si	n-type		Columnar prefered	$n = 2.0$	Sagra	1991
							$n = 1.2$	Sagra	1991
0.39	0.15	PtSi	Si	p-type				Tambe	1991
0.64		$Ti_{73}Co_2$,	Si	n-type			$n = 1.06$	Gromov	1995
0.55	0.52	$TiSi_2$	a-Si	n-type	450			Liauh	1993
0.59	0.57	$TiSi_2$	a-Si	p-type	450			Liauh	1993
0.52		$TiSi_2$	Si	n-type				Mallardeau	1989
0.61		TiW	Si	n-type				Babcock	1986

3.6.1 Materials

3.6.1.1 Cr–Cr_xO_y/Ta

A method of fabricating a low-voltage (i.e., 0.5 eV) Schottky barrier was described by Dalal et al. (1980) which involved evaporating Ta/Cr–Cr_xO_y/AlCu through a lift-off mask. The Ta/Si interface provided the rectifying contact and the Cr–Cr_xO_y cermet was the diffusion barrier to inhibit the reaction between AlCu and Ta. By forming selected PtSi contacts prior to evaporating the metallization layer, a combination of both low- and high-voltage Schottky contacts, together with ohmic contacts, could be formed on a single contact level. In this process, Ta was evaporated first, followed by Cr–Cr_xO_y. The Cr–Cr_xO_y layer was formed by e-beam evaporation of Cr as water was bled into the evaporator. A detailed process for evaporating transition metals to form low-barrier Schottky diodes was described by Dalal and Lowney (1983); this involved a series of steps to be used for degassing the charge while it is melting, as well as the wafer and evaporator itself, to ensure a deposit of high quality.

3.6.1.2 Al/NiSi

In a study of the reaction of the Al/NiSi contact structures on n-type (111)Si, Hoekelek and Robinson (1978) showed that a NiSi phase was formed in the contact with $\phi_B = 0.62$ eV.

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After sintering the NiSi in contact with a thin Al overlayer, $NiAl_3$ formed which had $\phi_B = 0.76$ eV with Si. The electrical characteristics of the $NiAl_3$ layer were stable up to 500°C with no evidence of Al penetration into the substrate.

3.6.1.3 $TaSi_2$

The application of cosputtered amorphous and polycrystalline $TaSi_2$ for contact metallization was evaluated by Neppl and Schwabe (1984). They found that the atomic transport of Al and Si across the silicide was impeded up to 475°C if the silicide was metal rich. Metal-rich $TaSi_x$ provided low contact resistance and low Schottky barriers to n-type Si with minimal Si consumption.

3.6.1.4 $MoSi_2$

The value of ϕ_B for $MoSi_2$, formed by sintering a Mo film in contact with Si at 550°C, was determined to be 0.68 eV by Yamamoto et al. (1985). They further investigated the thermal stability of the layer in contact with Al–2% Si and found it good up to 500°C. The value of R_c for the poly-Si/$MoSi_2$/Al–2% Si structure was found to be 6.0×10^{-7} to 7.0×10^{-7} Ω cm^2 which matched that of a poly-Si/Al–2% Si contact.

3.6.1.5 Intermetallics

Intermetallic compounds of Al and transition metals can be formed into stable materials for use as Schottky barrier contacts by a process disclosed by Howard et al. (1982). In their process, Ta and Al can be evaporated sequentially without breaking vacuum in the desired proportions to form an intermetallic compound. Subsequently, photoresist techniques, together with chemical etching, are used to pattern the Ta/Al bilayer. After stripping the photoresist, the bilayer is sintered to form the intermetallic compound.

3.6.1.6 Selective CVD W

Selective metal deposition could have significant advantages for contact processing. It places the desired metal film directly into the contact and requires no additional processing to remove the excess or overburden of material elsewhere on the chip as occurs with nonselective, blanket metal depositions. For example, Gargini (1983) used a selective CVD process to deposit W into contact openings to provide a diffusion barrier only on the Al–Si contacts. Besides gaining obvious process efficiency, this showed that selective CVD W also provides an effective diffusion barrier for VLSI applications.

With strong incentives such as possibly improved yields, reduced processing time and costs, etc., the absence of this potentially high leverage process in manufacturing deserves mention. The Achilles' heel of selective CVD is the apparent vulnerability to incomplete cleaning of contact holes which will prevent metal deposition and create an open contact. While this can happen to some degree with blanket CVD, physically vapor deposited (PVD) nucleation layers such as sputtered TiN will coat all surfaces and provides a reasonably pristine surface for blanket CVD. In effect, for the incompletely cleaned contact, the apparent tradeoff is an open, nonfunctional contact for selective CVD vs. a functional, but possibly more resistive one, for blanket CVD. Until the quality of Si surfaces in all contact openings can be guaranteed to be free of nonnucleating films, it is unlikely that selective processes will be used to any great extent in IC manufacturing. Additional processing-related information is contained in a recent study of the selective CVD of tungsten metal on Si followed by ion beam mixing via As implant to form WSi_2 diodes (Saraswat et al., 1984).

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3.6.1.7 $CoSi_2$/$NiSi_2$ as Schottky Barrier Diode Contacts

Advanced molecular beam epitaxial film growth techniques for Co and Ni silicides were utilized by Fathauer et al. (1988) to produce $CoSi_2$ layers on p^+-doped Si(111). Prior to growing the $CoSi_2$ layer, a fresh Si surface was created by *in situ* epitaxial growth of p^+ Si on to the Si(111) wafer surface. Measured values of ϕ_B ranged from 0.61 to 0.89 eV, depending on the thicknesses of the epitaxially grown p^+ layer. Interfaces between single-crystal $NiSi_2$ and Si, of both (100) and (111) orientations, produced by codeposition of Ni and Si on the appropriately oriented Si substrate, were analyzed by Kikuchi et al. (1988). For $NiSi_2$/Si(100), ϕ_B was 0.65 eV, independent of the silicide thickness. For type-B $NiSi_2$/Si(111), where the term "type-B" refers to a twinned structure, resulting from a 180° rotation about the surface normal to the orientation of the Si(111) substrate, ϕ_B was found to be dependent on $NiSi_2$ thickness, becoming constant at 0.65 eV for silicide thicknesses at or exceeding 50 nm. A value for ϕ_B of 0.78 to 0.79 eV was estimated by extrapolation to a thickness of $NiSi_2$ of 1 to 2 atomic layers.

The temperature and pressure dependencies of Schottky barrier heights on Si for a variety of contacts (Ti, W/Ti, PtSi, Pd_2Si, IrSi, $CoSi_2$, $TiSi_2$, Sm, and $NiSi_2$), some of which were epitaxial ($NiSi_2$/Si(111), types A and B) or faceted ($NiSi_2$/Si(100)), were investigated by Werner et al. (1993). In contrast to the type-B twinned epitaxial relationship between $NiSi_2$ and Si(111), type A refers to a $NiSi_2$ that is identical in orientation to the underlying Si(111). From the analysis of epitaxial $NiSi_2$/Si diodes, it was concluded that there is a direct correlation between interface crystallinity and both the value of ϕ_B and its temperature dependence. Additionally, both pressure and temperature coefficients of the polycrystalline Schottky contacts correlated with the same coefficients for the band gap, indicating that the thermal emission model fully accounted for the observations of ϕ_B.

A novel method of combining both $CoSi_2$ Schottky barriers and TiN diffusion barriers was investigate by Gromov et al. (1995) who utilized a TiCo alloy which was sintered in contact with Si at temperatures of 800 to 850°C to form $CoSi_2$/Si contacts (Schottky and ohmic) together with a TiN barrier layer. On n-type Si, the value of ϕ_B and the ideality (n) for an annealed $Ti_{73}Co_{27}$/n-Si contact were 0.64 eV and 1.06, respectively. Ohmic contacts to n-type Si had a value of ρ_c of $5 \times 10^{-7}\ \Omega\ cm^2$ and to p-type Si, $1 \times 10^{-6}\ \Omega\ cm^2$.

3.6.2 Novel Structures

3.6.2.1 Guard Rings

Dreves et al. (1981) disclosed the incorporation of a guard ring as a way to improve Schottky diode performance. Their process employs a peripheral ring or annulus around a diode that follows the diode contour and is directly under a re-entrant ledge in the surrounding insulating layers. A diffusion mask of Mo, evaporated into the contact structure, covered the diode area but not the peripheral guard ring area. Then they diffused the guard ring using a vapor source of the appropriate dopant. Anantha et al. (1987) disclosed a method for making a highly compact, self-aligned guard ring for a Schottky diode. It used the idea of "sidewall spacer technology" invented by Pogge (1981). The essential elements of this process are the conformal deposition of virtually any RIE etchable film over a step followed by directional etching to remove the film from the horizontal surfaces. The film can be a metal, semiconductor, polymer, or inorganic dielectric. The only restriction is that the deposited film has to be distinguishable in its etching characteristics from the underlying step so that it can be selectively removed. In the case at hand, the films of interest for fabricating the self-aligned guard ring are doped poly-Si and SiO_2. The combination of the steps described above creates vertical spacers that adhere to both the vertical sidewall and the bottom circumference of the diode opening. The optional SiO_2 film is the first to be deposited and

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etched, in order to position the diffused zone away from the very edge of the contact opening. The second is the poly-Si film which is processed identically to the oxide, and, upon doping, is the diffusion source for making the guard ring. Ion implantation is typically used to dope the poly-Si with either B or As. The diffusion step takes place by sintering after RIE removal of the remainder of the film. Subsequent deposition of a silicide-forming metal into the contact opening lined with a poly-Si sidewall produced a diode structure that is self-aligned with its guard ring, as indicated in Figure 3.34.

3.6.2.2 Hybrid Structures

Rothman et al. (1981) developed a process for combining sputtered diffusion barriers and low-barrier Schottky diodes into an evaporated, lift-off metallization technique for forming contact level connections on Si devices. For example, a blanket layer of sputtered TiW provided a diffusion barrier for the previously silicided, ohmic contacts and high-barrier Schottky diodes. In the same TiW deposition step, the unsilicided or bare Si contacts become the low-barrier diodes. A lift-off masking structure formed on the TiW surface provided the means for patterning the underlying barrier film. The AlCu conducting metallization was evaporated onto the patterned mask and lifted off to form a desired pattern of AlCu over a blanket field of TiW. RIE with CF_4 removed the exposed TiW except under the AlCu as the masking layer. For comparative purposes, cross-sections of contact structures built by (1) lift-off, (2) combined lift-off and subetch, and (3) subetch are shown in Figure 3.35. For the lift-off case (Figure 3.35a), the barrier layer does not extend fully to the edge of the silicide layer, permitting migration of Al along the side of the barrier down to the silicide, forming Pt_2Al. These metallurgical reactions constitute a well-known precursor to Al penetration. In Figure 3.35b, the sputtered barrier extends over the silicide, offering greater resistance to penetration and the evaporated AlCu allows a greater Cu content than is possible for RIE-defined AlCu. For the subetched structures in Figure 3.35c, the sputtered barrier again extends over the silicide as in case (2) above, but the cleft in the AlCu at the step from the surface of the insulator into the contact hole is minimal as compared to evaporated AlCu indicated in both cases (1) and (2). Because the AlCu is RIE etched, only a relatively low Cu content is tolerable, and on this basis the electromigration reliability of the totally subetched structure would be inferior to cases (1) and (2).

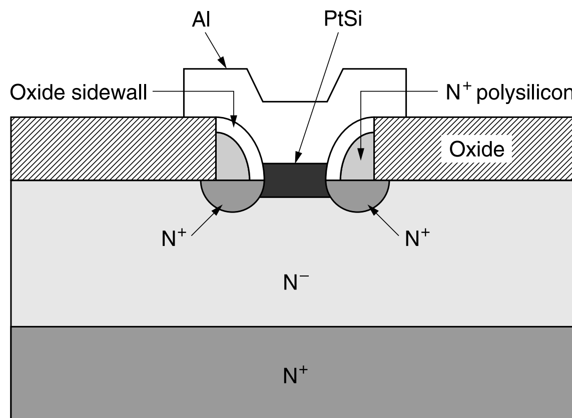

Figure 3.34 Schottky diode with self-aligned guard ring. The guard ring is formed by the out-diffusion of an n-type poly-Si sidewall. (From Anantha, N.G., H.S. Bhatia, S.P. Guar, P. Santosh, and J.L. Maurer, IV, U.S. Patent 4,691,435, 1987.)

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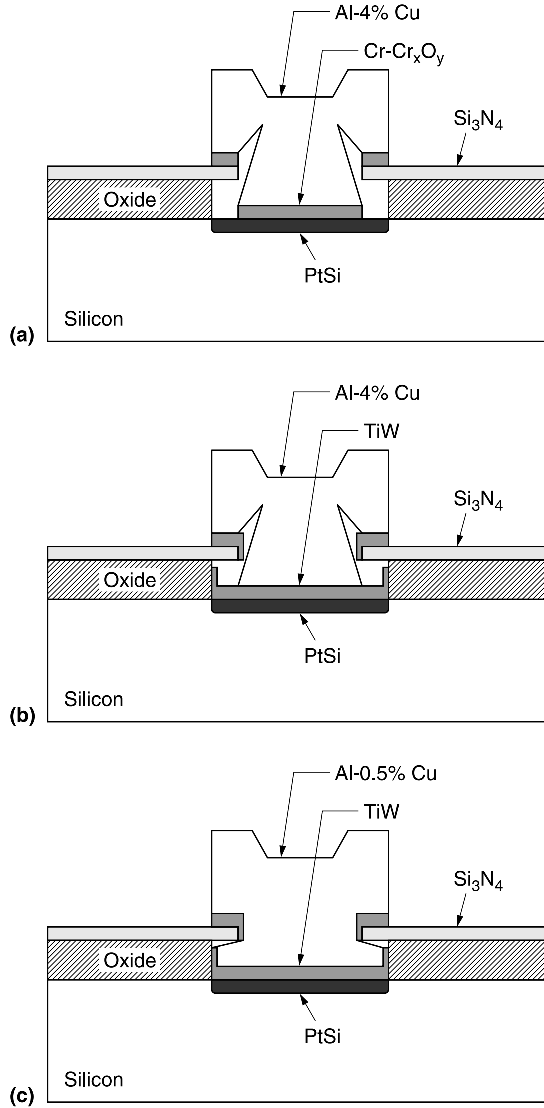

Figure 3.35 Comparison of contact structures fabricated by lift-off, hybrid, and subetch methods. (a) For the lift off case, the evaporated Cr–Cr$_x$O$_y$ barrier does not fully cover the PtSi layer, formed by sintering a sputtered Pt layer. Deep clefts form where the Al metal steps down into the contact hole. (b) For the hybrid case, the TiW barrier provides coverage fully across the silicide, and part way up the re-entrant sidewall. The Al metallization is identical to (a). (c) For the subetch case, the barrier coverage is the same as (b), but the sputtered Al metal has greater continuity as it steps down into the contact opening.

Fortunately, this limitation was eliminated with the introduction of more highly reliable Ti-clad Al–0.5% Cu structures.

3.6.2.3 Resistor and Diode Structures

Schlupp (1983) patented a more complex structure combining both a Schottky barrier and a resistor. This involved the deposition and patterning of a poly-Si layer over an insulator having a contact opening to the underlying Si. By forming a layer of PtSi in the same shape as the patterned

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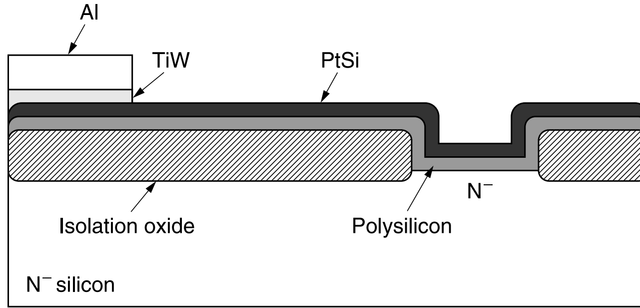

Figure 3.36 Combined Schottky diode and resistor structure using PtSi formed on poly-Si. (From Schlupp, R.L., WO Patent 8,301,866, 1983.)

poly-Si, using a salicide process, he formed the combined Schottky diode and resistor structure shown in Figure 3.36.

This process can also be used for the simultaneous formation of a silicide field plate around the periphery of the diode to improve the reverse electrical breakdown characteristics. Improvements in Schottky barrier diode characteristics described by Bergeron et al. (1982) linked the anode and cathode of a diode on n-type Si by ion implantation of P. They chose the thicknesses of oxide that overlay the adjoining Si regions to mask the P ion implant, to control the peak implant depth. Proceeding in this fashion, they built guard rings and a high-conductivity channel between the anode and cathode while causing only minimal PNP parasitic transistor action.

3.6.3 Some Processing Effects

3.6.3.1 Silicon Damage Effects

Chow et al. (1984) investigated the modification of ϕ_B of Schottky diodes using RIE in NF_3 gas mixtures. They observed that the RIE process caused an increase in ϕ_B for p-Si, and a reduction for n-Si. The introduction of point defects caused by ion bombardment is the likely cause of these effects. In an analogous study, Paz et al. (1984) characterized diodes formed by RF sputtering of TiW onto p-type Si, using such techniques as *I–V* measurements, deep-level transient spectroscopy (DLTS), and electron beam-induced current (EBIC) to support their arguments that sputter damage creates a hole trap at $E_v + 0.35$ eV, a strong recombination center. Straayer et al. (1986) studied the influence of sputter damage on the ϕ_B value of diodes. As a probe of sputter damage, they used Au sputter deposited onto p-Si. The value of ϕ_B of diodes formed using sputtered Au increased over those prepared with evaporated Au, and the increase was dependent mainly on the sputtering voltage. Increases in ϕ_B occurred with sputtering voltages over the range 0.5 to 1 kV, after which they remained fixed. The formation of sputter-induced traps within a thin surface layer (~10 nm) of Si fixed the value of ϕ_B.

Ar^+ ion bombardment of Al/Si contacts redistributes residual SiO_x and this reduces spiking of Al into Si by creating a uniformly reacting surface. Thermal annealing at 350°C increased the average value of ϕ_B from 0.49 eV, postimplant, to 0.64 eV after annealing, which is close to the undamaged value of 0.69 eV. Alpha particle channeling provided direct evidence that very little damage remained after annealing. Ohta et al. (1989) used DLTS to investigate defects associated with evaporated metal contacts to Schottky diodes. They discovered defect levels at 0.16, 0.14, and 0.12 eV below the conduction band and identified wet chemical etching as the origin of the defects. Supporting evidence came in the form of: (1) an increase in the concentration of defects with the amount of Si removed by chemical etching; and (2) a decrease in one of the levels (0.14 eV) with increasing etch rate.

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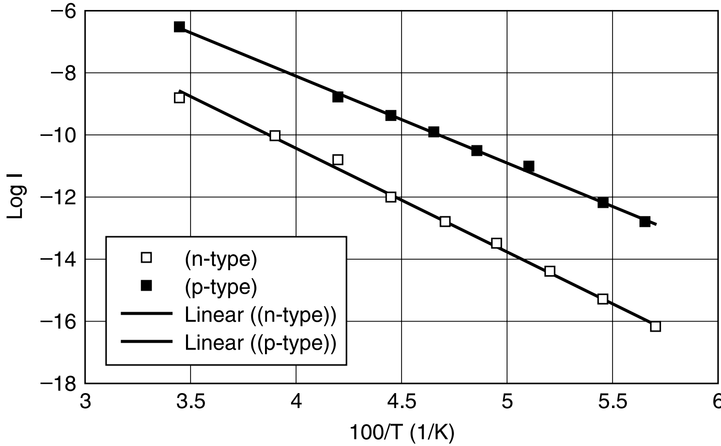

Figure 3.37 Temperature dependence of the forward current for TiW diodes on n- and p-type Si. The barrier height derived from the data on p-type (100)Si (filled squares) was 0.54 eV and for n-type (100)Si (open squares), the barrier height was 0.68 eV. The sum of these barriers is 1.22 eV, which is very close to the Si indirect band gap of 1.20 eV at 0 K. (From Aboelfotoh, M.O., *J. Appl. Phys.*, 61, 2558, 1987.)

After studying the effects of 150 keV implantations as a function of temperature, Malherbe et al. (1992) determined the influence of Ar^+ ion implantation on the *I–V* properties of Cr/p-Si(100) diodes. They found that the Ar^+ ion bombardment resulted in higher values of both n and ϕ_B. Drawing upon an earlier explanation given by Fonash et al. (1981) they argued that the surface damage layer reduced band bending near the surface, indicating that this layer stored a net positive charge.

Altman et al. (1975) patented a novel method for improving the reverse leakage characteristics in metal–semiconductor diode contacts that made use of ion bombardment. They extracted ions from an annular radio frequency (RF) diode that was interposed between the substrate and the evaporation source. After a predetermined exposure to ion impingement at the desired bias, movement of the RF diode structure to an off-axis position allowed an *in situ* deposition of metal. This sputter-cleaning step performed in a custom evaporator described above improved the reverse characteristics of Mg, Al, and Pt diodes on p-type Si. Improvements were the replacement of soft or gradual increase in leakage current with reverse bias by hard characteristics. Hard characteristics consisted of a small reverse current that was virtually independent of bias until breakdown occurred and the current increased abruptly.

3.6.3.2 Hydrogen Effects

An investigation of the etching of Si by MERIE with HBr as the etchant was reported by Nakagawa et al. (1991). After a surface treatment that removed 400 nm of Si by MERIE with HBr, they formed Ti diodes and used *I–V*, *C–V*, and DLTS measurements of these diodes to characterize the damage. They found that permeation of hydrogen was the dominant effect for p-Si, causing deactivation of dopants and an increase in ϕ_B, but for n-Si no such effects were detected. Annealing at 180°C restored the original properties of the diodes formed on p-Si.

3.6.4 Electrical Measurements

Difficulties occur in the measurement of ϕ_B for low-barrier diodes: (1) their relatively low resistance makes it difficult to identify the diode contribution to the overall resistance of the device

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structure; and (2) the recombination current in the diode can be an appreciable part of the total current, making uncertain the extrapolated value of J_0 needed to evaluate ϕ_B. (See Equation 3.4 for an explanation of J_0.) Suu et al. (1986) obtained improved values for low barriers by taking I–V measurements from two front surface contacts of different sizes, where one of the contacts substituted for the usual backside contact. As an example, they measured the value of ϕ_B for Gd/Si contacts and found it to be 0.38 eV.

Tanabe et al. (1991) reported on the spatial nonuniformity of the values of ϕ_B measured laterally across Schottky diodes (PtSi/p-Si, IrSi/p-Si) using internal photoemission. For both silicides, regions with the relatively high ϕ_B value of 0.39 eV coexisted with the anticipated values of 0.24 eV and 0.15 to 0.17 eV usually found for PtSi and IrSi on p-type Si. Inhomogeneities in interfacial defect densities and therefore in Fermi-level pinning produce the two coexisting regions. However, an additional investigation by Aboelfotoh (1991) cast doubt on the spatial fluctuation of barrier heights across a contact. Aboelfotoh (1987), based on his work shown in Figure 3.37, concluded that inhomogeneities must be of the order of the Debye length or less. He drew this conclusion because of the close match between the sum of ϕ_B on n- and p-Si and the band gap. Otherwise, there would be a lowering of the observed values of ϕ_B, making their sum for n- and p-Si consistently less than the band gap.

Sagara and Tamaki (1991) investigated inhomogeneities related to poly-Si grain structures and found that the diode characteristics of PtSi/n-poly-Si structures were quite different for columnar vs. preferentially aligned grains. Columnar refers to a fibrous texture where all the grains nucleate on the substrate such that the length of the grain is typically equal to the film thickness but the diameter is much smaller. (Columnar structures are generally undesirable, having poor step coverage, rough morphology, and an overabundance of high-diffusivity paths making them poor diffusion barriers.) Preferentially aligned grains share a common orientation normal to the substrate surface but are randomly oriented in the plane of the film. They tend to form equiaxed crystallites, with diameters that are comparable to the film thickness. For the preferentially aligned poly-Si on Si(100) studied here, the poly-Si grains also exhibited a significant degree of epitaxy with the underlying c-Si. For columnar structures, $n \sim 2.0$ and $\phi_B = 0.55$ eV, but for the preferentially aligned films, $n = 1.2$ and the values of ϕ_B were dependent on the implanted dose.

3.7 CONTACT STUDS FOR ULSI

Increasingly, the contact to a Si device, whether it is a c-Si, poly-Si, or silicide, occurs through use of vertical connections, referred to as *studs* or in this case contact studs. The need to planarize the topography resulting from the device build and to provide flexibility in contact wiring drive this change, despite the additional process complexity it brings. Extensive discussions of the process for forming studs appear in Chapter 6, and therefore only issues and solutions unique to contact studs appear here. Some of the pairs of these are: etching contact openings through different insulator thickness and use of etch-stop layers, conversion of contacting Si surfaces into silicides, and the use of barriers and borderless, bordered, or self-aligned contacts. Each of these issues modifies the specific processes used in the formation of contact studs. Figure 3.38 illustrates barrier issues, the shortcomings of sputtered barriers including sidewall thinning, poor bottom coverage, and breaks at corners. The superiority of the coverage of CVD liners is also indicated.

Dixit et al. (1989) described a method for forming a stable low-resistance ohmic contact. It involved lining the contact hole with an adhesion layer such as Ti, then with a barrier layer such as TiW, and finally filling the opening with either CVD or sputtered W, or sputtered Mo. The Ti adhesion liner makes a low-resistance contact to Si, and the barrier layer prevents encroachment of Si at the Si/SiO_2 interface. Moriya et al. (1983) used selective CVD W to form contact studs directly on Si and reported, for contact to n^+ Si, values of ρ_c of 8×10^{-7} to 2×10^{-6} Ω cm^2. In a typical fabrication sequence, the selected contacts, diffusions, and/or gate will be typically selectively silicided,

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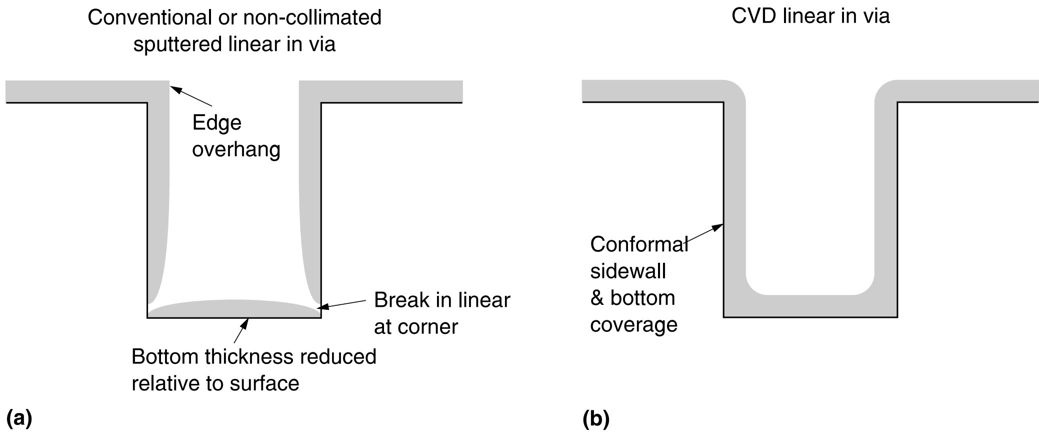

Figure 3.38 Comparison of liner coverage of vias by conventional sputtering and chemical vapor deposition.

followed by the deposition and planarization of the contact level insulator. However, Saito et al. (1993) used selective deposition of CVD $TiSi_2$ to form low-resistance contacts to Si through the contact hole, using a 0.2 μm hole with AR = 2.5. The value of ρ_c of the selective CVD $TiSi_2$ fell in the range of 2×10^{-7} to 6×10^{-7} Ω cm^2. Silane at 720°C was used to preclean the surface prior to the growth of $TiSi_2$ using $TiCl_4$ and silane. Contact stud application usually involves the use of dielectric layers of SiO_2, P, and B/P-doped SiO_2, in conjunction with etch-stop layers of silicon nitride, Al_2O_3, undoped poly-Si, and MgO (Kim et al., 1988).

Borderless contact design allows the contact stud partially to intersect the device contact region, providing design flexibility. Bordered contacts, in contrast, require that the contact stud land fully within the device contact opening. This enlarges the contact window dimensions due to the influence of overlay tolerances. A self-aligned contact process simplifies the process by relaxing the lithographic image size, while providing for maximum contacting surface. Figure 3.39 illustrates contact level studs built on an FET structure where the device level silicide contacts were self-aligned to the gate source and drain. In Figure 3.39a the studs are unbordered with respect to the gate, source, and drain contacts, whereas in Figure 3.39b the studs are bordered.

Bordering requires larger silicide pads to accommodate the stud and at least a 3σ border for the overlay tolerances. This may become clearer after examining Figure 3.40a and Figure 3.40b which show the top view of borderless and bordered contacts, respectively.

Source and drain contacts self-aligned to the gate sidewall insulation provide for precise gate length and therefore consistent device properties. Achieving such a structure requires an etch stop over the gate stack, including its sidewall and cap insulators. After the required overetch, the barrier layer is removed while retaining the sidewall and cap insulators of the gate. This ensures that the neither the source nor drain contact studs short to the gate electrode. A separate etch process is used to open the gate contact. Other variations of this process are possible. Givens et al. (1994) describe an etch process using a high-density plasma to etch 4% PSG in C_2F_6, with a selectivity of 100:1 to PECVD SiN. They followed this by etching SiN in a CH_3F/CO_2 plasma and achieved a 7:1 selectivity over SiO_2, or Si. Gambino et al. (1995) described a contact stud process that involved using a thick Si nitride cap over the gate electrode and oxidizing the gate sidewall. A thinner blanket nitride film conformally coated the device topography and served as an etch barrier for a C_4F_8/CO RIE process with a selectivity of 15:1. A BPSG film was planarized, and borderless contact hole openings were made to the source and drain regions. According to the authors, a 256 Meg

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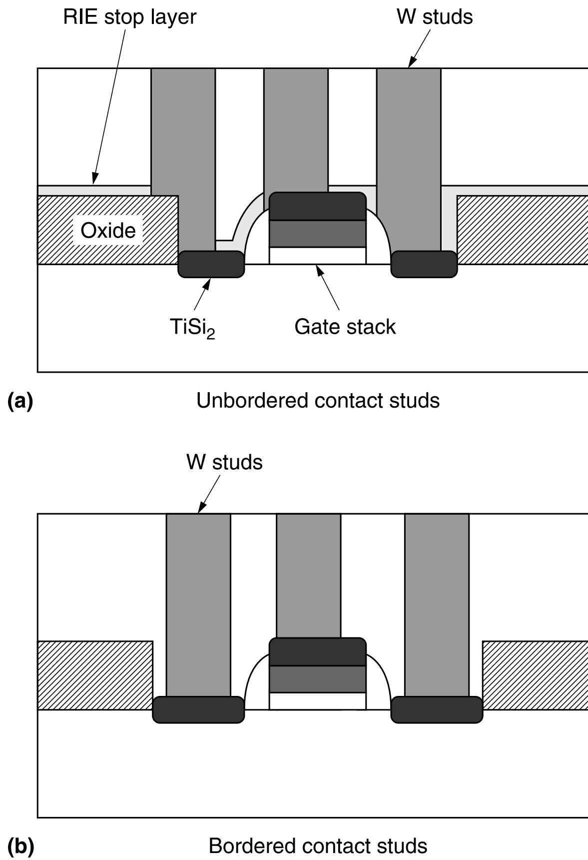

Figure 3.39 Comparison of borderless and bordered contact studs on a typical FET device structure. (a) The borderless case requires a RIE stop layer in order not to damage the device features. (b) For the bordered case, it is assumed that the silicide on the contact provides an adequate etch stop.

DRAM technology incorporates this process at a 0.25 μm minimum feature size. The area of the contact studs and the choice of materials and processes will continue to evolve, driven by shrinking devices and the need to reduce costs.

3.8 CONCLUSIONS

The improvements in contact technology reviewed here have largely taken the form of processes and materials that address the requirements of ever increasing yield and reliability and somewhat less so of electrical performance enhancements. From the earliest structures that employed Al metallizations directly on Si, to the advanced, multilayer processing that so typifies present IC manufacturing, we witness the use of much improved material systems. These can now provide virtually penetration-proof contact structures, highly stable Schottky diodes, and ohmic contacts that consistently approach the theoretical limits. The enhancement of electrical performance is less direct, as the substitution of more conductive materials does not enhance the performance of contacts as it can interconnects, e.g., by the substitution of Cu for Al. However, contacting materials can play a more subtle but still important role by their symbiosis with process design, to

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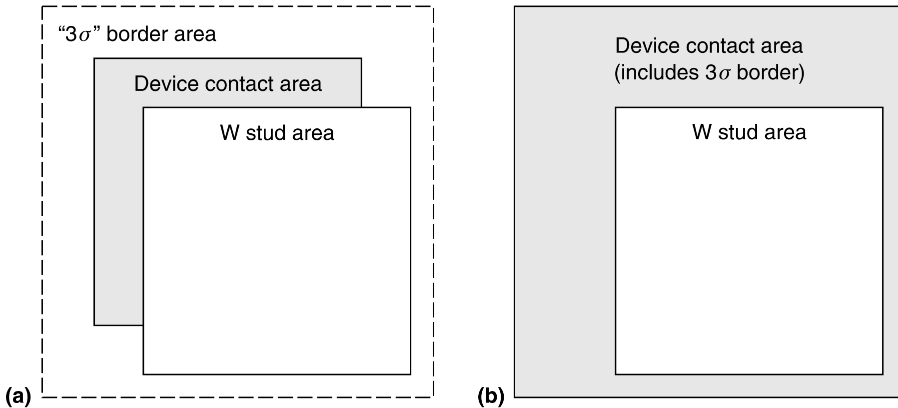

Figure 3.40 Top view schematic of borderless and bordered contacts showing relationship to 3σ overlay tolerance.

make possible self-aligned technologies that improve density, decrease distances, and thereby enhance overall chip performance. Advances in this area will likely be incremental and found more in the areas of improved deposition methods, more consistent material quality, and improved understanding of the rather large material set now at the user's disposal as opposed to the sort of quest for altogether new materials (low-K dielectrics, Cu) now taking place in the interconnections area.

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CHAPTER 4

Interlevel Dielectrics

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4.1 INTRODUCTION

The reduction of signal propagation delay is one of the driving forces behind the use of multilevel device structures and the principal one responsible for the search for improved materials with which to build them. The dielectric layers, the essential insulating components of a multilevel structure, contribute to the delay (RC) through the capacitance term, ε/d, where ε is the dielectric constant of the insulator and d is its thickness. Many recent papers use k as the symbol for the dielectric constant rather than ε. The total capacitance is due to the capacitance (1) between the first-level wires and the Si substrate, (2) between wires on the same level, and (3) between wires on successive levels. While a thick insulator would reduce the capacitance between levels, there are limits due to processing difficulties such as via hole etching and step coverage and/or hole filling capabilities. Also, thicker interlevel insulators increase the intralevel capacitance for a given line-to-line spacing, i.e., the cross-talk between conductors in hole level. Thus, the insulators best suited for the interlevel dielectric layers are those with a low dielectric constant. This chapter discusses both inorganic and organic insulators; SOGs, are also included, as they bridge the gap between both types.

Requirements for interlevel dielectric films, in addition to a low dielectric constant, are (1) high breakdown strength (however, since the average field experienced by the dielectric fills during operation of the device is quite low, this requirement is often exaggerated), (2) low bulk and surface conductivity, (3) low compressive stress (low to minimize wafer warpage and avoid adverse effects on devices and conductors; compressive to prevent cracking), (4) low defect density, (5) good adhesion

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to underlying layers (metals and dielectrics), (6) surfaces to which photoresist and permanent overlying dielectric and metal films adhere well, (7) low moisture content, (8) high resistance to permeation and absorption of moisture (i.e., high film density) and diffusion of mobile ions, (9) stability to chemicals in the processing and use environment and to thermal excursions, and (10) etchability.

The processes used to deposit the films must satisfy several criteria: (1) run-to-run reproducibility, (2) good uniformity within a wafer, (3) wide process window, (4) low contamination due to wafer handling, reactor design, process chemicals, or the conditions used for deposition and etching, (5) compatibility with underlying structures and materials, and (6) no radiation damage, particularly important for MOS devices. The equipment used, particularly for manufacturing, must be reliable. System maintenance should be relatively easy and infrequent. It should be capable of high throughput and occupy minimal floor space in the fabrication facility. In addition, in this era of smaller devices and high packing densities, conformal or planarizing films are required as well as void-free filling of the deep, narrow spaces.

No single material or deposition process satisfies every requirement. Compromises are necessary and sometimes complicated sequences of materials and procedures have been devised to try to meet as many demands as possible.

Table 4.1a, Table 4.1b, and Table 4.1c summarize some of the pertinent facts for a number of insulators.

Table 4.1a Properties of Inorganic Dielectrics

Material	Refractive Index	Dielectric Constant ε at 1 MHz	Dielectric Breakdown (MV/cm)
SiO_2			
Bulk silica	1.46	3.85	>10
Thermal	1.46	3.9	>10
Sputtered	1.46	3.9	3–7
CVD	1.46	4.1–5[a]	8–10
PECVD	1.45–1.47	4.1–5[a]	5–10
CVD PSG	~1.45	~4	8.5–11
PECVD PSG	~1.45	4.1–4.3[b]	8.5–11
CVD BSG		3.8	
PECVD BSG		3.9	
CVD BPSG		3.8–4.5[a]	
PECVD BPSG		~4	
F-doped	<1.46[c]	<4.1[c]	6–8[d]; <3[e]
Nitride			
CVD (Si_3N_4)	2.01	~7	10
PECVD(SiN_xH_y)	~2[f]	6–9	5
Al_2O_3	1.6–1.7	7–9	1–3
BN		2.7–7.7	
SiBN	2–1.7[g]	6.8–2.9[g]	Not sharp BD
SiBNO	~1.8–1.55[h]	Minimum: 3.3[h]	Not sharp BD

[a] Depends on deposition conditions.
[b] Depends on P-content.
[c] Depends on F-content.
[d] Fukada and Akahori (1993).
[e] Fukada and Akahori (1995)
[f] Depends on H-content and Si/N ratio.
[g] Depends on B-content.
[h] Depends on [Si] and [O]/[Si].

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Table 4.1b Properties of Selected Inorganic Insulators

Material	Stress[a,b] (MPa)	Thermal Stability	Etchability, wet/plasma
Sputtered SiO_2	C[c]	Stable[d]	BHF[e]/F-containing
CVD SiO2	T	Loses H_2O, OH; densifies	BHF[f]/F-containing
PECVD SiO2	T or C[g]	Loses H_2O, OH; densifies	BHF[f]/F-containing
F-doped SiO_2	C or T[h]	Loses HF	BHF/F-containing
Si_3N_4 (CVD)	High T	Stable[i]	H_3PO_4/F-containing
SiN_xH_y (PECVD)	C or T[b]	Loses H; densifies; stress → C	BHF[j]/F-containing

[a] C = compressive; T = tensile (+).
[b] Value usually depends on deposition conditions.
[c] Value depends on [Ar].
[d] May lose Ar at very high temperature.
[e] Etch rate close to that of thermal oxide.
[f] Etch rate depends largely on density, and [OH].
[g] Sign as well as value depends on deposition conditions.
[h] C stress decreases with [F]; may become T.
[i] May lose H at very high temperature.
[j] Rate depends largely on [H].

Table 4.1c Properties of Selected Inorganic Insulators

Material	Barrier to Na^+	Barrier to H_2O	Use
Thermal SiO_2	No	No	Passivate Si
Deposited SiO_2	No	No	Interlevel dielectric
PSG	Yes	Yes	Interlevel dielectric
Si_3N_4 (CVD)	Yes	Yes	Overstructures formed in Si
SiN_xH_y (PECVD)	Yes	Yes	Interlevel dielectric; final passivation

4.2 INORGANIC DIELECTRIC FILMS

4.2.1 SiO_2: Introduction

Deposited amorphous silica is used most often as the interlevel dielectric in multilevel devices, and deposition of SiO_2 will be used to illustrate the apparatus and processes used for depositing many of the inorganic dielectric films. The deposition methods used most widely are discussed in Chapter 1. The properties of SiO_2 films will be examined in greater detail than will those of other materials, with attention given to the relationship between the characteristics of the deposition system and the film properties. Some of the techniques to be discussed are rarely used now in manufacturing, but are included for historical perspective and, at times, to indicate the origins of current practices. Other deposition techniques, the use of which has never been widespread and thus are not described in Chapter 1, are reviewed briefly together with film properties. This has been done to illustrate new ideas; perhaps future development may make them feasible for manufacturing.

Silicon can be oxidized at high temperatures; the film is often referred to as thermal oxide. It is used to passivate the silicon substrate after the active and passive devices within it are completed and as the gate in MOS devices. Although it not used in the interconnections, it is mentioned here because its properties are often used as a standard to which the properties of deposited oxides are compared.

The deposited film may be simply SiO_2 (i.e., undoped, sometimes called USG, undoped silicate glass, to distinguish it from a doped oxide, e.g., BSG, borosilicate glass) or the film may have other

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constituents added intentionally to modify the material properties (dopants such as B, P, As, Ge, and F), incorporated as a result of the deposition method or conditions (e.g., H, Ar), or unintentionally during exposure to various environments (e.g., Na^+, H_2O). These subjects are discussed in a later section.

The usefulness of SiO_2 films for this purpose depends on their physical and chemical properties. When prepared properly, the films meet the requirement given above for an interlevel insulator.

However, the properties may deviate from ideality depending on the actual stoichiometry, the internal structure, i.e., the bonding, and the presence of other constituents, which depend on the method of deposition, the deposition conditions, and the environments to which the films are exposed.

An SiO_2 film that has all the attributes of a properly prepared film (described above) needed for a given application is a good-quality film. Nonideal films are of poorer quality. However, depending on the application, nonideality may be acceptable. For example, films with low tensile stress can be used when their thickness is not too great. When device speed is not a requirement, a higher dielectric constant film can be used. The breakdown strength for interlevel dielectrics need not be very high, as discussed above. However, porosity is never desirable, so that often the term poor quality often refers to films that are porous. Nonstoichiometric films that are electrically leaky are poor-quality films.

The films are characterized, as are all dielectric films, by measuring optical constants such as refractive index and dispersion, physical properties such as stress and porosity, electrical characteristics such as dielectric constant, leakage, and breakdown strength, and chemical properties such as composition, bonding, and etch rates in various etchants. Characterization techniques are described in Chapter 2. It must be re-emphasized that no single technique is adequate for film characterization, although a single property can be used to monitor the reproducibility of a deposition process.

The properties of SiO_2 films depend on the deposition method and the choice of deposition conditions; those deposited by many of the common techniques are reviewed in the following section.

4.2.2 Physical Vapor Deposition

4.2.2.1 RF Sputtered SiO_2

The basic principles of sputtering and a description of sputtering systems are covered in Chapter 1.

RF sputter deposition of SiO_2, despite the superior quality of the films, has never been used widely in device manufacturing because of its high cost. Although the quality of the films produced by the alternative, cheaper processes was (in earlier times) not as good, it was adequate for many of the devices being made. Now even the previous users of sputtered SiO_2 have largely abandoned it for cheaper (faster) processes, which now can compete in quality. Nevertheless work on sputtered oxide has continued to some extent. Many of the lessons learned in developing sputtered SiO_2 have been applied to improving and expanding the usefulness of plasma-enhanced chemical vapor deposition (PECVD) processes. Perhaps the most important is the demonstration of the influence of substrate bias on film quality (discussed below) and on step coverage (Kennedy, 1976) and on planarization (Ting et al., 1988) covered in a later section.

SiO_2 is sputtered from a dense target of very high-purity silica. Sputtering systems are described in Chapter 1. The effects of pressure, target–substrate spacing, and temperature on deposition (net accumulation) rates are discussed in Chapter 1. The absence of chemical interactions makes it easier to design the reactors and to determine the dependencies of the rate, uniformity, and film quality on the deposition parameters.

Increasing the substrate bias, i.e., the energy of ion bombardment, improves film properties. The dielectric constant and dissipation factor are lowered, the resistivity is raised, the etch rate in

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HF-based solutions is reduced, the pinhole density is decreased, and the step coverage is improved (Logan et al., 1970; Maissel et al., 1970; Vossen, 1971; Stephens et al., 1976). The effect on breakdown voltage is not conclusive since both improvement and deterioration (Schreiber and Froschle, 1976) have been reported. The improvement has been shown to be a result of an increase in the re-emission coefficient R (Jones et al., 1967; Maissel et al., 1970). R is the fraction of the material reaching the substrate which is re-emitted due to ion (and possibly neutral) bombardment and to elevated surface temperature (which may result from the increased ion bombardment or external heat sources). R increases as the pressure and input power are decreased and as the substrate bias and temperature are increased. R is related to the binding energies of the deposited species to the surface. Species trapped in nonoptimal sites are more easily removed, leaving behind the more tightly bound species which constitute a high-quality film. It was demonstrated that the re-emitted material, collected under conditions of little or no re-emission during redeposition, was a very fast-etching, porous film.

SiO_2 films sputtered under optimal conditions are very nearly stoichiometric in composition, contain negligible amounts of Si–OH and no water, have a dielectric constant minimally higher than bulk silica, are dense, and are good moisture barriers. The films have a low compressive stress. The Ar content and its role are discussed later. Although the presence of O_2 or H_2 in the sputtering gas reduces the deposition rate, benefits of using mixtures of Ar and these gases have been found. Suyama et al. (1987, 1988) reported that although the films were deposited at a low temperature (200°C), they were smoother and had improved electrical characteristics when compared with films deposited in Ar alone. Macchioni (1990) attributed the improvements to decreased deposition rates. Hydrogen addition (in a magnetron system, at a substrate temperature of 200°C) prevented formation of the microvoids seen in films sputtered in Ar alone; the film density was slightly higher than that of thermal oxide. From IR and AES measurements, it was concluded that the film structure was not changed by adding H_2 (Serikawa and Yachi, 1984). Apparently there was no (or insignificant) incorporation of H into the film. Previously, Serikawa (1980) had found that H_2 addition enhanced the step coverage of SiO_2 films.

A serious disadvantage of sputtering for SiO_2 deposition is its low rate which translates to low throughput, despite the use of batch systems, and thus higher cost. Several proposals have been advanced for improvement. One is the use of magnetrons (Homma and Tunekawa, 1988). Another is to increase, substantially, the power delivered to the target (Macchioni, 1990). Logan et al. (1990) developed a high-rate, low-voltage, single-wafer reactor. The low-voltage operation was achieved by using in-phase target and substrate sheath voltages, 40.68 MHz excitation, and a controlled-area confining wall electrode. Wafer temperature was controlled by gas conduction cooling to < 400°C. Rates as high as 1750 Å/min were attained under planarizing conditions. A major disadvantage was particulate generation; the size and density of particles were too high for VLSI (and ULSI) applications.

Particulate generation is a problem in all reactors. Poor-quality oxide is deposited on the chamber walls and fixturing; this material can flake and become incorporated into the film during deposition. It can become detached when the reactor is cooled and opened to the atmosphere and rain onto the wafers. The use of load locks has been tried but is difficult to implement in batch systems. Plasma cleaning has been suggested, but it is not clear that it has been tried; erosion of the target would be a drawback. The usual procedure, which adds to the cost (down-time), is chamber cleaning.

Most sputtering systems are operated at 13.56 MHz, but using a higher frequency has a particular advantage in SiO_2 deposition: damage to FET devices is reduced. Since the damage is probably caused by x-rays generated in the gate by secondary electrons produced at the target (Grosewald et al., 1971), lowering their energy by using the higher frequency reduces the damage (Logan et al., 1977). Another method for damage reduction is insertion of a DC-biased grid between the target and substrate electrodes to absorb the secondary electrons emitted by the target (Hazuki and Moriya, 1987).

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Meaudre and Meaudre (1981) studied DC current transport and Meaudre and Meaudre (1984) elucidated the mechanisms for AC conduction in RF sputtered SiO_2.

4.2.2.2 Reactive Sputtering

Reactive sputtering of SiO_2 has been investigated to some extent, but the availability of dense targets to be used in RF sputtering has reduced interest in this method of film deposition. Fuller and Baird (1963) used DC reactive sputtering of a Si target in an O_2 ambient to form adhering, continuous films of SiO_2 at low rates. The measured porosity accounted for the low dielectric constant and high etch rate of the films. Valetta et al. (1966) reported that unless the films were prepared at rates <200 to 300 Å/min and at temperatures >400 to 500°C, the films were soft, porous, and had poor adhesion. Many of the more recent studies have been part of a series investigating several other oxides for which reactive sputtering may be more appropriate (e.g., Barbee et al., 1984). A "biplanar magnetron" has been used for reactive sputtering at high rates (Rostworowski and Parsons, 1985).

4.2.2.3 Dual Ion Beam Sputtering

In this technique, a high-purity quartz target was bombarded with an O^+/O_2^+ and Ar^+ beam. The Ar was introduced through a hollow cathode and O_2 was injected into the source chamber (Emiliani and Scaglione, 1985) .The deposition rate was maintained at ~60 Å/min. The SiO_2 films had the correct stoichiometry, high density, and good mechanical properties. The H-content of the film was ~10% (measured by elastic recoil detection) and the SiOH in the IR spectrum correspondingly high. The films were O-rich (Si:O = 0.45) (Emiliani and Scaglione, 1987).

4.2.2.4 Deposition by Etching-Enhanced Reactive Sputtering (DEERS)

In this technique, Si targets were sputtered in a planar magnetron system in an O_2/CCl_4 atmosphere in an RF magnetron reactor. The rate rose slowly with small additions of CCl_4, then increased rapidly; at a concentration of 2 at% Cl, the rate reached its maximum value of about 30 times the rate with no CCl_4. The mechanism proposed was the formation of a high vapor pressure species at the target; these are sputtered into the plasma, fragment, and impinge on the substrate to react with O-bearing species to form the oxide (Ross, 1990). At high concentrations of etch gas, the optical and scratch properties of the film deteriorated. When the gases contained both Cl and F (e.g., CCl_3F) the films contained several at% of Cl and F ($Cl < F$) but these species were not bonded to Si (Nandra, 1990).

4.2.3 Chemical Vapor Deposition (CVD) of SiO_2

The principles of CVD processing and the apparatus used are covered in Chapter 1.

4.2.3.1 Inorganic Precursors

The most widely used inorganic precursor is SiH_4 but higher hydrides, Si halides, such as $SiCl_4$, or mixed hydride/halides have also been tried. The oxidizing agent is usually N_2O or O_2; CO_2 (Steinmeiner and Bloem, 1964), NO (Rand, 1967), O_3 (Maeda and Sato, 1977), and, most recently, H_2O_2 (see below) have been used. For application as an interlevel insulator with Al-based metallization, relatively low (400 to 450°C) deposition temperatures are required. The deposition rate decreases as the temperature is decreased and films deposited at low temperature are often porous with significant H content (OH and possibly H_2O) and have a high tensile stress. Another very

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serious disadvantage to the use of the inorganic precursors is that the deposited films have poor step coverage/gap fill characteristics. Takahashi et al. (1995) obtained improved step coverage by an oxide deposited using SiH_4 and O_2 at 15 torr, but only at elevated temperatures (≥600°C), which reduced the sticking coefficient of the growth species. Gas-phase reactions producing particles (snow, dust) which result in hazy films with high defect density and poor dielectric properties are another drawback. Addition of C_2H_4 to SiH_4/O_2 suppressed gas-phase particle formation but lowered the deposition rate.

A recent process, called Flowfill™, introduced the use of H_2O_2 with SiH_4 and N_2 at 500 mtorr; the oxide was deposited on a cooled substrate (0°C) and then annealed at 400°C in N_2 for 30 min. The resulting film planarized and filled gaps. SiH_4 and H_2O_2 were introduced separately into the chamber; the reaction rate was moderated by the presence of N_2. The mechanism of gap filling and planarization was postulated to be the formation of $Si(OH)_4$, a very viscous liquid, which condenses into small gaps and, when the thickness increases, is pulled flat by surface tension. The condensate is converted to SiO_2 by condensation polymerization during the annealing step (Matsuura et al., 1994; Dobson et al., 1994; Kiermasz, et al., 1995). Another view of the process of gap-fill considered the role of silanol (Si–OH), which has a high surface mobility (Gaillard et al., 1996). The CVD film was encased in SiH_4/N_2O-based PECVD oxides; they were compressive films, deposited at ~300°C, using 380 kHz. The thin lower film was needed to promote adhesion to the underlying metal and act as a moisture barrier during anneal and the thicker upper layer to protect the CVD film during the final furnace bake. The stack was called an Advanced PLanarizing interlayer dielectric (APL); it had a low tensile stress (10^9 dyne/cm^2), long-term stress stability, and only small amounts of OH were detected. The quality of the layers was said to be equivalent, both physically and electrically, to PECVD oxides.

Finally, another drawback to the use of SiH_4 is that, undiluted, it is an explosion hazard and requires safety precautions.

4.2.3.2 Organic (Organosilane) Precursors

The most commonly used precursor is TEOS, tetraethoxysilane (also referred to as tetraethylorthosilicate). Tetramethylcyclotetrasiloxane, TMCTS (Fujino et al., 1992b), tetraethylcyclotetrasiloxane, TECTS (Hochberg and O'Meara, 1989), octamethylcyclotetrasiloxane, OMCTS (Matsuura et al., 1991), diethylsilane, DES (Huo et al., 1991), hexamethyldisiloxane, HMDSO (Fujino et al., 1992a), tetrakis(dimethylamino)silane (Maruyama and Shirai, 1993), and trimethoxysilane, TMS (Suzuki et al., 1996) are among others that have been tried. These precursors are liquids; in the past this required the use of a carrier gas to transport the vapor from the chamber containing the liquid but there are now flow controllers for liquid sources. The advantage cited for the use of precursors other than TEOS is their higher vapor pressures (Galernt, 1990).

There is far less safety hazard associated with organic precursors, as there is with SiH_4. In addition, films deposited using organic precursors have much better step coverage/gap fill capabilities than do those prepared using SiH_4; this issue is discussed fully in Chapter 6.

Adams and Capio (1979), as well as Becker et al. (1987), reported deposition of conformal oxide films of excellent quality by the decomposition of TEOS, at ~700°C, in a LP CVD system, using pressures of 0.2 to 0.3 torr, but the high temperature makes the process unsuitable for almost all applications as interlevel insulators. Hochberg and O'Meara (1989) have discussed other organosilane compounds which are suitable for pyrolytic deposition of SiO_2 at lower temperatures. However, for the most part, oxidation has replaced pyrolysis. A strong oxidant is needed for low-temperature oxidation; ozone (O_3) is the oxidant of choice, although Pavelscu and Kleps (1990) studied the APCVD TEOS/O_2 system in which rates of 20 to 100 Å/min were obtained.

Maeda and Sato (1977) showed that SiO_2 could be deposited using TEOS and O_3 at temperatures as low as 200°C, although the rate was very low and the films porous.

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The pressures commonly used in TEOS/O_3 CVD processes have been <100 torr (60 torr (Spindler and Neureither, 1989; Ramkumar et al., 1992); 90 torr (Shih et al., 1992)), 600 torr (so-called subatmospheric, SACVD) (Lee et al., 1990), and 760 torr, APCVD (Nishimoto et al., 1987; Fujino et al., 1990a). Stonnington et al. (1992) reported on the use of very low pressures (10^{-1} to 10^{-3} torr). The advantages of low-pressure deposition were improved step coverage due to a longer mean free path, less particulate generation, and less background water vapor (which could be incorporated into the film), but the rates were significantly lower than those obtained at the higher pressures. There appears to be no significant difference between APCVD and SACVD, nor any advantage of one over the other. It is possible that the small reduction in pressure made adaptation of an existing reactor possible.

The advantage of the higher pressure (SACVD or APCVD) over the lower pressure (60 torr) is good step coverage/gap fill at higher deposition rates and increased density so that wet etch rates and film shrinkage upon heat treatment were reduced (Lee et al., 1992); however, there are strong surface-related effects (discussed below). Despite this drawback, most of the recent work described below has been done in this higher pressure regime.

In the APCVD processes, the deposition rate increases with increasing temperature at low temperature, but decreases with increasing temperature at higher temperatures. The transition to the high-temperature regime, which is used in preparing films for VLSI/ULSI applications (~400 to 450°C), occurs at 300°C according to Kotani et al. (1989), at ~375°C (Maeda and Sato, 1977; Nishimoto et al., 1989), and ~400°C (Nguyen et al., 1990). Fujino et al. (1990b) showed that the rate as well as the transition temperature depended on the concentration of O_3 in the reaction mixture. As the O_3 content of the reaction mixture was increased, the deposition rate increased rapidly, reached a maximum, and then decreased slowly (Fujino et al., 1990b). In the high-temperature range, the wet etch rate decreased (Kotani et al., 1989) but the tensile stress increased (Kotani et al., 1989) as the temperature was increased. Hosada et al. (1992) reported that high temperature and high O_3:TEOS ratios during film deposition lowered the moisture absorption, and, thus, they concluded increased the film density, but never to a completely acceptable level in terms of subsequent outgassing in vias. They postulated that some of the water in the films was chemically bonded at sites where TEOS oxidation was incomplete; this absorption could be inhibited by annealing the films in steam, but not in O_2 or N_2. Postdeposition exposure to an RF plasma (100 kHz) at 300°C, 0.5 torr for 5 minutes in NH_3, N_2, Ar, and O_2 reduced the moisture content considerably. The higher the temperature during treatment, the lower the moisture content (Fujino et al., 1993). Reducing the deposition rate, by changing the process conditions, produced films with lower moisture content (Chiang et al., 1992).

Whether the higher or lower pressure processes are used, the deposited films are porous and contain significant amounts of Si–OH, increasing the dielectric constant. The porosity results in moisture absorption which increases the dielectric constant still further. Desorption upon heating is responsible for via poisoning. Absorption/desorption result in stress changes during thermal cycling; the hysteresis has been studied by Ramkumar and Saxena (1992) and Ramkumar et al. (1993). Hysteresis is smaller at higher O_3:TEOS ratios (Kwok et al., 1994). Stadtmueller (1992) related the tensile stress and low density in TEOS-based oxides to the production of byproducts after decomposition of TEOS on a hot surface during film formation.

Another disadvantage of the high-pressure TEOS/O_3 CVD oxide is its sensitivity to the underlying material, which influences several properties of the film (Nishimoto et al., 1989; Fujino et al., 1990a,b, 1991a,b, 1992, 1994; Huang et al., 1993; Ong et al., 1993; Kwok et al., 1994). Since PECVD oxide films (see Section 4.2.4) have been used as underlayers in gap-fill processes using SACVD TEOS/O_3 (e.g., Kwok et al., 1994), these materials were among those examined for their surface effect. The deposition rate was lower on thermal oxide than on Si (except at very low O_3 concentrations). The wet etch rate of the film decreased with increasing O_3 concentration in the reaction mixture when deposited on Si, on SiH_4-based PECVD oxides, and on N-doped TEOS/N_2O

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PECVD oxide. The trend was reversed for films deposited on thermal oxide and on PECVD TEOS oxides. Film shrinkage increased with increasing O_3:TEOS ratio when the substrate was TEOS-based PECVD; the trend was reversed on Si substrates. The films were smooth when deposited on Si and on a SiH_4-based PECVD oxide; they were rough on TEOS-based PECVD oxides and the roughness increased when the CVD oxides were deposited using higher O_3:TEOS ratios. The process in which the highest O_3:TEOS ratio was used produced the best films (dense, low shrinkage) when the substrate was Si, but was the most surface sensitive. Stress hysteresis was greater when the base was TEOS-based PECVD oxide than when it was Si or SiH_4-based PECVD oxide.

Ramping down the RF power at the conclusion of the PECVD TEOS-based oxide deposition minimized the surface sensitivity of the SACVD oxide (Huang et al., 1993). *In situ* exposure of thermal oxide and the TEOS-based PECVD oxide to Ar or N_2 plasmas eliminated the substrate dependence (Fujino et al, 1992; Kwok et al., 1994). Deposition was also a function of the density of the underlying pattern. Although the dimensions of the features may be identical, the thickness of deposit was greater in an area with a less dense pattern. Coating the underlying metal with a TEOS/O_2 PECVD oxide eliminated the difference (Ahlburn et al., 1991); the PECVD oxide also acted as a moisture barrier between the CVD oxide and the metal film. The surface sensitivity was also eliminated by using P-doped CVD oxide (Ong, 1993). Another process, called pressure ramp-up (PRU), took advantage of the surface insensitivity of oxide deposited at 60 torr and the gap-fill properties of films deposited at higher pressures. The initial film was deposited at 60 torr and then the pressure increased to 450 torr for the remainder of the process (Tu et al., 1996).

Fujino et al. (1990, 1991) attributed surface sensitivity to the difficulty of a reaction between hydrophobic TEOS and a hydrophilic surface of SiO_2 as opposed to the ease of reaction with the hydrophobic Si surface. Kwok et al (1994) refuted this model. Surface analysis showed the presence of F on substrates having surface dependence, but there was no indication of the source. On one surface (PECVD oxide after N_2 plasma treatment) both F and N were detected, and it was postulated that N counteracted the effect of F. The model proposed that the gas mixture containing the film precursors is electronegative due to abundance of O atoms and there is repulsion between the electronegative F-coated surface and the precursors, leading to a lower rate and poorer quality film. Electropositive surfaces (e.g., N-, H-coated) attract the precursors and a better quality film is formed. This model explains the efficacy of N_2 and Ar plasma treatments; N on the surface overcomes the effects of F (as stated above) and Ar sputters off the F.

Thick tensile films tend to crack so that the tensile stress in the CVD oxide limits its useful thickness. Where thick films are required, thin layers of the CVD oxide are used in combination with compressive PECVD oxide films to reduce the total stress and thus increase the cracking resistance of a thick film. The porosity requires *in situ* deposition of a PECVD oxide capping layer oxide or *in situ* plasma modification. The surface sensitivity dictates modification of the underlying layer or a change in its nature or deposition process. Thus the films deposited using TEOS and O_3 are almost always combined with other films.

A semiselective CVD process using TEOS and O_3 was developed by Homma et al. (1993). It involves capping Al interconnects with TiN or TiW and exposing the surfaces of the metal and the PECVD oxide between the metal stripes to a CF_4 plasma. The thickness of oxide then deposited on the metal was substantially thinner than that deposited in the spaces.

The primary advantage of using TEOS (or other organosilanes) over the inorganic precursors is the improved step coverage. The profiles are rounded and are characterized as having a flow-like appearance. The mechanisms explaining the step coverage are discussed in the chapter on integration. Nguyen et al. (1990) and Fujino et al. (1990b) discussed the reaction mechanism. They both noted that there were two temperature regimes: (1) the lower temperature one, in which the reaction was thermally controlled (increasing rate with increasing temperature) and (2) the higher temperature one described by Nguyen et al. as a "surface diffusion reaction" region and by Fujino et al. as one in which the high temperature results in fewer adsorbed reactants. At the higher temperature,

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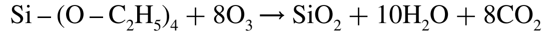
the higher decomposition rate of O_3 and its loss at the walls may also be a factor. The overall reaction, when the reactants are heated, is



$$Si-(O-C_2H_5)_4 + 8O_3 \rightarrow SiO_2 + 10H_2O + 8CO_2$$

although the intermediate reactions and the precursors in the gas phase and on the surface are not known. Fujino et al. depict the reaction as a chain of reactions in which the Si-containing moiety (the oligomer) is adsorbed in the surface while C_2H_4 and H_2O are desorbed, resulting finally in the deposition of SiO_2 and elimination of the C- and H-containing species They note that the flow-like behavior of the TEOS/O_3 film has been assumed to result from a liquid-like behavior of the oligomers. None of the incompletely reacted TEOS fragments are incorporated into the film; they are probably oxidized to Si–O and Si–OH before incorporation. Ozone may participate in the reaction or act as a catalyst. The higher temperature, although lowering the rate, enhances H and Si–OH elimination and film densification.

4.2.4 Plasma-Enhanced Chemical Vapor Deposition of SiO_2

The principles of reactive plasma-assisted processing and a description of the reactors used are covered in Chapter 1.

PECVD and CVD processes use the same Si-containing precursors, principally SiH_4 and TEOS, although halides such as $SiCl_4$ and SiF_4 (Falcony et al., 1991) and the organic compound TMCTS (Webb et al., 1989) have also been tried. In TEOS-based PECVD deposition, in which the plasma creates reactive species, O_2 can replace the more highly reactive O_3 needed for thermally activated deposition. Except in the high-density reactors, discussed below, N_2O is often the oxidant when SiH_4 is the precursor. Although lower deposition temperatures are possible in PECVD, since a discharge supplies the energy, produces reactive species and ions to bombard the surface, thereby densifying the film as well as enhancing the surface reactions, it will be seen that higher deposition temperatures result in good quality films.

SiH_4- and TEOS-based films will be considered separately, wherever possible, in the following discussion. The advantages of using organic precursors instead of SiH_4 are the same for PECVD as for CVD.

4.2.4.1 Capacitively Coupled Plasmas; Bell Jar Reactors

Some of the earliest work was done in bell jar systems. TEOS was decomposed in an RF oxygen discharge by Alt et al. (1963) who reported that the films were dense. Ing and Davern (1965) found that films deposited at high rates had occluded organic material, were less stable electrically, and had higher dielectric losses. Mukherjee and Evans (1972) noted the presence of OH groups in films deposited below 500°C. Secrist and Mackenzie (1966) used microwave excitation to produce films structurally similar to silica but containing extensive amounts of water.

SiH_4 and N_2O were used by Sterling and Swann (1965) who found that, although films can be formed at low temperature, they contained a large amount of water. Higher deposition temperatures were preferable; the films thus formed were hard, glassy, and adherent. Joyce et al. (1967/68) also used SiH_4 and N_2O and concluded that the film properties depended on the SiH_4/N_2O ratio and the deposition temperature.

As Sterling and Swann (1965) pointed out, N_2O is preferred over O_2 because of the spontaneous reaction between SiH_4 and O_2, so that, as pointed out by Hess (1987), using O_2 increases the possibility of a homogeneous reaction instead of the desired heterogeneous surface reaction. Gokan et al. (1987) mentioned the low dissociation energy of the N–O bond in N_2O as another advantage of the use of that oxidant. Nevertheless O_2 was used with SiH_4 to prepare a range of SiO_x compounds; no mention was made of any homogeneous reactions (Pan et al., 1985).

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4.2.4.2 Capacitively Coupled Planar Reactors

The capacitively coupled planar reactor, patented in 1973 by Reinberg, displaced the tubular or bell-jar systems. This reactor or modifications of it were used for batch processing until they were, in turn, largely displaced by single-wafer or multiple-station reactors.

4.2.4.2.1 SiH_4-Based Oxides

SiH_4 and N_2O, and an excitation frequency of 50 kHz, were used by Hollahan (1979). He reported the films were compressive, contained some N, and that step coverage of a shallow V-groove by a thin film was conformal. Adams et al. (1981) also used SiH_4/N_2O mixtures in a similar reactor, but 13.56 MHz excitation of the plasma. The deposition temperature was 200 to 340°C and the pressure 133 Pa. They reported that films deposited over deep straight-sided steps were thin along the vertical walls and contained no N. They emphasized the strong dependence of the film properties on the deposition conditions. They summarized their findings: with increasing deposition temperature, the growth rate and film density increased and the wet etch rate and H-content decreased and the film stress was compressive under all deposition conditions.

Gokan et al. (1987) found that the compressive stress decreased as the pressure was increased and the temperature decreased. The opposite trend was reported by van de Ven et al. (1987) who used a multiple-station reactor with a much higher deposition rate and temperature (400°C); below ~250 Pa the film stress was tensile (~5×10^8 dyne/cm^2) and changed sign at ~250 Pa. The maximum value of the compressive stress was ~1.5×10^9 dyne/cm^2.

Batey and Tierney (1986) reported that excellent film properties were obtained by lowering the SiH_4 and N_2O concentrations with a very large flow of helium to reduce the deposition rate. Chapple-Sokol et al. (1991) also used this highly diluted reaction mixture and found that the deposition rate decreased as the temperature was increased. They postulated that this might be due to reduced reactant residence time at the higher temperatures. At 250°C, H_2O and Si–H were detected in the IR spectrum; as the temperature was increased, the H-concentration (Si–OH only) decreased. The rate increased with increasing input power, reached a maximum, and then decreased but the power had little influence on the H-content of the film. The film properties (porosity, density) improved with increasing temperature and power, although temperature has the greater influence in decreasing the Si–OH content. The power played a significant role in incorporation of adsorbed precursors to low-energy sites within the growing film.

4.2.4.2.2 TEOS-Based Oxides

Kirov et al. (1978) deposited SiO_2 from TEOS and O_2, using a 13.56 MHz discharge. At temperatures below 400°C the films contained absorbed water. Veprek and Boutard (1991), using a 27 MHz discharge, found that good-quality TEOS-based oxides could be prepared at relatively low temperatures if the deposition rates were kept low. The results reported by Hey et al. (1990), for TEOS-based oxides, agreed with those of Gokan et al. (1987), i.e., the stress went from compressive to tensile when films were deposited at pressures of ~170 Pa. Also, the wet etch rate increased monotonically with increasing pressure. They attributed both results to reduced ion bombardment at higher pressure and concluded that the high-frequency power had little effect on improving the film properties. The use of TEOS, for deposition of SiO_2 with improved step coverage properties, in a high-pressure, single-wafer reactor was described in a patent filed in 1991 (Wang et al., 1994). Patrick et al. (1992) showed that the deposition rate and H-content of TEOS-based oxides decreased with increasing temperature; decreasing the TEOS/O_2 ratio also decreased the rate. The rate was independent of power but the stress increased as the power was increased. The dielectric constant increased as the deposition rate increased. Films deposited at a low temperature absorbed moisture at a rapid rate.

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Based on the experience gained from sputtering, i.e., higher energy ion bombardment of the substrate (by the use of applied substrate bias) improved the quality of the deposited films, modifying reactors for dual frequency operation was a logical step. Both van de Ven (1990) and Hey (1990) showed that increasing the fraction of low-frequency power made the film stress of a TEOS-based oxide less tensile (more compressive) and lowered the wet etch rate, i.e., the film was denser; therefore it absorbed less atmospheric moisture. These effects illustrated, again, the beneficial effect of higher energy bombardment.

4.2.4.2.3 Moisture Absorption

Because of the adverse effects of moisture in the films (e.g., increased ε) effort has been expended on finding ways of ensuring moisture resistance. Harrus et al. (1991) reported that the use of low frequency during deposition, i.e., by employing a dual frequency reactor, improved the moisture resistance of both TEOS- and SiH_4-based oxides. Later results by the same group (van Schravendijk et al., 1992a,b) were that a TEOS-based oxide with a compressive stress $\geq 10^9$ dyne/cm^2 and a refractive index ≥ 1.458 would not absorb water regardless of the deposition conditions, although they also stated that the use of low-frequency power was necessary to produce compressive stress. They used the stress hysteresis (the difference between the film stress as-deposited and at the end of a complete thermal cycle) to demonstrate the influence of stress and refractive index on moisture absorption, as shown in Figure 4.1 and Figure 4.2. In the absence of moisture, there is no hysteresis. By using the flexibility of a dual-frequency plasma, they were able to deposit a film of low compressive stress at 250°C, equivalent to a film deposited at 350°C.

Robles et al. (1992) and Galiano et al. (1992) deposited TEOS-based oxides with a compressive stress of 10^9 dyne/cm^2 that did not absorb moisture. There was a negligible influence of deposition rate or the use of a mixed frequency. The higher the deposition temperature, the better the moisture resistance. Thus they concluded that the moisture resistance of TEOS-based oxides was determined by the initial stress and the deposition temperature only.

For SiH_4-based oxides, films with a refractive index ≥ 1.465 do not absorb moisture but such films have a lower compressive stress (van Schravendijk et al, 1992). Incorporation of N or excess Si was required to make low-stress films moisture resistant. Blain et al. (1995) agreed with these results, i.e., that a high compressive stress does not guarantee a dry, stable film. Very low moisture absorption is related to a high refractive index and a low as-deposited compressive stress. A Si-rich

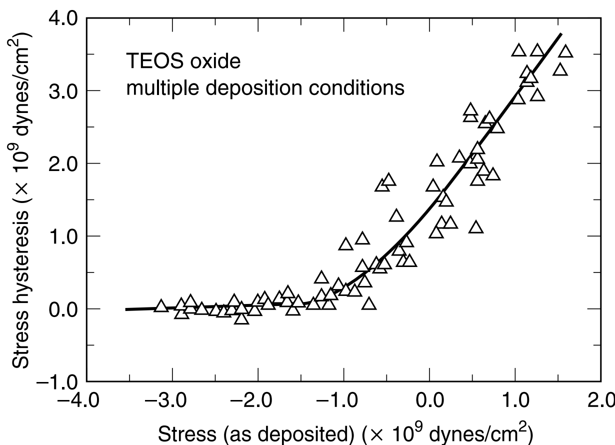

Figure 4.1 Stress hysteresis of TEOS-based PECVD SiO_2 films vs. as-deposited stress. (Reprinted from van Schravendijk, A.S. Harrus, G. Delgado, B. Sparks, and C. Roberts, VMIC, 1992, p. 372. With permission.)

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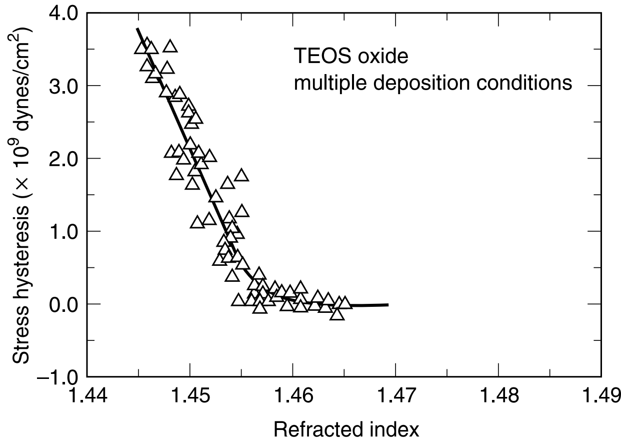

Figure 4.2 Stress hysteresis of TEOS-based PECVD SiO_2 films vs. refractive index. (Reprinted from van Schravendijk, A.S. Harrus, G. Delgado, B. Sparks, and C. Roberts, VMIC, 1992, p. 372. With permission.)

oxide, which met the refractive index and stress criteria, did, indeed, have superior moisture resistance. It was stated that moisture absorption is controlled by composition, mechanical stress, and density.

Since TEOS- and SiH_4-based oxides behave differently with respect to moisture absorption, it was postulated that there must be a significant difference in their molecular structure (van Schravendijk et al., 1992).

4.2.4.2.4 Step Coverage

As stated before, the step coverage capabilities of PECVD oxides increase when TEOS is used instead of SiH_4 as the Si- containing precursor, but those of the CVD TEOS/O_3 film are even better; this is discussed in detail in another chapter.

In an effort to improve step coverage, a process called TOP-PECVD, which used a pulsed RF plasma, was introduced by Ikeda et al. (1992). Deposition of SiO_2, using TEOS and O_3, was alternated with exposure to an O_2 plasma so that the ion bombardment could dehydrate the film. This cyclical procedure resulted in a thick homogeneous film, more conformal than conventional TEOS/O_2 PECVD oxides but denser than CVD films.

4.2.4.3 Deposition Models

4.2.4.3.1 TEOS-Based Oxide

The explanation of the decrease in deposition rate with increasing temperatures (negative activation energy) has been explained in terms of adsorption/desorption; at higher temperatures the chance for adsorption decreases while that for desorption increases (e.g., Chin and van de Ven, 1988). This model has been discarded by Raupp et al. (1992). They viewed the deposition process as following two paths: O ion-assisted and O atom-initiated. The rate of the ion-assisted reaction is proportional to the O ion flux with a reactive sticking coefficient close to 1. The rate of the O atom-initiated reaction is nearly independent of temperature and TEOS concentration but is directly proportional to the O-atom concentration. They stated that the evidence favored a model in which the growing film is saturated with TEOS precursors and oxidative attack by O atoms and ions was the rate-determining step, not precursor adsorption. Thus, they explained that the (apparent) negative

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activation energy was due to an activated atomic-O surface recombination which decreases the O-atom concentration as the temperature is increased.

4.2.4.3.2 SiH_4-Based Oxide

Smith and Alimonda (1993) studied the chemical reactions which occur in the plasma deposition of SiO_2 in undiluted and He-diluted SiH_4/N_2O mixtures; they analyzed the plasma by means of a mass spectrometer connected to the reaction chamber and configured for line-of-sight sampling of the plasma species in the deposition plane. They found that if the RF power was sufficient to generate a supply of O atoms in excess of that needed to convert all the SiH_4 to SiO_2, the IR spectrum will show Si–OH peaks (a few at%) in addition to the Si–O peaks; but no detectable ($<0.5\%$) HO–H, Si–H, or N–H peaks. Oxygen consumes SiH_4 by the generation of various silanols, $SiH_n(OH)_m$. However, since O is known to react with the Si–H bond by extracting H to form OH, the silanols must be formed by subsequent reattachment of the OH. The decrease of OH with increasing temperature is evidence for the thermally driven OH elimination. The silanol precursors contribute to film formation and to particle formation (with loss of rate). The importance of silanols in film deposition relative to more direct reactions of SiH_n and O at the surface is not known, although surface reactions must dominate at low pressure when there are not enough gas collisions to form gas-phase precursors. The reaction pathways are shown in Figure 4.3. Smith and Alimonda detected no effect of the He dilution on the chemical reactions in the plasma or on the electrical properties of the film. They concluded that excess O was the key to obtaining a good oxide. They measured the quality of the oxides in terms of breakdown fields and electron trapping; these, however, are not of great importance for an interlevel dielectric.

4.2.4.4 High-Density Plasmas

Next in the development cycle were the high-density plasma systems, ECR, RFI (or ICP or TCP), and the helicon. ECR was the first to be introduced commercially. The initial interest in these kinds of systems was fueled by the widely publicized, but mistaken, idea that excellent-quality films, capable of filling high aspect ratio gaps, could be deposited at low temperatures, perhaps even at room temperature, and that the low ion energies of such a plasma minimized or eliminated damage. However, as mentioned previously, substrate bias, essential for gap filling, results in wafer heating and perhaps damage. Pai et al. (1992) discusses this in some detail. Thus, despite the cooled

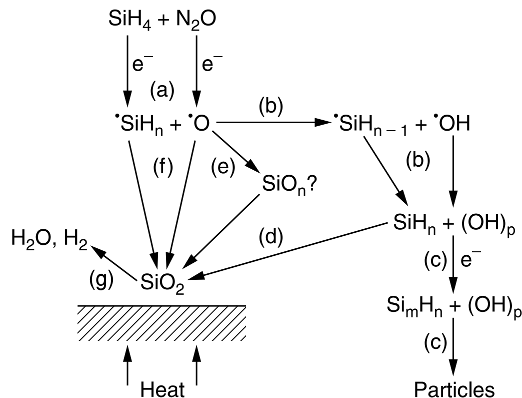

Figure 4.3 Reaction pathways for SiH_4-based PECVD SiO_2. (Reproduced from Smith, D.L. and A.S. Alimonda, *J. Electrochem. Soc.*, 140, 1496, 1993. With permission of the Electrochemical Society, Inc.)

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wafer holder, the wafer temperature was high (in some cases ~500°C), although earlier it had been reported that oxides prepared in an identical way had been deposited at low temperature. The systems developed most recently have substrate bias and He-backed chucks for temperature control.

4.2.4.4.1 ECR

SiH_4, injected into the reaction chamber, has been used as the Si source most often; TEOS is an alternate source used infrequently (Pai et al., 1992). O_2 is the usual oxidant, although N_2O has been tried (Herak and Thomson, 1990; Chau et al., 1991). O_2 is introduced into the plasma chamber, usually with Ar.

The deposition rate of the oxide increases with increasing flow of the Si source and microwave power. The deposition rate decreases with increasing temperature for both SiH_4 and TEOS as the Si source. This trend is opposite to that seen for oxide deposition in the (capacitively coupled) low-density plasma reactors using SiH_4, but the same as that observed for TEOS as the precursor. This implies that the mechanism of oxide deposition from SiH_4 must be different in the low- and high-density plasmas.

The decrease in rate with increasing temperature has often been explained as due to thermally enhanced desorption of a precursor from the surface on which the film is being grown, although it may be recalled that Raupp et al. (1992) suggested an alternative mechanism involving loss of active O to explain the negative activation energy in the low plasma density deposition of oxide from TEOS. There has been no suggestion in the literature that Raupp's explanation might also be applicable to oxide deposition from SiH_4 in an ECR reactor.

There is one exception to the decrease in rate with increasing temperature for SiH_4-based oxide deposition. Herak and Thomson (1990) used a different ECR configuration, one in which the substrates were placed in the chamber beneath the field coils, i.e., in direct contact with the plasma, or else near the SiH_4 inlet, in the plasma afterglow. They found that when the substrate was located in the afterglow, the deposition rate increased with increasing temperature, suggesting that under these circumstances there was a thermally activated surface reaction. However, when the substrates were in direct contact with the plasma, the rate decreased with increasing temperature, as has been reported for the divergent-field ECR reactors.

As the substrate bias increases, the deposition rate decreases, except, as discussed below, for very low RF power levels. By analogy to bias sputter deposition, this has been attributed to sputter etching, competing with deposition, but this interpretation seems to be open to question.

Lassig (1994) investigated low-temperature (~200°C) deposition of oxide in the regime in which very low RF power was applied to the substrate. In the range 0 to 0.6 W/cm^2, the rate increased slightly. He attributed this result to an ion-assisted deposition reaction, as had been proposed by Chang et al. (1990) and Raupp et al. (1992) for PECVD and by Chang et al. (1993) for ECR deposition. At low RF power levels there is an excess supply of neutral precursors, possibly silane or one of its radicals, so that the rate is ion-limited. As the ion energy increases, the supply of neutral precursors becomes depleted and the ion-induced rate eventually saturates. As the bias is increased further, the rate falls due to sputter etching However, Pai et al. (1992) showed that the sputter etch rate was insufficient to account for the rate reduction in the TEOS-based ECR deposition, and that the rise in temperature, due to the ion bombardment, contributed to the rate reduction which they attributed to precursor desorption.

For all values of applied bias, increasing it made the films more like thermal oxide: the wet etch rate decreased (i.e., the film density increased), and the position of the Si–O band in the IR spectrum was shifted to higher frequency and the band half-width decreased. Lassig (1994) also concluded that for a given ratio of SiH_4 to O_2, increasing the substrate bias resulted in a decrease in H-bonded SI, as applied bias increased the oxidation of silane. The compressive stress was reduced

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as the substrate bias was increased; the trend opposite to that observed for sputtered oxide films. Films deposited with substrate bias, and optimal reactant ratio, show no hysteresis upon thermal cycling (Chiang et al., 1989). The compressive stress increased with increasing deposition temperature (Chebi et al., 1992) and with increasing O_2:SiH_4 ratio (Lassig, 1994).

Denison et al. (1990) also found that the density of the oxide film decreased with increasing incorporation of Ar. Fukada et al. (1988) reported that a high-quality film, equivalent to thermal oxide, can be formed when the ECR position is located close to the substrate; they suggested that the quality is related to highly excited ions transported to the substrate. The results of Herak et al. (1989) are at odds with most of the work reported in the literature, in that they found the properties of their films, deposited at 350°C, were insensitive to the O_2:SiH_4 ratio.

The trends reported here without attribution have been noted by many investigators, some of whom have been cited when discussing other oxide properties, and some of whom have not been cited previously, e.g., Nguyen and Albaugh (1989), Andosca et al. (1992), Fukada et al. (1992), and Hemandez et al. (1994).

The influence of deposition conditions on the film composition, particularly the H-content of the films, and the influence of the H-content on film properties, as well as the step coverage and gap-fill characteristics are discussed in other sections.

4.2.4.4.2 Helicon Plasmas

The first report (Charles et al., 1993) of the use of a helicon plasma for deposition of SiO_2 from SiH_4 and O_2 emphasized the usefulness of this kind of reactor for low-pressure (2 mtorr) and low-temperature (~200°C) deposition of films comparable to those deposited by other techniques at much higher temperature.

O_2 was introduced at the top of the reaction chamber (the helicon source) and SiH_4 via a ring placed above the wafer. Since the wafer was merely loosely clamped to the substrate table kept at 20°C, its temperature was raised by exposure to the plasma to ~200°C. The same power was used for all the experiments. No substrate bias was applied. The deposition rate increased as a function of the SiH_4 flow rate for an O_2:SiH_4 flow rate ratio (R) ≥ 3 ([O]/[Si] ratio in the film ≥ 1.95). A decrease in deposition rate resulted in a decrease in refractive index, "P" etch rate, XPS linewidth of both the O 1s and Si 2p peaks, and an increase in the Si–O stretching peak frequency, approaching, but never reaching, the values for thermal oxide. The [O]/[Si] ratio in the film increased with increasing R; the film was stoichiometric when $R = 10$. At this ratio the deposition rate was very low (~25 nm/min).

Nishimoto et al. (1995) also deposited SiO_2; the reactants were SiH_4, O_2, and Ar. A 100 kHz bias could be applied to the substrate in this reactor. The pressure was varied between 8 and 16 mtorr; the substrate temperature was not given. The films had a low compressive stress, low H-content, good water-blocking properties, and wet etch rates comparable to those of thermal oxide. The deposition rate, which had a maximum value of ~100 nm/min, increased with increasing SiH_4 and O_2 flow rates, indicating a diffusion-limited reaction. The rate was also increased by increasing the flow of Ar and decreasing the distance between the SiH_4 source ring and the wafer; it was decreased with increasing substrate bias, attributed to sputter etching. The film composition and chemical structure were determined by the value of the O_2/SiH_4 flow rate ratio (R); at $R = 1$, the refractive index and the wet etch rate were comparable to those of thermal oxide as was the position of the Si–O peak. It was concluded that film oxidation and densification were a result of the high-density oxygen plasma produced by the helicon source. It is not clear why the value of R at which thermal oxide-like properties were reached was so different in these two investigations. The only apparent difference in the reactors was the ability to apply substrate bias in the later experiments, but there was no mention of any interaction of bias and R in that paper. The H-content could be reduced

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by increasing the substrate bias and by increased helicon source power. It was suggested that Ar sputtering increased the film density. Films with low compressive stress were obtained at high helicon power and/or substrate bias and no stress hysteresis (i.e., moisture absorption) was observed; films containing a small amount of Si–H were also stable with respect to moisture absorption.

Thus it appears that good films were deposited in a helicon reactor, but comparable films have been deposited in lower density plasma reactors. The advantage appears to be not in the quality of the films (unless it is confirmed that these good films were deposited at a significantly lower substrate temperature) or in the deposition rate, but in the ability to fill high aspect ratio gaps (as discussed in another chapter).

4.2.4.4.3 Inductively Coupled Plasmas

SiO_2 films were deposited using $SiH_4/O_2/Ar$ in a biased inductively coupled plasma (ICP) reactor. The wafers were placed on an electrostatically clamped holder with He backside flow for temperature control; the deposition temperature varied between 250 and 350°C. The pressure in the reactor was < 5 mtorr. The rates were higher than in the helicon system (180 to 400 nm/min) but the source power was also higher. Since power density and efficiency were not given, it is difficult to compare the achievable rates in these two kinds of HD reactors.

The deposition rate of the oxide increased with increasing SiH_4 flow and source power, suggesting a species (plasma-activated SiH_4) transport-limited process. The sputter etch rate, necessary for gap fill, increased with increasing substrate bias (Mountsier et al., 1994).

Films deposited using a high O_2/SiH_4 flow rate ratio (~2) did not absorb water and contained only a small concentration of Si–OH; the H-concentration varied between 1.4 to 4 at%, depending on the deposition conditions. The films had a low compressive stress. The Si–O stretching frequency and band width of these films were similar to those of high-temperature LPCVD oxides. Increasing substrate bias and temperature densified the films and reduced the H-content. Films deposited in an O_2-rich region are stoichiometric and have a refractive index of 1.46 and a wet etch rate almost two times greater than that of thermal oxide (Nguyen et al., 1995).

SiO_2 films, deposited in the absence of bias and thus at the lowest temperature, have a lower Si–OH content and less tendency to absorb atmospheric moisture, and were smoother compared with films deposited with bias (Shoda et al., 1996). As the RF bias was increased, the concentration of Si–OH increased monotonically, reaching its maximum value at ~500 W. As the bias was increased further, the Si–OH content decreased slowly, as shown in Figure 4.4 (Weigand et al., 1996).

For biased deposition, the Si–OH concentration decreased monotonically with substrate temperature, opposing the effect of substrate bias. The explanation offered was that thermal energy annealed sputter induced defects responsible for Si-OH incorporation in the growing film (Weigand et al., 1996).

The most noteworthy capability of the biased ICP system is its high aspect ratio gap filling (Moutsier et al., 1994; Nguyen, et al., 1995), as discussed in another chapter.

4.2.5 Other Deposition Methods

4.2.5.1 Evaporation

This has never been used to any significant extent for deposition of interlevel insulators. Stoichiometry control is difficult. For example, in a good vacuum, SiO is deposited from an SiO_2 source; when SiO_2 is deposited (by changing the conditions), it is a poor-quality film (Pliskin and Lehman, 1965; Pliskin and Castrucci, 1968).

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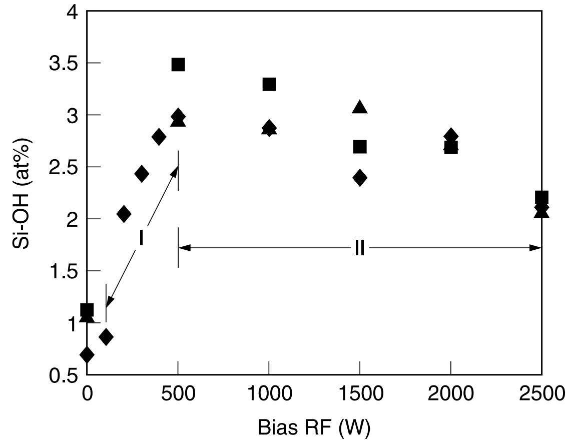

Figure 4.4 SiOH content of SiO_2 films deposited in an inductively coupled plasma reactor vs. bias applied to the substrate. (Reproduced from Weigand, P., N. Shoda, T. Matsuda, S.V. Nguyen, T.E. Jones, M.J. Shapiro, R. Ploessl, and J. Rzucek, VMIC, 1996, p. 71. With permission.)

4.2.5.2 Plasma-Enhanced Evaporation or Activated Reactive Evaporation (ARE) of Thin Oxides

The basic process is evaporation of Si (using an e-gun or a resistance-heated source) in the presence of activated oxygen. Bunash (1981) produced a plasma above the source using a DC-biased electrode placed between the source and the substrate. Low-frequency plasma excitation of O_2, magnetically confined in a separate chamber, is introduced into the high-vacuum reaction region. The low temperature of the substrate (30 to 250°C) and the ability to form SiO_2 patterns by lift-off were emphasized (Chang et al., 1983). Microwave excitation of O_2 was used by Murakami et al. (1985). Another version of this method was described by Lorenz et al. (1991). Silicon was evaporated using an e-gun as O_2 was fed directly into the chamber and activated in an Ar plasma created by a heated filament in a separate cavity connected to the chamber through an orifice. Substrate temperatures were 100 to 400°C and the deposition rate 120 Å/min. The film was stoichiometric, with < 1 at% H (from the residual gas); the electrical properties were comparable to those of thermal oxide. The emphasis was on suitability as a gate dielectric, although the application of SiO_2 as an interlevel dielectric was mentioned.

4.2.5.3 Ion Beam Deposition

Minowa et al. (1983) deposited SiO_2 using a reactive ionized cluster beam (RICB); the source was SiO_2 and an adequate supply of O_2 was injected into the chamber. The substrate temperature was < 300°C and the film quality was almost as good as that of thermal oxide; the step coverage was uniform but the deposition rate was 60 Å/min in what appears to be a single-wafer reactor.

Wong et al. (1985) used what appears to be the same method but they called it nozzle beam deposition, since they say that there was no proof that clusters of oxide were present. Film quality depended on the ionization current and acceleration voltage applied to the beam.

Minowa and Ito (1988) deposited SiO_2 using dual ion beams: an ionized cluster beam (ICB) with an SiO source together with an ionized gas beam (IGB) with an O_2 source. The beams collide in transit or on the substrate surface held at or below 200°C. The properties of the film depended on the partial pressure of O_2, the oxygen ion current density, and the deposition rate. With an

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adequate supply of O_2 (since the deposition rate depends on the O_2 ion current) deposition rates as high as 2600 Å/min can be reached. SiO_2 of a quality almost as good as that of thermal oxide was deposited at a substrate temperature ~200°C and a rate <1200 Å/min in a single-wafer system for a 5-inch wafer.

4.2.5.4 Digital CVD

SiO_2 formation by this method is accomplished by repetitive cycles of (1) deposition of a few monolayers of SiH_x and (2) oxidation. Both SiH_x (from He-diluted SiH_4) and oxygen radicals are generated from remote microwave plasma discharges and these were alternately irradiated onto a Si wafer. The species are ejected with near-supersonic velocity into a vacuum chamber and fill deep trenches in Si conformally (Nikano et al., 1989, 1890; Sakaue et al., 1993). The oxide grows a little faster on the bottom than on the sidewalls of the trench; it was postulated that the radicals are reflected from the sidewall. The SiOH content decreased with increasing O_2 irradiation; therefore the pulse width of the O_2 was larger (100 times) than that of the SiH_x. The deposition rate decreased with increasing temperature but the film quality was improved, i.e., the SiOH content was decreased. The deposition rate was 3 Å per 5.05 sec pulse at 300°C; the area was ~1 cm^2. There was no discussion of the possibility of scale-up. Although an interesting concept, the process has no foreseeable application for ULSI processing.

A variation of the method was used by Horiike et al. (1990). Triethylesilane (TES) and H, created in a remote microwave source, produced C_xH_y radicals which were deposited on a c-Si wafer and then oxidized, layer-by-layer. The excellent step coverage was attributed to the high viscosity of the radicals. The deposition temperature was 350°C. Both deposition rate and conformality were a function of the H_2 concentration, peaking at about 60% H_2. At high H_2 concentration an overhang structure was formed, instead of filling from bottom to top The films contained organic species and further work was needed to improve the film quality.

4.2.5.5 Liquid-Phase Oxidation

Trimethylsilane (TMS) was reacted with O atoms, generated in a microwave discharge chamber, on a substrate cooled by liquid nitrogen (Noguchi et al., 1987). Hirose (1988) used the phrase liquifaction CVD. The deposition rate increased with decreasing substrate temperature, reaching a maximum value at about 20°C, decreasing with further decrease in temperature. Above about –20°C, the step coverage was typical of CVD films, i.e., an overhang profile with sidewall coverage decreasing as the depth increased. Below that temperature, the profile changed and deep narrow grooves were filled completely, reminiscent of liquid flowing into a hole. The proposed mechanism is consistent with that view: as the substrate temperature is lowered, the partially oxidized condensate migrates readily on the Si surface, filling corners; continued growth maintains the initial profile. Thus, oxidation occurred in the liquid phase. The as-deposited film resembles PECVD HMDS. Annealing in O_2 at 300°C for one hour densified the film by about 15%, reduced the Si–OH band, shifted the Si–O–Si band, but had almost no effect on the intensity of the $Si–CH_3$ band. Although the ability to fill gaps and thereby planarize the surface is a useful property, the nature of the film appears to make it unsuitable for VLSI application.

4.2.5.6 Liquid-Phase Deposition (LPD)

There has been a substantial amount of work done in this field, but only by investigators from Taiwan and Japan. It has been used exclusively to deposit F-doped SiO_2 and is discussed in Section 4.2.7.

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4.2.6 Doped Oxides

In this section the effects of the dopants B, P, B/P (Kern and Heim, 1970; Kern and Rosler, 1977), As (Ashwell and Wright, 1985), and Ge (Chien et al, 1984; Thakur et al., 1994) are discussed. The doped oxides, called BSG, PSG, BPSG, etc., are not mixed oxides, but are silicate glasses as shown by IR absorption and etch rate measurements (Kern and Fisher, 1970). One of the uses of these dopants is to reduce the flow temperature of SiO_2. B is most effective; it greatly reduces the viscosity of the oxide because the smaller atom can enter the interstitial positions easily to weaken the Si–O bond (Malik and Solanski, 1990). The flow temperature reduction improves with increasing dopant concentration, but as the concentrations of dopant increase, the films become unstable to moisture. Also, since the tendency of B to form boric acid is less than that of P to form phosphoric acid, BSG appears to be preferable to PSG for this application. Mixtures of dopants are used since flow at lower temperatures can be achieved with reduced sensitivity to moisture. BSG, PSG, and BPSG have other properties (discussed below) besides promoting flow; As (Ashwell et al., 1985) and Ge (Chien et al., 1994; Thakur et al., 1994) are used alone or in combination with other dopants only to promote flowage which is discussed in a later section.

Doped oxides have been deposited using APCVD (Kern), LPCVD (Kern), SACVD (Robles et al., 1995), and PECVD (Law et al., 1989). The growth temperature has been in the range of about 300 to 800°C. The Si sources have been usually SiH_4 and TEOS, although $SiCl_4$, tetrapropoxysilane, and, in the case of BSG, $(CH_3)_3SiBO_3$ (tris(trimethyl)siloxy boron or tris(trimethyl)silyl borate, abbreviated as SiOB) have also been used. The oxidant has been O_2, O_3, or N_2O. Pyrolysis of TEOS has been another option (Becker and Rohl, 1987). The most widely used P-dopants have been PH_3, trimethyl phosphite (TMP), and trimethyl phosphate (TMPO), although PCl_3 and $POCl_3$ were used in the earlier days. The B-sources in common use are B_2H_6 and trimethyl borate (TMB); SiOB has been used more recently. Tri-*n*-propyl borate and BCl_3 have also been mentioned.

4.2.6.1 PSG

Shioya and Maeda (1986) reported that the preparation method of PSG films deposited from the hydrides affected many of the properties of the films; their results are summarized in Table 4.2. However, it should be noted that the PECVD films were deposited at a lower temperature (300°C) than is customary. The density of all the films increased slightly and their etch rates in HF solution increased markedly with increasing P-concentration, although the refractive index did not. The etch rate of PSG in HF solution can be used to measure the P-concentration (Pliskin, 1977). The PECVD films had superior crack resistance; the APCVD films were most susceptible, although P-doping did improve their resistance.

The P in PSG exists as P(V) and P(III) (Tong et al., 1984; Houskova, 1985; Treichel et al., 1990). Both P–Si (interstitial, i.e., P replacing O in and interspersed between the SiO_2 tetrahedra) and P–O (substitutional, i.e., P substituting for Si in the SiO_2 tetrahedra) states were detected by ESCA in 8 wt% P CVD films and P-implanted thermal oxide (Wu and Saxena, 1985). The populations of these bonding states depend on deposition and annealing conditions. In CVD films, P–Si > P–O, as deposited, but conversion of P–Si to P–O upon annealing has been observed. Wu and Saxena (1985) also postulated that reflow, stress, and etch rates might depend on the relative populations of the states, but did not venture to say just how.

One of the most important effects of P-doping is the inhibition of the movement of cations (usually Na^+) in the presence of an electric field, since Na^+ will move rapidly through an SiO_2 film under the influence of a field and change the threshold voltage of an FET device. PSG "acts as a getter of Na^+ and a barrier against Na^+ drift" (Balk and Eldridge, 1969). Kern and Smeltzer (1985) concluded that the protective mechanism was solely gettering, at least in APCVD BPSG, but whether this is true for all BPSG films has not been confirmed. The protective effects of P-doping

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Table 4.2 Properties of PSG Films vs. %PH_3 in Feed Gas

Property	Plasma	LPCVD	APCVD
Deposition rate	—	—	Incr. monotonic × 6 at 20%
Etch rate in HF	Incr.; highest	Incr.; intermediate	Incr., lowest
RI	—	—	—
Density	Incr. slightly; highest	Incr. slightly; intermediate	Incr. slightly; lowest
Stress	C → T ~7%	C → T ~7%	T → C; monotonic
Stress after anneal	If C, min. ~600°C; if T, T → C at ~800°C	If C, min. ~600°C; if T, T → C at ~800°C	T → C; monotonic
IR: P = O	Incr; intermediate	Incr.; lowest	Incr.; highest
ε ~ 3.8–4.5	Highest	Lowest	Intermediate
	Incr. slightly	—	—
ε after anneal	—	—	—
Almost identical			
ε ~ 3.5–3.9			
Breakdown field	Decr. slightly	Incr. slightly	Incr. slightly
	Lowest	~Same as APCVD	~Same as LPCVD
Absorption water vapor[a]			
IR: SiOH	Highest	Intermediate	Lowest
IR: P = O	None	None	Some
Etch rate after water vapor	Decr	Decr	Decr

Note: —, little or no change.
[a] Water vapor treatment: 2 atm, 120°C, 2 hours.

increase with increasing P-concentration. However, since the polarizability also increases with increasing P-concentration, too high a concentration will result in instability. Another factor that places an upper limit to the P-concentration is that the films become increasingly hygroscopic with increasing P-content, resulting in corrosion of Al-based wiring insulated with PSG (Paulsen and Kirk, 1974; Bhide and Eldridge, 1983). Si–OH bonds and physically absorbed H_2O can be detected in a PSG film, after it has been exposed to water vapor at temperatures of 70 to 100°C, using IR spectroscopy. The dielectric constant of CVD PSG prepared from the hydrides was reported to be close to that of fused silica (Kern and Heim, 1970). The effects of deposition method and P-concentration on the electrical properties of hydride-based PSG films, as measured by Shioya and Maeda (1986), are given in Table 4.2.

However, the dielectric constant of PECVD PSG, prepared using TEOS, O_2, and TMP at a temperature of 390°C was lower than that reported by Shioya and Maeda, as might be expected in light of the higher deposition temperature. In this case as well, there was no change in ε as the P concentration was increased until about 4 wt% P was incorporated in the film and then it increased slightly (from 4.07 to 4.27 at 10 wt% P).

Another advantage of the use of PSG is the ability to etch it selectively with respect to the undoped oxide in CF_4/H_2 mixtures. Almost infinite selectivity is possible, depending on the P-content of the PSG and the H_2 concentration in the etch gas (Vender et al., 1993).

4.2.6.2 BSG

White et al. (1990) reported that for APCVD BSG, incorporation of B ($\leq$4.5 wt% B) by the addition of diborane to SiH_4/O_2 mixtures produced films stable to moisture, with moderate tensile stress, high breakdown strength, and a lower dielectric constant than the undoped film (3.8 vs. 4.1) and these films could be candidates for use as an interlevel dielectric. Both B–O (1380 cm^{-1}) and Si–O bands are found in the IR spectrum. B-doped films tend to have a high silanol content and

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bind water in their structure, so that upon exposure to the atmosphere, the tensile stress is reduced. Moreover, if the concentration of B in the films is too high, they are unstable with respect to moisture attack, decomposing into boric acid.

APCVD BSG films were also prepared by the addition of either TMB or SiOB to a TEOS/O_3 mixture (Fujino et al., 1991a); there were no major differences in the film due to the dopant source. Step coverage was very good whether the BSG was deposited using TEOS + O_3 and a boron dopant (TMB) or just SiOB + O_3. They reported on the effects on a number of properties of changes in temperature and dopant flow rate for TMB (Figure 4.5a), for SiOB (Figure 4.5b), and the effect of O_3 concentration for the SiOB + O_3 deposition (Figure 4.5c). The deposition rate of the BSG films was substrate material dependent as was that of the undoped oxide. The leakage current of the TMB/BSG films was very low, without annealing, and was independent of the dopant concentration (measured to 9 mol% B). Higher O_3 concentration in the reaction mixture resulted in denser films with the lower leakage. The B–O peak did not change after exposure to the atmosphere, but the Si–OH peak increased. The advantage of SiOB is the existence of the B–O–Si bond leading to an integrated network; Fujino et al. (1991a) stated that TMB/BSG is a mixture of SiO_2 and B_2O_3, which contrasts the conclusion of Kern and Fisher (1970). Yuyama et al. (1994) prepared CVD BSG

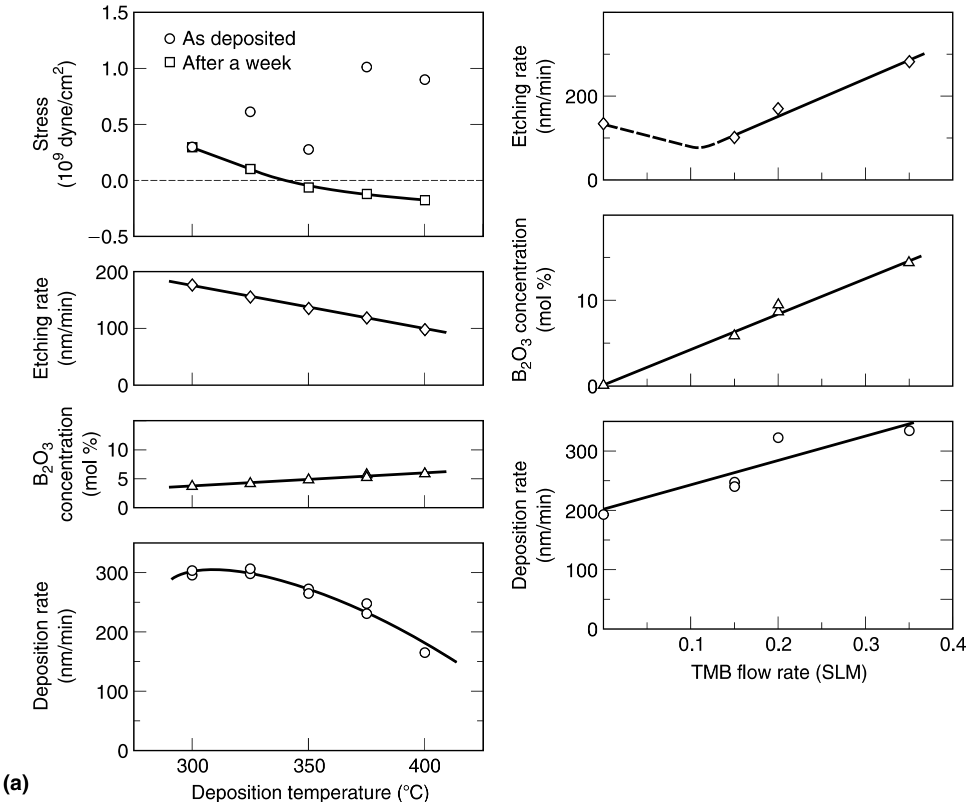

Figure 4.5 (a) APCVD TEOS-based TMP/BSG films. Left (from top to bottom): stress, wet etch rate, B_2O_3 concentration, and deposition rate vs. deposition temperature. Right (from top to bottom): Wet etch rate, B_2O_3 concentration, and deposition rate vs. TMB flow rate. (b) APCVD TEOS-based SiOB/BSG films. Left (from top to bottom): stress, wet etch rate, B_2O_3 concentration, and deposition rate vs. deposition temperature. Right (from top to bottom): wet etch rate and deposition rate vs. SiOB flow rate. (c) APCVD TEOS-based SiOB/BSG films. From top to bottom: stress, B_2O_3 concentration, and deposition rate and wet etch rate vs. ozone concentration. (Reproduced from Fujino, K., Y. Nishimoto, T. Tokumasu, and K. Maeda, *J. Electrochem. Soc.*, 138, 550, 1991. With permission of the Electrochemical Society, Inc.)

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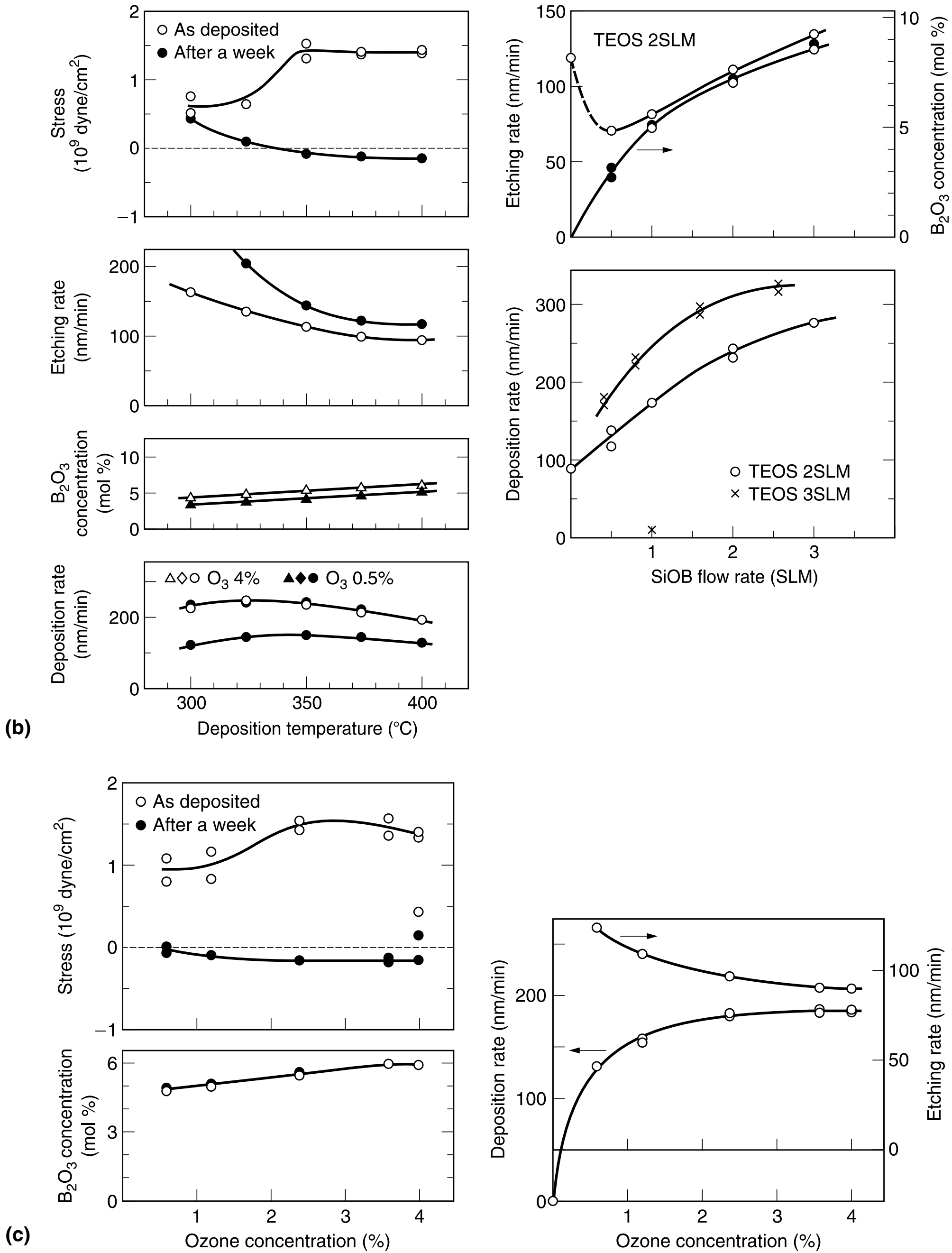

Figure 4.5 (Continued)

(6 wt% B) using SiOB and O_3. The as-deposited film had a high water content (4.4 % H_2O) and $\varepsilon = 4.37$. A postdeposition treatment for 3 minutes in a N_2 plasma eliminated the water completely and reduced ε to 3.35; neither exposure to an O_2 plasma nor annealing in a furnace at 750°C was as effective in eliminating the water (a surprising result for the high-temperature anneal) or lowering ε as much. Their results indicated that the reduction of the moisture, *per se*, cannot account for the low dielectric constant, since the dielectric constant of an undoped film with equivalent water

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content was much higher. PECVD BGS was prepared using TEOS, O_2, and TMB. The results were similar to those reported by White, i.e., the dielectric constant for a film with B = 3.6 wt% was 3.87 vs. 4.03 for the undoped film (Schwartz and Chapple-Sokol, 1992).

4.2.6.3 BPSG

BPSG is the doped oxide used most extensively as an interlevel dielectric film since it combines the protection against the instability due to ionic contaminants of PSG with the reduced flow temperature of BSG. Table 4.3 summarizes the effect of some of the process variables on the deposition process and film properties for SACVD BPSG (Robles et al., 1995). Rojas et al. (1992) compared BPSG deposited using PCVD, LPCVD, and PECVD using liquid and gaseous sources. They concluded that films deposited using a higher-temperature TEOS-based LPCVD process had superior chemical and physical properties.

The value of ε of BPSG films prepared by CVD from the hydrides appears to depend on the composition, preparation method, and annealing (densification) conditions (Kern and Heim, 1970; Kern and Schnable, 1982) and was in the range 3.8 to 4.5 (after fusion). Treichel et al. (1990) reported that for a PECVD film, deposited using SiOB, O_2, and TMP (3.6 wt% B/4.2 wt% P), ε was 3.3. In contrast, for a BPSG film, prepared in the same model of reactor, at the same temperature, but using TEOS, O_2, TMP, and TMB, and having the same composition and IR spectrum, ε was ~4 (Schwartz and Chapple-Sokol, 1992). The result of Treichel et al. is another example of the use of SiOB as both a Si and B source producing a film with an exceptionally low value of ε. Treichel et al. also reported that the spectra of the films deposited using TEOS and TMB (+TMP) and SiOB (+TMP) were virtually identical, indicating no gross structural difference. Thus it is difficult to explain the discrepancy between the results of Treichel et al. and Schwartz and Chapple-Sokol, or the role of the specific reactants. It may be recalled that Fujino et al., in depositing BSG, found that the B-dopant source (TMB or SiOB) had no major effect on the film properties. However, they did not measure ε.

Other papers of interest, not discussed here, are Levy et al. (1987), Pignatel et al. (1991), Rojas et al. (1992), and Dobkin (1992). The paper by Becker et al. (1986) includes an extensive bibliography.

4.2.7 F-Doped SiO_2

Incorporating fluorine in the silica network reduces both the dielectric constant (ε) and, to a lesser extent, the refractive index (n). F-doped SiO_2 (sometimes called fluorosilicate glass, FSG) films were the first low dielectric constant films to be used in the commercial production of ICs. These films also exhibit enhanced step coverage and gap-filling properties, discussed in another chapter.

Earlier work on F-doping was directed toward improving the quality of oxide films deposited at low temperatures or for improving the gap-filling capability rather than for the reduction of ε.

Table 4.3 Effect of Deposition Variables on Properties of SACVD BPSG Films

	Increasing Variables				
	Pressure (torr)	O_2 conc. (wt%)	B (wt%)	P (wt%)	Anneal (°C)
Deposition rate	decr	none	incr	incr	not tested
% Shrinkage	none	decr	sl. decr	decr	incr
Wet etch rate	none	none	decr	incr	none
Reflow angle	none	decr	decr	sl. decr	decr

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Falcony et al. (1993), using SiF_4 additions to SiH_4/N_2O mixtures, had relied on the affinity of F for H to minimize or eliminate H incorporation in SiO_2 films deposited at low temperature. Homma et al. (1993) used a F-substituted organic precursor and water for improved flow during room-temperature CVD of SiO_2 by forming precursor oligomers which condense, flow, and then polymerize on the surface. NF_3 was added to the reaction mixture in PECVD of SiO_2 (Ibbotson, 1990) to suppress sidewall growth for improved gap fill. Incorporation of F into the gate oxide increased the radiation hardness of MOS devices (deSilva, et al., 1987; Ahn et al., 1991).

LPD was introduced as a process for coating a silica film on the surface of glass at a low temperature ($\geq 40°C$). Fluorine was incorporated (up to ~5%) into SiO_2 (Nagayama et al., 1988). LPD was originally carried out by reacting boric acid with a silica-saturated solution of hydrofluosilicic acid, to precipitate, after a series of reaction steps, F-doped SiO_2 (Homma et al., 1990, 1993). F-incorporation lowered the value of ε to 3.7 (Homma et al., 1991). The deposition rate was low, in the range ~100 to 300 Å/h. Chang et al. (1997) summarized work on LPD of SiO_2 by boric acid addition. The deposition process is surface controlled. The deposition rate varies approximately linearly with temperature and increases with increasing boric acid concentration, and is constant over time. They discussed the role of water as a reagent and the effect of the sequence of adding SiO_2.

Chou and Lee (1994) investigated the initial growth mechanism. They proposed that the chemical reaction that replaces Si–H surface bonds with Si–OH bonds as well as the formation of intermediate products are rate-limiting processes. Oxide growth occurs only when the concentration of HF (a reaction byproduct) is less than some critical value which depends on the condition of the surface.

Exposure to 254 nm UV illumination enhanced the deposition rate of LPD SiO_2. The enhancement was greater at higher concentrations of hydrofluosilicic acid and dependent on the concentration of boric acid. The increase was attributed to the increased concentration of intermediate species due to the activation of SiF_6^{2-} species by UV exposure (Huang et al., 1996).

In later work, films were deposited without boric acid (Yeh et al., 1994), adding only H_2O to the silica-saturated hydrofluosilicic acid. Increasing the amount of water added increased the growth rate and the SiOH concentration but decreased the F-concentration and film density (Yeh and Chen, 1995). The LPD oxide is somewhat O-deficient and can be represented as $SiO_{2-x}F_x$. Both SiOH and water bands are observed in the FTIR spectra. The stress in such films is tensile; the lower the concentration of water, the lower the stress (Yeh et al., 1996). Yeh et al. (2000) found that the dielectric constant and stress were lowest (3.5 and 43 mPa) when the deposition temperature was maintained at 25°C, both increasing at 15°C and at 35°C. They attributed this to the high F-content, low OH content, and low bond strain. Stress hysteresis was observed upon thermal cycling. The stress increased upon thermal annealing.

The selectivity of LPD (oxide deposition requires the existence of –OH groups on the underlying surface so that no oxide was deposited, e.g., on photoresist or W) with the potential for planarization was the advantage claimed for the process (Homma et al., 1990, 1991, 1993).

Annealing the films increased the density and refractive index, and decreased the "P" etch rate and the Si–F band intensity. FTIR spectra, showing a shift and broadening of the Si–O–Si peak, indicate partial restructuring of the oxide during anneal (Yeh et al., 1995; Yeh and Chen, 1995).

The current method of choice for depositing F-doped oxide is PECVD. Among the earliest reports of F-doped SiO_2 prepared using PECVD was that by Usami et al. (1993) in a parallel plate reactor and by Takada and Akahori (1993) in an ECR system. A capacitively coupled reactor has been used most frequently in later studies. In addition to ECR, dual-frequency, helicon, ICP, unspecified high-density, and remote systems have also been reported.

Only limited work has been done using thermal CVD. Table 4.4 summarizes the F-sources, the basic reaction mixtures to which the dopant is added, and the type of reactor used for PECVD and CVD deposition of F-doped SiO_2 with lower ε for potential use as interlevel dielectrics.

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Table 4.4 F-Doped SiO_2: Deposition Techniques, F-Sources, Basic Reaction Mixtures

Deposition technique	F-source	Basic Reaction Mixture	Reference
PECVD	C_2F_6	$TEOS/O_2$	Usami et al. (1993, 1995)
PECVD/dual frequency	C_2F_6	$TEOS/O_2$	Carl et al. (1995a,b), Mizuno et al. (1995), Matsuda et al. (1995), Takeishi et al. (1995)
PECVD/dual frequency	SiF_4	$TEOS/O_2$	Matsuda et al. (1995)
PECVD/dual frequency	FTES (TEFS)	$TEOS/O_2$	Mizuno et al. (1995)
PECVD/bias ECR	SiF_4	$SiF_4/O_2/Ar$	Fukada and Akahori (1993)
PECVD/bias ECR	SiF_4	$SiH_4/O_2/Ar$	Fikada and Akahori (1995)
HD plasma	SiF_4	$SiF_4/O_2/Ar$	Carl et al. (1995a,b), Qian et al. (1995)
LTAPCVD	FTES (TEFS)	$TEOS/O_3$	Yuan et al. (1995)
RPECVD	SF_6	$TEOS/O_2$	Yu et al. (1995)
RTAPCVD	FTES	$TEOS/H_2O$	Homma (1996)
$\mu\lambda$PECVD	FASi-4[a]	O_2	Virmani et al. (1996)

[a] FASi-4: bis(methyldifluorosilylilyl)ethane.

Although these PECVD films are sometimes referred to as SiOF, this does not reflect the stoichiometry; the F-content is usually < 10 at%. Yang and Lucovsky (1997) suggested that since, in the limit, there is one F atom bonded to each Si atom, "the resulting pseudo-compound composition is $Si_2O_3F_2$. At lower F-concentrations, the film might be described as a mixture of SiO_2 and $Si_2O_3F_2$ where a pseudobinary alloy notation $(SiO_2)_x(Si_2O_3F_2)_{1-x}$ is appropriate."

Incorporation of F in the SiO_2 network, i.e., the existence of an Si–F bond, has been demonstrated by XPS (the Si–F peak at 687.3 eV) and a band in the IR spectrum at ~935 cm^{-1}. Although Tamura et al (1996) and Han and Aydil (1997) refer to SiF_2 bonds, Lucovsky and Yang (1997) stated that there is no definitive spectroscopic evidence for them, up to ~12 at% F. Other changes in the SiO_2 network, revealed in the IR spectrum, are (1) a shift in the position of the Si–O–Si bond-stretching peak from ~1060 cm^{-1} to higher wavenumbers and a reduction in its peak width, (2) a reduction in the integrated IR absorption strengths of the Si–O–Si bond-bending (~810 cm^{-1}) and rocking modes (~465 cm^{-1}), and (3) an increase in the Si–O–Si bond angle of ~5° to 10°, reducing the density of the film (Usami et al., 1993, 1994; Nakasaki and Hayasaka, 1994; Matsuda et al. 1995; Lim et al., 1996; Lucovsky and Yang, 1997; Yang and Lucovsky. 1997; Han and Aydil, 1997; Iacona et al., 2001). Another characteristic of F-doped SiO_2 is the low concentration, or in some cases the absence, of Si–OH bonds probably due to the scavenging of H by F. SIMS measurements showed that the concentration of F is uniform throughout the film (Usami et al., 1994).

The electronic, ionic, and orientation (dipolar) components of the dielectric constant of a material are shown in Figure 4.6. All of them contribute to the value of ε as determined by C–V measurements (at >10 kHz). The electronic polarization equals n^2. Since F-doping results in only a small decrease in n, the decrease in electronic polarization is a not a large effect.

The replacement of strongly IR-active Si–O–Si with weaker Si–F bonds contributes to the reduction in ε. As discussed above, the presence of Si–F bonds induces changes in the IR spectrum, i.e., in the vibration modes, which result in a large decrease in the ionic polarization component of the dielectric constant. According to Lucovsky and Yang (1997) this is the primary factor contributing to the decrease in ε.

If there is no orientation polarization, as is the case for pure SiO_2, the difference between ε as determined by C–V measurements and n^2 can be attributed to ionic polarization. To test this assumption, Lim et al. (1996) and Shimogaki et al. (1996) analyzed the IR spectrum using the Kramers–Kronig relationship to calculate the components of the dielectric constant and concluded that the decrease in ionic polarization (due to the changes in the Si–O stretching and rocking modes) was the most important factor in the reduction of ε.

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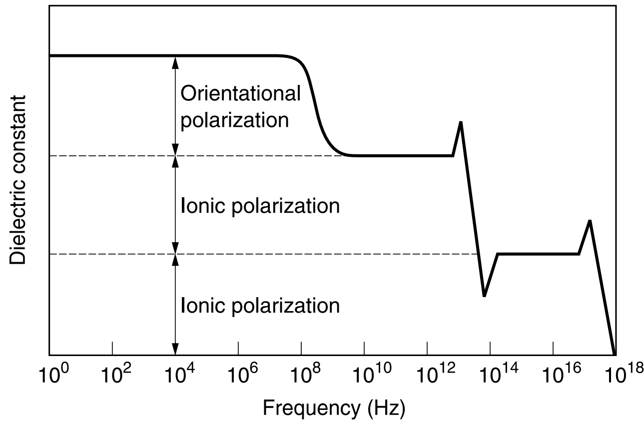


Figure 4.6 Dispersion of the dielectric constant (ε vs. frequency).

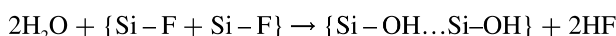
PECVD SiO_2 films contain Si–OH bonds, increasing ε over that of thermal SiO_2. Thus, another contribution to the reduction of ε is the replacement of most, if not all, of the more polarizable Si–OH bond by Si–F. Although this is merely mentioned in passing by some authors, Lim et al. (1999) demonstrated this effect more dramatically. They chose operating parameters that resulted in an undoped PECVD SiO_2 film with an unusually high content of SiOH, i.e., an unusually high value of ε (~4.5). Figure 4.7 shows the results of adding an F-source to the reaction mixture. The decrease in the electronic and ionic polarization, calculated using the Kramers–Kronig relationship, was about the same as reported earlier but these were too small to explain the reduction in ε obtained from *C–V* measurements. Lim et al. therefore attributed a major role to a decrease in orientation (dipolar) polarization as Si–F replaces Si–OH. Any residual orientation polarization, due to absorbed moisture, can be estimated determining the dielectric constant before and after annealing.

Finally, the reduction in density is reflected in a decrease in ε.

The usual oxidant in PECVD processes is O_2, although Hsieh et al. (1996) used N_2O in place of O_2 in a TEOS/C_2F_6-based process. They found reduced dependence of the deposition rate on temperature (implying a shift in the deposition mechanism) and the F-doping was more efficient but films of equal F-content were similar to those deposited using O_2. The differences in film properties which have been attributed to the method of deposition and to the kind of reactor used for PECVD are discussed below.

The F-source used in the deposition reaction affects the film properties. One important distinction among possible sources is whether the Si–F bond is present in the source molecule (e.g., SiF_4) or whether F must be formed in the plasma (e.g., from C_2F_6) and then react with the Si source to form the Si–F bond. This is discussed in more detail below.

As the flow rate of the F-source compound increases, the F-content of the film increases and the values for ε and refractive index of the deposited oxide decrease (Saproo et al., 1996; Lim et al., 1997) and are sometimes shown to saturate at high flow rates (Yu et al., 1995; Weise et al., 1997). Films with a very high F-content (~12 at%) have been prepared, but they are unstable when exposed to moisture. This is a result of the attack of the Si–F bond by water molecules producing Si–OH bonds, increasing ε. Mizuno et al. (1995a) stated that film stability played a major role in determining the lowest possible value of ε, i.e., the highest practical F-content, so that the stability of *all* SiOF films has become an important issue. Yang and Lucovsky (1998) show the reaction as



$$2H_2O + \{Si-F + Si-F\} \rightarrow \{Si-OH\ldots Si\text{–}OH\} + 2HF$$

where { } indicates nearest neighbors and … hydrogen bonding.

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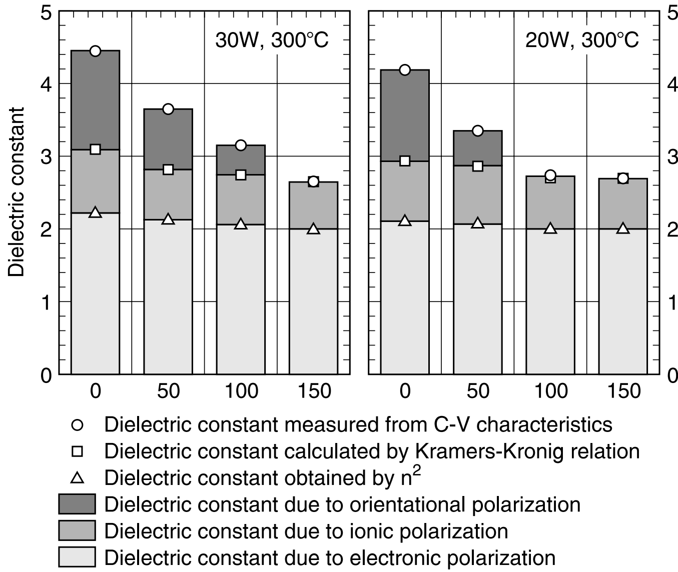

Figure 4.7 Changes in the dielectric constant of SiO_2 determined, by *C–V* measurement, Kramers–Kronig relation, and n^2 as the flow rate of CF_4 added to SiH_4/N_2O increases. (Reproduced from Lim, S.W., Y. Shimogaki, Y. Nakano, K. Tada, and H. Komiyama, *J. Electrochem. Soc.*, 146, 4196, 1999. With permission of the Electrochemical Society, Inc.)

They emphasized the role of the paired Si–F arrangement which becomes more important as the concentration of F increases. Their analysis yielded an upper limit for chemically stable F incorporation (~10 to 12 at% F) and a lower limit for ε (3.2 to 3.4). Kim et al. (1999) reported that addition of Ar to the reaction mixture improved the moisture resistance of the film. There is disagreement in the literature about the practical limit to the concentration of fluorine in the film, probably due to differences in the reactor configuration, choice of reactants, and process conditions. Carl et al. (1995a,b) and Passemard et al. (1996) concurred that films containing more than ~3 to 4 at% F were unstable, absorbing moisture readily and outgassing, thus possibly resulting in blistering and increasing the susceptibility of the interconnection wiring to corrosion as well as in interface problems. Saproo et al. (1996), however, reported that the film stability was a complicated function of the process conditions and did not depend solely upon the F-content; they prepared stable films with F-concentrations as high as 11.5 at% and unstable ones with lower F-content. Increasing the deposition temperature improved stability. The use of bias in helicon plasma CVD also improved the stability of low dielectric constant SiOF films (Tamura et al., 1996).

In situ capping with undoped oxide, although it increases ε, protects the film from atmospheric moisture and acts as a barrier to out-diffusion of both water and F, reducing the problems of instability, although the sidewalls of etched vias and trenches are not protected. The use of cluster tools, i.e., integrated processing, reduces the exposure of the film to moisture and thus may extend the useful range of F-doping.

The lowest value of ε has often been found to be about 75% of that of the undoped oxide prepared under the same conditions. This comparison is often omitted, and only the ultimate value is given, so that it is difficult to assess the effectiveness of the process. The F-content does not, itself, determine ε. For a given F-content, the value of ε depends on the reactor, reaction mixture, and processing conditions. These factors also determine the value of ε for the undoped film to which the F-doped film is compared. The lowest value of ε reported is about 2.3 (Lim, 1995; Lim et al., 1996) but such a film was not very stable (Shimogaki et al., 1996).

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Annealing at 400°C decreased the value of ε (Usami et al., 1994). The investigators used an H_2 ambient and annealed for 30 minutes and reported that the decrease was smallest for the film with the highest F-content. However, Lim et al. (1996) and Shimogaki et al. (1996) reported the opposite trend, i.e., the higher the F-content of the film, the greater the reduction after annealing for 10 minutes (ambient not given).

As stated above, Si–OH is either absent or present in minute quantities in most F-doped oxides. However, Mizuno (1995a,b) reported that there was a significant Si–OH peak in the films deposited using either C_2F_6 or triethoxyfluorosilane (TEFS) in a dual-frequency reactor and this could be reduced only by capping the film with undoped oxide. Higher temperature deposition or annealing were ineffective.

The change in deposition rate with increasing flow rate of the F-source compound depends on the compound and on the base reaction mixture. For example, in a dual-frequency reactor using TEOS/O_2/SiF_4, the rate decreased and then increased (Matsuda et al., 1995); in a single-frequency reactor using TEOS/O_2/C_2F_6, the rate decreased monotonically (Usami et al., 1993, 1994); in a biased ECR reactor, the rate increased linearly in an SiF_4/O_2/Ar mixture (Fukada and Akahori, 1993) but decreased in an SiF_4/SiH_4/O_2 mixture (Fukada and Akahori, 1995).

The advantage to using an F-source that has Si–F bonds in its structure is thought to be related to the fact that the Si–F units are probably incorporated directly into the silica network whereas Si–F bonds must be formed by reaction of F with the network when F is supplied by the dissociation in the plasma. There is experimental evidence to support the conjecture that the latter type of bond is weaker and more reactive than the former. Shapiro et al. (1995) and Matsuda et al. (1995) reported that, for dual-frequency films, uptake of moisture was more immediate and reached a higher level for the C_2F_6-based films than for the SiF_4-based ones and HF evolution upon heating was greater for the former films. Mizuno (1995a,b) reported that, for the same Si–F content, films made using C_2F_6 had a slightly higher value of ε than those prepared using TEFS, perhaps due to moisture absorption. In addition, HF evolution upon heating mixed-frequency films began at a lower temperature for C_2F_6-based films than for triethyoxyfluorosilane (TEFS or FTES)-based ones. This appears to be a consequence of the fact that there is less unbonded F when SiF_4 or TEFS is used instead of C_2F_6, since there is less dissociation of the Si–F bond in the plasma and, therefore, less F_2 to react with water from the atmosphere (Matsuda et al., 1995). Lee et al. (1996) proposed that the presence of an Si–F bond in the precursor (ethoxyfluorosilane) was responsible for the fact the films had a higher density and were more resistant to moisture absorption than those deposited using C_2F_6. Rana et al. (1997) found that SiF_4-based films had a greater thermal stability than FETS-based ones but recommended a maximum F-content of 2.5%, limiting the reduction in ε. Fukada et al. (1998) stated that precursors that generated hydrogen species, such as $SiF_4 + SiH_4$, resulted in films that were very resistant to moisture absorption, i.e., to changes in dielectric constant upon exposure to air.

Takeishi et al. (1995, 1996) reported that the value of ε for films prepared in a dual-frequency reactor using C_2F_6/TEOS/O_2 increased upon exposure to air but that annealing the film in an N_2O plasma stabilized them. Swope et al. (1996, 1997) emphasized that the effect was confined to the surface, that the bulk properties were unaffected. They also found that the plasma treatment could enhance the adhesion to SiN of high F-content films, without changing the moisture stability. Exposure of SiOF films to an ECR O_2 plasma increased the surface roughness, decreased the etch rate in BHF, increased the refractive index, density, and dielectric constant from 3.14 to 3.43, but blocked moisture absorption.

It appears that high-energy ion bombardment of the substrate *may* blur the distinction of the type of F-source. Equivalent results, i.e., good stability toward moisture, were obtained when using C_2F_6/TEOS/O_2 in a dual-frequency reactor in which the low-frequency power was very high and an ICP reactor using SiF_4/O_2/Ar. With lower low-frequency power, i.e., with less energetic ion bombardment, the C_2F_6-based SiOF films were inferior (Carl, 1995a,b). These results can be

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explained by ion bombardment densification of the film. In contrast, Mizuno et al. (1995a,b), using a dual-frequency reactor, reported that the wet etch rate of their C_2F_6-based, high-power, low-frequency, high-F-content films increased with increasing high-energy bombardment. They inferred a lower density due to breaking of the weak Si–F bond. However, the TEFS-based oxide became denser, i.e., the etch rate was lower at higher bombardment energies.

The compressive stress in the film decreases with increasing F-content. It has been suggested that F-incorporation loosens the structure so that the stress becomes more tensile and more unstable. However, for the same F-content, increasing the ion bombardment (e.g., by increasing the low-frequency power in a dual-frequency reactor) increased the compressive stress of the film (Carl et al., 1995a). They postulated that ion bombardment densifies the film, making the stress more compressive and more stable. The influence of the source of F is again emphasized in the work of Mizuno et al. (1995a,b). They found the same trend in stress with increasing low-frequency power for a TEFS/TEOS-based oxide; the largest change in film stress was for films deposited using the lowest TEFS/TEOS ratios. There was a decrease in tensile stress at low low-frequency power, but this trend was reversed as the power was increased. Only for the films prepared with the lowest C_2F_6 flow rate in the reactant mixture did the stress eventually become and remain compressive, although at the highest low-frequency power there was a trend toward lower compressive stress. This was explained by the weaker F-bonding in the C_2F_6-based oxide. High-energy ion bombardment breaks the bond, releasing F, so that a more porous film is produced.

Both the elastic modulus and hardness decrease with increasing incorporation of F in the film. For example, for a film deposited in a dual-frequency reactor using TEOS/O_2 as the base mixture, E decreased from 167 to 100 GPa and H from 20.4 to 12 GPa when C_2F_6 was added to dope the film with 7.5% F; at this F-content the stress became tensile (Tseng et al., 1997). The reduction in the values of the mechanical properties is almost insignificant, however, when compared to the more than order of magnitude lower values measured for the very-low-ε films described in later sections.

Fukada and Akahori (1993) first reported a relatively high breakdown strength (6 to 8 MV/cm) for SiOF films deposited using SiF_4 and O_2, but later (Fukada and Akahori, 1995) reported, for the same kind of film, a very soft breakdown of < 3 MV/cm. The ultimate leakage current, however, was lower than that of several other films in current use, as shown in Figure 4.8. This breakdown strength may be adequate for an interlevel dielectric.

The etch rates in HF-based solutions and in reactive ion etching (RIE) are increased as the F-content increased. This may be attributed to reduced density and to F released during etching.

Increasing the F-content of SiO_2 does continue to reduce the value of ε down to some limiting value. It is used in the production of high-speed chips and will continue to be used until the integration and reliability of the lower ε materials are proved to be satisfactory. For lower speed requirements the use of F-doped SiO_2 may continue even longer, since, as stated above, the processes, tools used, and many of its properties, are similar to the familiar ones of undoped SiO_2.

4.2.8 Contaminants: H and Ar

4.2.8.1 Hydrogen

H is incorporated into many deposited SiO_2 films. The amount incorporated and the bonding depend on the method of preparation and on the temperature; in general, the higher the temperature, the lower the H-content. H-bonds are formed, as silanols, Si–OH, either H-bonded (IR absorption at 3650 cm^{-1}) or free (3740–3750 cm^{-1}), as absorbed H_2O (at 3300–3400 cm^{-1}), or as Si–H (~2100–2300 cm^{-1}) (Pliskin, 1973). Incorporation of water may possibly occur during deposition or, more likely, by entrapment after the film is formed, within the reactor or after exposure to moisture in the environment. Adams and Douglas (1959) proposed that inclusion of OH groups involves

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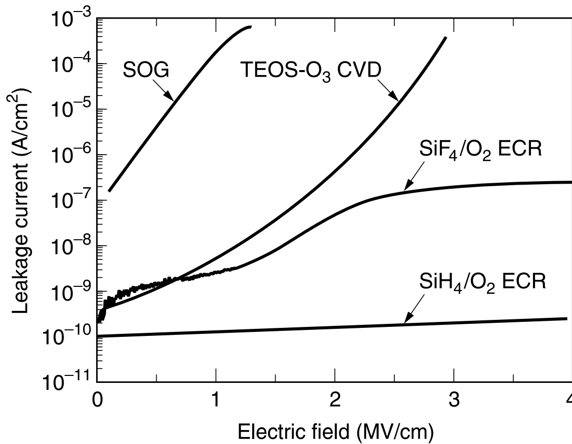

Figure 4.8 Leakage current vs. electric field for several dielectric films. (Reproduced from Fukada, T. and T. Akahori, DUMIC, 1995, p. 43. With permission.)

the breaking of Si–O–Si bridges, i.e., Si–O–Si + H_2O = Si–OH HO–Si. Films formed by chemical reactions, i.e., CVD (thermal or plasma assisted) usually contain H. Bias-sputtered SiO_2 films contain a negligible amount of Si–OH and no water, but films sputtered at low bias tend to be porous and, therefore, absorb atmospheric moisture readily.

Whatever the source or type of bonding, e.g., as Si–H or as Si–OH, the effect of H incorporation is to increase the dielectric constant of the film, and thus increase the signal propagation delay. The relationship between OH content and ε has long been recognized. The IR spectra showed that "water" in fused silica was present as Si–OH (Adams and Douglas, 1959). The value of ε increased linearly with increasing OH content (Andeen et al., 1974). This trend was also observed in SiO_2 films deposited using SiH_4 and O_2 in an ECR plasma reactor (Lassig, et al., 1993). The dielectric constant of PECVD oxides (using TEOS and O_2 in a capacitively coupled reactor) increased linearly with increasing total H (OH + H_2O) content (Patrick et al., 1992). In the case of films formed in an ECR plasma using SiH_4 and O_2, the incorporation of OH groups depends on the ratio $R = O_2/SiH_4$. When the ratio is high, the Si is completely oxidized, H is liberated and reacts with the excess O and produces OH and ε increases. In O-deficient plasmas, i.e., low R, Si is incompletely oxidized and Si–H bonds are formed, increasing ε. At an intermediate value of R, the bonded H will be at a minimum (Figure 4.9) as will the value of ε (Figure 4.10).

Increasing the deposition temperature reduced [OH] and the tendency to absorb moisture upon exposure to a high-humidity environment (Patrick et al., 1992). Lassig et al. (1993) attributed the decrease in [OH] to thermally enhanced water desorption during deposition.

The OH-content of porous films is high and such films absorb water from the environment very readily, with a large increase in the dielectric constant. The absorption of water is reversible; heat treatment at 400°C for half an hour desorbs all the water, which is reabsorbed upon subsequent exposure. The OH content, however, is unaffected by this treatment; heating at or above ~600°C is required. Heating at 1000°C transforms deposited films so that they become indistinguishable from thermally grown SiO_2, i.e., free of H.

Stress is also affected by moisture absorption. If the initial stress is tensile, it is decreased (Blech and Cohen, 1982) and may become compressive. If the initial stress is compressive, the stress increases (Gokan et al., 1987). A change of stress upon exposure to humid environments is an indication of moisture pick-up. Another indication is stress hysteresis during thermal cycling (Bhushan et al., 1990; Cramer and Murarka, 1995).

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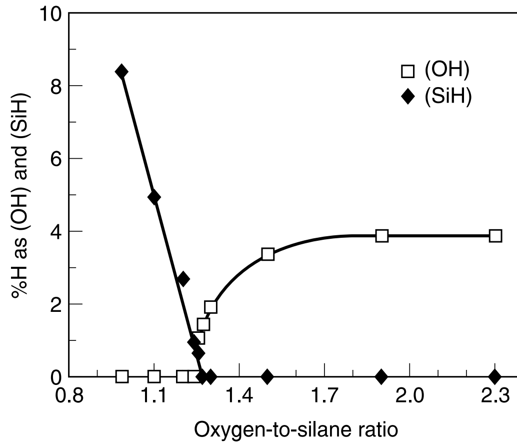

Figure 4.9 Percentage of H (as OH and SiH) in SiH_4-based ECR films vs. O_2/SiH_4 ratio in feed gas. (Reproduced from Lassig, S., K. Olsen, and W. Patrick, VMIC, 1993, p. 122. With permission.)

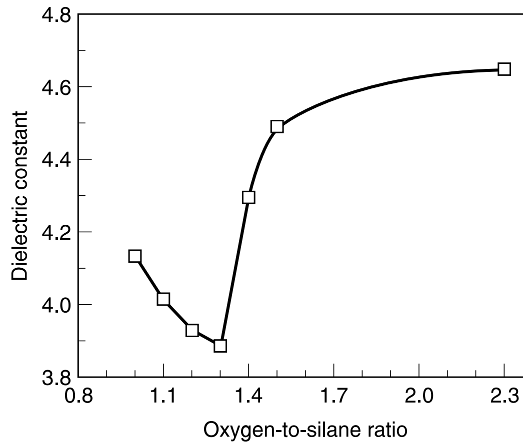

Figure 4.10 Dielectric constant of SiH_4-based ECR films vs. O_2/SiH_4 ratio in feed gas. (Reproduced from Lassig, S., K. Olsen, and W. Patrick, VMIC, 1993, p. 122. With permission.)

Some of the deleterious effects of desorption of the absorbed moisture are poisoned (i.e., high-resistance) vias, metal blistering and corrosion, device instability, etc., as well as the mechanical instability related to stress changes.

4.2.8.2 Argon

Large amounts of Ar can be incorporated into sputtered SiO_2 films (e.g., $Ar/SiO_2 \geq 0.1$); the Ar content increases with increasing substrate bias. Unlike H-incorporation, Ar does not affect the dielectric properties of the films. In fact, sputtered films with a high Ar content most closely resemble thermally grown oxide (Schwartz and Jones, 1970). The room temperature stress of sputtered films is compressive; this is thought to be a consequence of the incorporation of Ar since it does increase with bias as does the Ar content. Although annealing the films at 400°C decreased the Ar content, the stress remained unchanged.

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4.2.9 Etching of SiO_2 Films

4.2.9.1 *Wet Etching*

SiO_2 films are soluble in HF-based solutions. When used to etch masked SiO_2 films to form through-holes, the HF solution is buffered by the addition of NH_4F (BHF). In a given solution, the etch rate depends on the film quality (thermal oxide has the lowest rate). For a given oxide, the rate is determined by the ratio NH_4:HF; the rate decreases as the ratio increases. As discussed in Chapter 1, reactive plasma-assisted etching has replaced wet etching for patterning. BHF may still be used, at times, in brief clean-up steps and in place of "P" etch in evaluating deposited oxides.

4.2.9.2 *Sputter Etching*

This technique is used rarely for patterning now. However, in some processes used in fabrication multilevel device structures, *in situ* sputter etching (cleaning) is used to remove insulating films (e.g., oxides, polymers) from the surface of a metal at the bottom of a via hole, before deposition of the next metal layer (e.g., Bauer, 1994).

4.2.9.3 *Reactive Plasma-Assisted Etching*

The steps in a device fabrication process in which SiO_2 films are etched are (1) forming through holes (contacts to the Si substrate and vias connecting sequential metal levels) and (2) etchback planarization, which is discussed in another chapter.

The requirements for a successful process are adequately high rates (for throughput requirements), profile control, uniformity, reproducibility, minimal damage and contamination, and good selectivity to the mask and the substrate.

SiO_2 is etched in F-containing plasmas. Etching in a barrel reactor was the earliest application of dry processing in reactive gases, but it was realized very quickly that it could not meet the requirements of VLSI/ULSI processing. RF sputter etching of SiO_2 by fluorochlorohydrocarbon gases was reported by Hosokawa et al. (1974). RIE in capacitively coupled reactors of various designs has since been the method of choice, although the high-density plasmas are coming into use.

4.2.9.4 *Etch Mechanism*

The final volatile Si-containing product is SiF_4 and most of the O is probably desorbed as O_2 (Winters, 1983). According to Winters and Coburn (1979) F atoms (produced from XeF_2 at very low pressure) do not react spontaneously with SiO_2 but do react in the presence of ion bombardment. Flamm et al. (1979) found that F atoms (at a higher pressure) etched SiO_2 at a measurable rate (~100 Å/min at room temperature). The difference in results may be due to the difference in atom flux or in the sensitivity of detection. SiO_2 etches slowly and isotropically in a fluorinated plasma in a barrel reactor, in which ion bombardment is negligible but the pressure (reactant supply) is high.

Several experiments demonstrated that RIE of SiO_2 is dominated by an ion-driven mechanism. Schwartz et al. (1979) showed that in a low-pressure RIE system, the profile of SiO_2 etched in CF_4 was vertical beneath a nonerodible vertical mask, i.e., there was no undercut and a loading effect, due to depletion of neutral species, was small. When the effect of ion bombardment was minimized, etching became isotropic, the etch rate was reduced significantly, and the loading effect was substantial. The etch rate of SiO_2 in various Freons had a stronger dependence on the sheath voltage than on the nature or concentration of the chemical species (Fortuno, 1986; Simko and Oehrlein, 1991); the existence of a threshold voltage for RIE of SiO_2 was inherent in the etch model

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(Fortuno 1986). Therefore, in the absence of lateral mask erosion, nonundercut vertical profiles would be expected in low-pressure RIE systems, irrespective of the specific F-containing etchant.

4.2.9.5 Etch Gases

The compounds used for etching SiO_2 include CF_4 (one of most widely used in the early days of plasma etching) and other saturated and unsaturated fluorocarbons (e.g., C_2F_6, C_3F_8, C_2F_4), hydrofluorocarbons (e.g., CHF_3), as well as SF_6, NF_3, and chlorofluorocarbons (CF_xCl_{4-x}). These gases are often used as mixtures with the reactive gases O_2 or H_2; inert diluents, such as Ar or He, are sometimes added.

The chlorofluorocarbons (CFCs) are ozone-depleting gases and there is international agreement to phase out production of them.

The perfluorocompounds (PFCs), the fully fluorinated compounds such as CF_4, C_2F_6, and C_3F_8, as well as CHF_3, SF_6, and NF_3, used to clean etch chambers as well as etch the dielectric films, contribute substantially to global warming, i.e., have high global warming potentials (GWP_{100} values for a 100 year integrated time horizon, *relative to* CO_2) because of their high infrared absorbencies and, in some cases, long atmospheric lifetimes. Another indication of the effect of a gas on warming is its measured radiative forcing, the relative effectiveness of greenhouse gases to restrict long-wavelength radiation from escaping into space. The values of these factors for the compounds listed above (Raoux et al., 1999) are shown in Table 4.5. The choice of many of these compounds has been dictated by their ease of handling and their ability to etch anisotropically and selectively.

Another estimate of the environmental impact of a process is given by the metric known as MMTCE (million metric tons of carbon equivalent):

$$\mathrm{MMTCE} = (\textstyle\sum_i Q_i \times 12/44 \times \mathrm{GWP}_{100})/10^9$$

where Q_i is the mass of emitted gas i in kg.

Mohindra et al. (1994) suggested and demonstrated the use of the shorter lifetime PFC alternatives such as the hydrofluorocarbons (HFCs), C_2F_5H, $C_2F_4H_2$, although, as stated above, CHF_3 is an exception. Although CF_3–CFH–CF_3 has a higher GWP_{100} value than the iodofluorocarbons discussed below, it is about a quarter of that of CHF_3. Karecki et al. (1998a, 2000) used this compound in preliminary studies in an HD plasma reactor. The etch rate was ~3/4 of that in C_3F_8, selectivity to resist was good, and the etch profile was vertical. A high degree of polymer deposition inside the etched features, however, led to an etch-stop problem.

Emission controls are now required for the PFCs, CHF_3, SF_6, and NF_3 (Mocella, 1996).

Iodofluorocarbon compounds (IFCs), such as iodofluoromethane (CF_3I), 1-iodoheptafluoropropane (CF_2I–CF_2–CF3), and 2-iodoheptafluoropropane (CF_3–CFI–CF_3), have low (< 1) or negligible GWP_{100} values. They have been evaluated as etchants for dielectric films in both RIE (Fracassi and d'Agistino, 1998) and high-density plasma systems (Karecki et al., 1998a,b, 2001a,b).

Table 4.5 Environmental Factors for a Variety of Gases

Gas	Lifetime (yr)	Radiative forcing	GWP_{100}
CO_2	100	0.000018	1
CF_4	50,000	0.10	6500
C_2F_6	10,000	0.23	9200
C_3F_8	7000	0.24	7000
SF_7	3200	0.64	23,900
NF_3	740	0.21	8000
CHF_3	250	0.18	11,700

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The RIE etch rates in CF_3I were similar to those in CF_4 and CF_4/CHF_3 mixtures and a thicker polymer layer was formed on Si than in CF_4. It was pointed out that C_2F_6 generation is probably the main drawback to the use of CF_3I.

In an inductively coupled high-density plasma, CF_3I was unacceptable since it was nonselective to resist. Etch rates in the other IFC compounds were comparable to that obtained in a C_3F_8-based process. Although the polymer-forming tendency was greater than that of C_3F_8 (lower F:C ratio), it was insufficient to offset the physical component of the etch, i.e., bombardment of the surface by energetic, massive iodine ions. On the sidewalls and feature corners, which receive less energetic bombardment due to shadowing and charging effects, polymer deposition was heavier, often resulting in tapered profiles under high-selectivity conditions. Nearly vertical sidewalls could be obtained but then mask and stop layer selectivity was limited.

Instead of changing etchants and modifying etch processes, the use of "a high density plasma to fragment the effluent gases and to add gases such as O_2 to form products which have low GWPs" has been suggested (Liao et al., 1999). Trifluoroacetic anhydride (TFAA) + O_2, used for chamber cleaning after PECVD of dielectric films, reduced MMTCE by a factor of 8 with a slightly longer clean time than an optimized PFC process and almost 100% destruction of the source. TFAA was observed in the plasma (Pruette et al., 1998). A plasma-induced reaction of CF_4 and C_2F_6 with an excess of CaO destroyed > 70% of CF_4 and > 80% of C_2F_6 forming CaF_2 (environmentally benign) and releasing CO and CO_2 (Delattre et al., 1999). A remote microwave cleaning technology to dissociate 99.9% of the NF_3 used for cleaning PECVD chambers was described by Raoux et al. (1999). Perfluorinated ether (C_4F_8O) was found to be an effective chamber cleaning compound and reduced global warming emissions significantly (Pruette et al., 2000). The abatement of the process effluents, however, may require costly installation and equipment maintenance (Pruette et al., 2000).

4.2.9.6 Selectivity

Unlike O_2 additions, addition of H_2 to CF_4 reduces the F atom concentration markedly. Thus, as expected, the etch rate of Si is reduced significantly; at some concentration of H_2 in the feed gas, the Si etch rate goes to zero. In his paper (1975) and a patent issued later (1976) Heinecke was the first to demonstrate that this gas mixture, as well as fluorine-deficient CF compounds, e.g., C_3F_8, could be used to obtain selectivity of SiO_2 over Si in plasma etching. He also showed that polymer formation would occur under some conditions. Ephrath (1979) extended the work (on CF_4/H_2 mixtures) to (capacitively coupled) RIE systems. Polymer surfaces are affected in much the same way as Si surfaces. Reduction of the etch rate of Si by the addition of H_2 is the result of two processes: reduction of the F-concentration due to scavenging by H_2 (e.g., Doh et al., 1996) and deposition on the Si surface of a C-containing material (a fluoropolymer) blocking access of the etchant. The H_2 concentration at which the etch rate of Si in CF_4/H_2 went to zero was called the "polymer point" since a visible film was detected on the Si surface (Ephrath and Petrillo, 1982). The effectiveness of using polymer-forming etchants was enhanced by the use of Si-coated electrodes which scavenge F. The etch rate of SiO_2 is affected only slightly in the same range of H_2 concentration, probably because the liberation of O removes any adsorbed blocking layer. Only at very high concentrations of H_2 does the etch rate of SiO_2 decrease significantly. Good selectivity, i.e., a high etch rate ratio (ERR) = ER_{SiO_2}/ER_{Si}, is essential for etching contact holes in SiO_2 to the Si substrate, particularly as the junction depths become smaller. It should be emphasized that not only a high ERR but a low absolute etch rate of Si is needed for a successful process (Jacob, 1976). Coburn (1982) has described a boundary between etching of Si and polymerization on the Si surface (on which SiO_2/Si selectivity depends) in terms of the F/C ratio and substrate bias for various CF compounds, showing how the chemical composition of the reactant gas, addition of O_2, H_2, and loading affect that boundary. Selectivity to photoresist, to prevent loss or distortion of the mask, and to Si_3N_4, used as etch-stop layers in several processes now used in IC fabrication, is equally important and follows

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the similar trends as does selectivity to Si. In addition to the choice of etchant, other system variables such as total flow, total pressure, residence time, RF power, sheath voltage, wafer temperature, and reactor configuration have a strong influence on polymer formation and on selectivity.

Oehrlein et al. (1994a) pointed out that in the low-density capacitively coupled RF discharges deposition of polymer is due to neutral species. In addition, as soon as the discharge is ignited the wafer is bombarded with energetic ions. Thus, a polymer film is *not* accumulated on SiO_2 surfaces in CF_4 plasmas.

Oehrlein et al. (starting in 1994 and in a series of subsequent papers with colleagues) initially used an ECR reactor with CF_4 and CHF_3 as etchants. In a high-density reactor, the formation of radicals and ions is more efficient than in a capacitively coupled reactor. In the absence of adequate RF bias at the substrate, the wafer is bombarded with low-energy ions (equal to the plasma potential) which, together with the neutral species, were found to be essential for growth of a fluorocarbon polymer film. Thus, in CF_4 in an ECR plasma, a film can form on SiO_2 as well as on Si, etc. (Oehrlein et al., 1994a). With low substrate bias (above an apparent threshold energy), oxide etching will occur but is inhibited by the presence of the fluorocarbon film. This range of etch rates was called the "fluorocarbon etch suppression regime" (Oehrlein et al., 1994b). At high substrate bias there was no polymer film on the oxide surface. This is the oxide reactive (or chemical) sputtering regime, in which the etch rate increases linearly with the ion current and the square root of the ion energy. The fluorocarbon film on a Si surface was thicker in CHF_3 than in CF_4 which translates into a lower etch rate of Si, and a higher selectivity in CHF_3 than in CF_4.

Etching in RFI reactors produced results similar to those obtained in ECRs using CF_4 and CHF_3, although in the RFI reactors mixtures of H_2 with CHF_3, C_2F_4, and C_3F_6 were used (Bell et al., 1994; Rueger et al., 1997, 1999). It was noted that high-density plasmas had an enormous polymerizing ability. As the RF bias was increased in the suppression regime, the F-content of the layer decreased, leaving a C-rich highly crosslinked monolayer. It was postulated that energy dissipation in the overlying layer decreased the etch rate of SiO_2 below that expected for reactive sputtering. The formation and etching of the fluoropolymer film, i.e., its thickness, governs etch selectivity since etching of Si in a fluorocarbon plasma involves diffusion of the reactant and product species through it. According to Bell et al. (1994) the best condition for suppressing the Si etch rate was in an intermediate pressure regime, in which there is a balance between a F-deficient thicker protecting layer and a lower ion flux to reduce the ion-enhanced diffusion of F through the film, but not so low as to reduce the etch rate of SiO_2. Rueger et al. (1999) concluded that high selectivity depends on the defluorination of the steady-state fluorocarbon film on Si while maintaining a high ion current to the wafer.

Standaert et al. (1998) proposed a model in which the etch rate of Si is controlled by a neutral etchant flux though the overlying fluorocarbon layer since the contribution of direct ion impact is reduced as it thickens; the ion energy, however, was an important factor in etching Si. They assumed that one of the roles of ions on the etching process was an enhancement in the diffusivity of F atoms through the layer and in the reaction probability of F in the fluorocarbon film, with the F originating in the plasma. The second role included ion fragmentation and dissociation of the fluorocarbon surface molecules.

Schaepkens et al. (1999) compared the SiO_2 to Si_3N_4 etch selectivity with that of SiO_2 to Si in ICP plasmas using CHF_3, C_2F_6/C_3F_6, and C_3F_6/H_2. They reported that, in general, the etch rates of all three substrate were inversely proportional to the thickness of the fluoropolymer film. The film on SiO_2 was sufficiently thin so that at a high substrate bias the etch rate did not depend on the etchant. The thickness of the fluorocarbon films on Si_3N_4 was intermediate between that on Si and SiO_2. The thinner films on SiO_2 and Si_3N_4 are due to their ability to form volatile species with C (COF_2, CO_2, CO, CNF, FCN); there are no volatile Si–C species. They stated that "the difference in the fluorocarbon consumption between SiO_2 and Si_3N_4 is possibly due to differences in bond strength, substrate stoichiometry, and volatility of the reaction products, etc." They also found a

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fluorinated oxide or nitride reaction layer between the substrate and fluorocarbon film. The thickness of the reaction layer decreased as that of the fluorocarbon layer increased as might be expected since the fluorocarbon layer inhibits etching.

Tatsumi et al. (2000) and Matsui et al. (2001a,b) used a dual-frequency reactor and $CF_4F_8/Ar/O_2$ as etchants. They found that the steady-state thickness of the polymer layer on SiO_2 was related to the F atom flux which, in turn, depended on the incident C–F reactive species and the reaction probability (s). The value of s was a function of the net ion energy, which is the difference between the incident ion energy and that lost in the polymer layer. A thick polymer layer reduced the etch rate of SiO_2. In a highly selective process, the fluorocarbon layer on SiO_2 was very thin (< 1 nm); on Si and Si_3N_4 it was much thicker (~5 to 6 nm). They also found a reaction layer (possibly the intermediate product of etching Si and Si_3N_4) at the interface between the fluorocarbon film and the Si and Si_3N_4 surfaces. They postulated that the films on Si and Si_3N_4 were thicker than the ion projection range whereas there was no energy loss as the ions penetrated the thin film on SiO_2. At high ion energies, the reaction layer was thicker and the fluorocarbon layer thinner; Si and Si_3N_4 etched rapidly and selectivity was degraded.

Standaert et al. (2004) found that, although the steady-state thickness of the polymer film was approximately constant at high values of the self-bias voltage, the etch rates increased markedly with increasing bias. Thus they concluded that the ion energy, as well as the polymer thickness, was important in etching the substrates. They also reported that at low values of the substrate bias $ER_{SiO2} > ER_{SiN}$ but at higher voltages $ER_{SiN} > ER_{SiO2}$, although the thickness of the polymer film on SiN always was greater on the SiN surface than on the oxide surface.

Despite the almost universal characterization of the fluorocarbon film as an etch inhibitor, Standaert et al. (2004) stated that “fluorocarbon film is not necessarily inhibiting the etch rate. As a matter of fact, ion-induced defluorination of the fluorocarbon film can be the main source of fluorine used for etching of the substrate.”

Increasing the temperature of the wafer resulted in a decrease in the rate of deposition of the fluorocarbon film so that etch rates increased. The etch rate of photoresist increased faster than that of SiO_2 so that the selectivity was degraded (Perry et al., 2001). Etching to the insulator/metal interface is discussed in Section 4.2.9.8.

4.2.9.7 Profile Tailoring

If vertical interconnects (studs/plugs) are not used, it is advisable to round the tops of the holes or taper the sides, to improve step coverage by the subsequent metal layer. The shape of an etched feature can be controlled by shaping the resist mask during the lithographic processing by various protocols of reflow baking (Huang et al., 1984; Saia and Gorowitz, 1985) or low-dose flood exposure of the resist after the soft-bake step, before exposing the pattern (White and Meyerhofer, 1987). The shape can also be modified, during etching, by controlled mask erosion, selecting a suitable resist to oxide etch rate ratio, or changing the ratio during oxide etching. The change in ratio is accomplished by adding O_2 to the etchant, among which have been CF_4, CHF_3, C_2F_6, SF_6, and NF_3 (Viswanathan, 1979; Bondur and Frieser, 1981; Duffy et al., 1983; Light and Bell, 1983; Peccoud et al., 1984; Castellano, 1984; Saia and Gorowitz, 1985; Bogle-Rohwer et al., 1985; Kudoh et al., 1986; Jillie et al., 1987). Nagy (1984), by ion etching, propagated a facet formed in the resist mask (due to the angular dependence of ion etching) to the mask/oxide interface; this results in replicating the facet in the oxide. In another technique, the RF power was pulsed and it was possible to etch the resist isotropically and the oxide anisotropically (Giffen et al., 1989). An optimized slope multi-tier contact etch process was developed for a batch reactor (Mautz et al., 1994). It combined an initial anisotropic oxide etch with sequential steps of photoresist removal and oxide etching.

The use of a cantilevered mask produced controlled taper of the via independently of the mask profile. The thickness of the organic layer beneath the overhanging nonerodible mask (which

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controls the via size) determines the taper (Rothman et al., 1981). Changing the ratio of etch gases, CHF_3 and CF_4, in a high-pressure reactor tapered the slope independently of the resist shape (Chen and Mathad, 1987). By lowering the substrate temperature to about –50°C, Ohiwa et al. (1992) were able to etch tapered holes in SiO_2 at high rates using CHF_3; the results were explained by fluorocarbon polymer effects. A triode reactor was used to taper oxide profiles by controlled resist erosion and splitting the power between the top and bottom electrodes (Bogle-Rohwer et al., 1985). It was also used to perform an iso-anisotropic etch process. In this latter process, the isotropic etch of the oxide, with no resist erosion, was carried out in a downstream mode in which the RF power was fed to the side electrode; the anisotropic etch was a standard RIE process (Giffen et al., 1989). Still another approach which is decoupled from the mask shape was to reshape vertical holes in SiO_2, taking advantage of the incident ion angle dependency of etching of oxygen ions in an ECR etcher to facet the hole edges (Hashimoto et al., 1990).

4.2.9.8 Through-Hole Etching

4.2.9.8.1 Contact Holes

Etching contact holes in SiO_2 requires the proper profile and high selectivity to Si or a silicide (as well as the mask) or else the use of an etch-stop layer. The high aspect ratio and the variable insulator thickness make contact hole etching a challenging process.

4.2.9.8.2 Via Holes

In etching via holes, originally the ratio of the etch rates of the various etchants to that of the photoresist mask (the selectivity) was the important factor for ensuring adequate protection during etching as well as for profile tailoring. The underlying metal films were Al, W, TiW, TiN, Ta, etc. In the case of Al, after exposure to a CF_4 plasma, a thin fluorinated film was detected on its surface by RBS (Chu and Schwartz, 1976). Since Al cannot be reactive ion etched in a fluorinated plasma (AlF_3 is involatile), it is merely sputter etched slowly. The other underlying metals mentioned can be reactive ion etched in these plasmas, but any loss can be accommodated during the deposition of a vertical interconnect, if it is used, or the next interconnection-level metal. Since via holes are often sputter cleaned using Ar or reactive gases, the effect of overetch was not important in this respect.

More recently, as the size of via holes has been reduced substantially, sputtering of the underlying metal has become an additional concern. Redeposition of the metal on the walls of the via may not be uniform (surface roughening) and may reduce their size, making subsequent processing even more difficult. Two patents (Arleo et al., 1993; Rhoades et al., 1993) described the addition of N_2 or a N-containing gas to F-based etchants to suppress redeposition by sputtering of the underlying conducting film. Rhoades et al. (1993) postulated that the action of N_2 is to form a volatile compound, such as AlN or TiN, instead of involatile AlF_3 or an organometallic polymer which would be sputtered and redeposited. Control of sputtering (and microloading) was also achieved in an ECR reactor by increasing the flow rate of C_4F_8 in a mixture of C_4F_8 and O_2. The protection was afforded by a fluoropolymer film deposited only in the bottom of the via (Hisada et al., 1994).

4.2.9.9 Feature-Size Dependence of Etch Rate

This etch-rate dependence is a major difficulty in etching SiO_2 features of different sizes in the newer ICs in which the sizes have been reduced and the aspect ratios (ARs) increased. An introduction to this topic is found in Chapter 1, Section 1.5.8.10.

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4.2.9.9.1 RIE Lag

RIE lag is one of the names given to the phenomenon in which small features etch at a slower rate than do large ones. Its effect has been observed in high-pressure plasma processes, in low-pressure batch RIE, and in low-pressure MERIE processes (Jones et al., 1990) as well as in ECR (Fujiwara, 1989; Nojiri, 1989; Joubert et al., 1994a,b,c) and RFI reactors (Joubert et al., 1997; Schaepkens et al., 2000a,b), and in a variety of etch gases. The effect is somewhat more pronounced in holes than in trenches (Joubert et al., 1994c).

Many explanations have been offered and conflicting results have been reported. Coburn and Winters (1989), using simple vacuum conductance arguments, concluded that in high AR features conductance is adequate to allow the outflow of reaction products, but can be expected to limit the flow of reactive species to the bottom of the feature, thus explaining the etch rate dependence of high AR features. Jones et al. (1990) considered possible causes for the phenomenon: (1) transport limitations in narrow gaps, (2) polymerization, (3) geometric, shadowing, (4) ion deflection by surface charges, and (5) ion scattering in the plasma. They concluded that ion scattering in the sheath is the principle mechanism, as did Lii et al. (1990). Jones et al. stated that ion-driven processes are more sensitive to RIE lag and that processes in which the sheath width is small with respect to the mean free path in the plasma will exhibit less lag. Such processes would be those using electronegative gases (e.g., SF_6), very low pressures, or low bias, and that the scattering angle could be decreased by using light nonionizing diluents such as He.

Abachev et al. (1991) developed equations for the particle flux including particle reflection and adsorption (when the mean free path was much larger than the width of the feature, i.e., width < 1 μm and pressure < 100 Pa) and concluded that limited ion and radical delivery were the main mechanisms. Fujiwara et al. (1989) and Sato et al. (1991) also concluded decreasing species concentration on the trench bottom was responsible.

Arnold and Sawin (1991) analyzed localized charging during plasma-assisted etching of a perfectly insulating surface. They assumed an isotropic electron flux and directional ion bombardment. The resultant field acts to deflect the arriving ions thereby reducing the ion flux densities (and etch rates) at the bottom of the feature and cause appreciable fluxes to the sidewall. They concluded that the skewing of the ion direction would contribute not only to RIE lag but also to feature bowing (profile modification) and microtrenching.

Davis (1991) examined the image potential between an ion and the wall of an etched feature for small, high AR features. He concluded that low-energy ions (<200 eV) are attracted to the walls resulting in loss of directionality and reduced vertical etch rates.

Gottscho et al. (1992) considered eight mechanisms which have been offered to explain ARDE: (1) Knudsen transport of neutrals, (2) ion shadowing, (3) neutral shadowing, (4) differential shadowing of insulating microstructures, (5) field curvature near conductive topography, (6) surface diffusion, (7) bulk diffusion, and (8) image force deflection. They concluded that only the first four are consistent with AR scaling. "There may be many causes for ARDE; these may be reduced to neutral and ion transport phenomena which in turn are affected by gas phase collisions, surface scattering, and surface charging."

Sato et al. (1991) also observed a larger effect when etching Si with F-containing gas than with Cl-containing gases, which they attributed to enhanced ion-assisted etching with the heavier halogen, which runs counter to the argument of Jones et al. (1990) that ion-dominated etching processes are more susceptible to RIE lag. Both Fujiwara et al. (1989) and Nojiri et al. (1989) report that at very low pressures, in an ECR reactor, the effect is no longer observed, although other investigators have found this not to be true.

A model of RIE lag, based on polymer deposition while etching SiO_2 in selective (to Si) gases, was proposed by Joubert et al. (1994a,b,c). They correlated RIE lag in an ECR reactor (at 1 mtorr) with the deposition rate of fluorocarbon films on unbiased blanket SiO_2 samples, so that RIE lag

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problems are greatest when highly polymerizing etchants are used. Their model assumed that the net oxide etch rate on a blanket wafer holds for oxide etching at the bottom of a feature. It included (1) ion scattering which reduces the density and energy of ions at the bottom of a high AR trench or hole, which (2) causes oxide etching to move from a regime in which the oxide is etched to one in which a thin fluorocarbon polymer can grow on the oxide surface, thereby slowing its etch rate. Thus, if the reduction of the energy flux results in the deposition of a thick polymer layer on the oxide, etching may stop entirely as the AR (particularly in a hole) increases. The etch-stop phenomenon was observed with all the etchants used (CHF_3, C_3F_6, C_2F_4, and $C_2F_4 + H_2$) but the more polymerizing the gas, the smaller the AR value at which etching stopped. They also concluded that RIE lag may be reduced by operating at high RF voltages (power), but this may result in the loss of the resist mask.

Westerheim et al. (1995), using C_2F_6 in an ICP plasma, found that RIE lag was observed at high bias power, but reverse lag at low bias power. This is not consistent with Joubert who had suggested that high bias might reduce lag. They suggested that polymer deposition was controlled by both the flux of deposition precursors and ion bombardment.

Doh et al. (1997) agreed with Joubert (1994) that RIE lag (using C_4H_8/H_2 in an ECR reactor) improved with increased bias voltage and decreased pressure (in an ECR reactor); they postulated that the improvement was due to an increase in the ion energy with voltage and an increase in ion current density at reduced pressure. Increasing the bias frequency from 100 to 800 kHz, at constant bias, improved RIE lag substantially; this they attributed to a shift in the ion energy distribution toward higher energy.

Hayashi et al. (1996) measured the ion current in via holes using capillary plates (i.e., glass or Si plates with small holes) in a MERIE system with C_4F_8 + CO as the etchant) and concluded that etch rates decreased as the AR increased because of decreasing ion current. They observed etch-stop behavior in etching SiO_2 (at AR = 6) but, surprisingly, Si_3N_4 continued to etch (at a slower rate) even at AR = 30. This seems to be explained by the fact that they observed (using XPS) that the fluorocarbon film deposited on Si_3N_4 surfaces at the bottom of the hole was richer in F and more susceptible to sputtering than that deposited on large open Si_3N_4 surfaces.

In another study, using C_2F_6 in an RFI reactor, Joubert et al. (1997) also found by XPS that the fluorination of the polymer on the bottom of a contact hole increased strongly with increasing AR. Other studies had shown that ion bombardment of a fluorocarbon film reduced the F/C ratio; thus the increase in F/C is consistent with a loss of ion density and energy in high AR holes. After overetching to the underlying Si, thicker polymer films were found (by SEM) at the bottom of the higher AR holes; the films were thicker at the edges of holes than at the center.

Schaepkens et al. (2000a) studied RIE lag in an IPC reactor using CHF_3 and C_3F_6/H_2 at 6 mtorr. The etch time was relatively short in order to keep the AR constant. The thickness of the polymer film deposited on the SiO_2 at the bottom of the holes was measured using an SEM. For the same process conditions, the polymer film was thicker in C_3F_6/H_2 than in CHF_3 and the transition from deposition to etching required a higher self-bias voltage. For both feed gases, the rate of polymer deposition at zero bias decreased as the AR was increased. A possible explanation is that breadloafing of the fluorocarbon film at the mouth of the feature inhibited access of the isotropic neutral flux (and low-energy ions) needed for polymer growth (Standaert, 2005). Although the rate of polymer deposition decreased as the AR increased for both feed gases, for AR < 2 there was a slight reduction in the etch rate of SiO_2 (at high bias). In CHF_3, for AR greater than about 2, there was *no* fluorocarbon deposition on the feature bottom but the etch rate of SiO_2 (at high bias) decreased markedly as AR increased. Similar results were reported for lag in the C_3F_6/H_2 plasma. In this plasma, however, polymer deposition at zero bias persisted to higher values of AR, although none was observed at the voltages used in practical etching processes (greater than about 50 V). These oxide etching results appear to be at odds with the assumption that the net accumulation of polymer at the bottom of the oxide feature impedes etching at high bias. Since oxide etching is

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considered to rely on direct ion impact, RIE lag can be explained by the loss of ion density/energy and differential charging in the high AR features. A slight dependence on feature diameter (as well as AR) was observed; this was said to be consistent with differential charging.

Since thick resists exaggerate the AR, finding mask materials or etch gases for which the etch rate of the mask is low, making thinner masks possible, helps to decrease the severity of the problem. Loss of neutral and ion flux and reduced ion energy at the bottom of high AR features are important contributors to RIE lag. The role of polymerization has been emphasized by some investigators and ignored by others.

4.2.9.9.2 Reverse Lag

Reverse (inverse) lag, in which small holes etch at a higher rate than large ones, has been observed in oxide etching (Dohmae et al., 1991; McVittie and Dohmae, 1992). This was attributed to reflection of ions off the sidewalls, which depended on the wall angle and ion energy, with reflection effects increasing at lower energies. When reflection was suppressed by using an overhang structure, standard lag resulted. Fang et al. (1996), however, attributed reverse lag in a high-density reactor using C_3F_8 to reduced polymer deposition at the smaller via holes and enhanced deposition on large areas. Doemling et al. (1996) also concluded that the inverse lag using CHF_3 in an ICP reactor was due to the reduction in neutral flux to the bottom of the feature, i.e., reduced polymerization. They also stated that regular RIE lag will be observed for high ion/neutral ratios and/or high ARs and inverse RIE lag for smaller ion/neutral ratios and/or smaller ARs.

Schaepkens et al. (2000b) observed reverse lag when the duty cycle of a pulsed RF bias supply in an ICP reactor was decreased. This is consistent with polymer deposition, which is highest on larger features (see above), during the long off period.

4.2.9.9.3 AR-Independent Etching (ARIE)

The existence of ARIE etching has been considered. Bailey and Gottscho (1995) concluded that it was possible to achieve ARIE over a restricted range of ARs, *but* it required a delicate balance between ion, etchant, and inhibitor fluxes. They suggested that to minimize ARDE one should operate a high-density plasma at low pressures and high neutral flow rates but, as Gottscho et al. (1992) stated, other factors besides pressure are altered when the reactor geometry is changed, so that pressure reduction alone may not be adequate to account for the improvement.

Hwang and Giapis (1997) concluded, from computer simulations, that etch rate scaling with AR breaks down when there are significant surface discharge currents. Under conditions of ion-limited etching and no inhibitor deposition the etch depth depends on the maximum incident ion energy, reaction threshold, and surface discharge threshold, irrespective of the trench width (≤ 0.5 μm). They predicted that ARIE to a depth of 2.3 μm can be attained in a CHF_3 plasma, making possible an increase to an AR > 10 before etching stops.

4.2.9.9.4 Conclusions

The lower etch rate of the smaller features (RIE lag) results in overetching the larger features on a wafer. This may result in microtrenches, enhanced etching of the substrate adjacent to the sidewalls. At higher bias powers (which may improve RIE lag) sidewalls became more vertical but microtrenching depths increased. Microtrenching decreased with decreasing trench width, but this could be due to the overlap of the trenches from the sidewalls in smaller features. Increasing the frequency of the bias voltage from 1.3 to 10.5 MHz reduced microtrenching significantly and increased the etch rate ratio of SiO_2 to resist.

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Decreasing the duty cycle of the pulsed RF bias voltage reduced the sidewall angle and critical dimensions. The presence of a thick polymer layer in a contact hole when etching stops may prevent microtrenching in the Si substrate. The changes in sidewall slope were said to be the result of a cooperative mechanism of deposition from the plasma and redeposition of etch products. The trenching was attributed to specular ion reflection from sidewalls. Since the bias power that results in high etch rates and vertical sidewalls produces the most microtrenching, high etch selectivity to underlying layers is most important (Westheimer et al., 1995; Schaepkens et al., 2000b).

4.2.9.10 Angular Dependence of RIE Rates

This subject was introduced in Chapter 1 (Section 1.5.10) and continues here with emphasis on dielectric films.

Mayer et al. (1981), in RIBE of SiO_2 using CF_x^+, reported that at low energies the etch yield had a cosine-like dependence on angle but reverted to a sputtering-like behavior at higher energies. Barkland and Blom (1993), using RIBE, showed that the angular dependence of the etch rate of Si_3N_4 in CHF_3 ($+O_2$) exhibited a maximum at about 60° and depended chiefly on the simultaneous formation and etching of a polymer layer (since it is known that a thick fluorocarbon film forms on Si_3N_4 in polymerizing plasmas), and on the ion-enhanced etching of Si_3N_4, and that these have different angular dependences. Under the same conditions the etch rate of SiO_2 followed a cosine-like curve as did that of Si_3N_4 when no polymer deposition was possible, i.e., when etched in XeF_2 + Ar. Figure 4.11 contrasts the angular dependences of oxide and nitride films etched in a polymerizing plasma. It shows that, although at normal incidence the etch rate ratio $ER_{SiO_2}/ER_{Si_3N_4}$ is substantial, at angles greater than about 55° the etch rate of the nitride approaches that of the oxides, so the ratio approaches one and selectivity is lost. The etch rate of a polymer (formed from a CHF_3 discharge) showed the same maximum at ~60° in both Ar and $CHF_3 + O_2$. Adding more O_2 to the etch mixture (thereby decreasing the net polymer thickness) increased the etch rate of Si_3N_4 at normal incidence, shifted the maximum to lower angles, and decreased its height. The XPS spectrum of an Si_3N_4 surface etched at 0° showed distinct CF_x ($x = 1, 2, 3$) and C–CF_x peaks, whereas the CF_x peaks were almost absent from the spectrum of the surface that was etched at a 60° angle, indicating very small amounts of material on that surface.

Schaepkens et al. (1998) investigated the etch rate ratio $ER_{SiO_2}/ER_{Si_3N_4}$ of films deposited on 54.7° V-groove samples formed by the anisotropic wet etch of Si. The samples were etched in an ICP reactor in CHF_3 and C_3F_6. In both plasmas, the rates of polymer deposition were lower on the inclined surface than on the flat surface and the etch rates were higher, resulting in smaller net

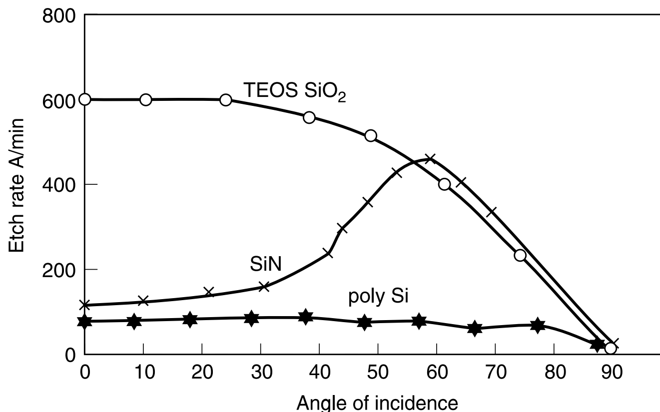

Figure 4.11 Etch rate vs. angle of incidence: ion beam, CHF_3/O_2 etchant. (Adapted from Barklund, A.M. and H.-O. Blom, *J. Vac. Sci. Technol.*, A11, 1226, 1993.)

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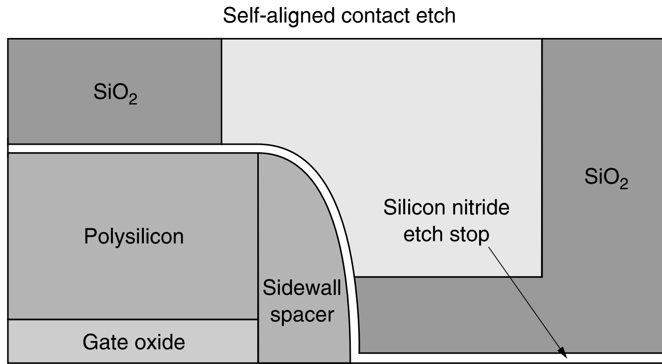

Figure 4.12 Self-aligned contact etch. (Reproduced from Singer, p., *Semiconductor International*, Vol. 20, No. 6, p. 109, June 1997. With permission.)

polymer thickness. SiO_2 etched more slowly on the inclined than on the flat surface in both etchants, as did Si_3N_4 in the less polymerizing CHF_3 plasma (cosine-like dependence, chemical sputtering). The etch rates of the oxide and nitride in CHF_3 were about equal on both surfaces, i.e., there was no selectivity. In C_3F_6, Si_3N_4 etched more slowly than SiO_2 on the flat surface (selective etching) but on the inclined surface it etched more rapidly. Due to this reversal, SiO_2 etch selectivity is no longer maintained at corners and inclined surfaces so that, for example, in self-aligned contacts (Figure 4.12) the oxide spacer is exposed and ultimately etched away.

These results, the dependence on polymer accumulation and the loss of selectivity on angled surfaces, were similar to those of Barklund and Blom (1993).

Cho et al. (2000) measured the etch rate of SiO_2 as a function of angle in a CF_4 plasma using a Faraday cage in a TCP reactor. The normalized etch rates (at several bias voltages) followed a cosine-like dependence. The normalized yield Y is given by

$$Y(\theta) = R(\theta)/\Gamma\cos\theta$$

where $R(\theta)$ = rate at θ and Γ = ion flux normal to the cathode, and Y exhibited a weak maximum between 45° and 75°.

This deviation from the cosine-like dependence was attributed to a thin fluorocarbon film on the surface. Cho et al. posited that maxima at high angles were due not to yield enhancement but to yield suppression by a very thin polymer film (a few monolayers) at low angles with the thickness reduced to a submonolayer at the higher angles. They also mentioned physical sputtering as a contributor to the positive deviation from a cosine curve.

Lee et al. (2002) extended the work of Cho et al. (2000) to a CHF_3 plasma. They found that at low bias ($\leq$200 V), the etch rate followed a cosine curve for all substrate angles. At high bias, however, the rates were higher than those given by the cosine curve for angles ~30° to 70°; above ~70° the rates dropped rapidly and net film deposition occurred on the nearly vertical surfaces. This was attributed to the fact that there is very little etching of high angle surfaces but emission of C_xF_y species from the bottom of the features increased in this high ion energy regime.

The etch rate of HOSP (a spin-on low dielectric constant polymer film containing C, H, O, Si; see Section 4.4.6.3) was compared with that of SiO_2 in CF_4 and CHF_3 in an ICP etcher (with a Faraday cage). The etch rate of HOSP was higher than that of SiO_2 in both plasmas. The rates of both films in CHF_3 decreased with increasing angle, due to the cosine dependence of the incoming flux and there was a net gain in thickness at higher angles (> 85°) and bias voltage due to redeposition of particles emitted from the bottom surface of the substrate. The normalized etch rate, $ER(\theta)/ER(0°)$, of SiO_2 in CHF_3 followed a cosine dependence at low bias but an over-cosine tendency at the higher bias, whereas that of HOSP was over-cosine at both biases. The deviation

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was larger for the higher bias. Over-cosine behavior was attributed to physical sputtering and the difference between SiO_2 and HOSP at low bias to differences in porosity and hardness. At high angles ($>70°$) redeposition distorted the angular dependency and under-cosine behavior was observed. The dependence of the normalized rate on angle for SiO_2 in CF_4 was similar to that in CHF_3 but for HOSP the deviation from a cosine curve was greater than in CHF_3 and was the same for both bias values. HOSP continued to etch at 90°, despite the absence of energetic ion bombardment, indicating isotropic chemical etching due, it was postulated, to reaction with F radicals which also suppressed redeposition (Hwang et al., 2003). It is difficult to reconcile the large over-cosine behavior (sputtering) with the enhanced chemical etching by F radicals.

4.2.10 Silicon Nitride

Although the high dielectric constant of silicon nitride (~7) excludes its use as an interlevel dielectric layer, it is included here because of its other uses in semiconductor devices. It provides good protection against Na and Cu ion migration through other dielectric films (SiO_2, low-ε materials) and against moisture penetration. Thus it is often used as a protective layer over devices to prevent instability. It has been used as a mask for selective oxidation of Si. Currently important uses are as an etch-stop layer in polymerizing fluorocarbon etchants and as hard masks for etching low-ε films in dual damascene processes, described more fully in Chapter 6.

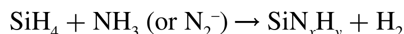
A limited thickness of the compound can be formed by thermal nitridation of silicon at high temperatures (e.g., Ito et al., 1980; Nemetz and Tressler, 1983; Delfino et al., 1992, and references therein).

CVD at high temperature is the method used most commonly for the preparation of stoichiometric films containing little or no H. The high temperature required makes CVD films unsuitable as interlevel dielectrics other than with refractory metals. Its use is limited to coating gate electrodes and contacts in Si devices and as an etch stop in self-aligned contacts. Milek (1971, 1972) has reviewed the early work on the use of silicon nitride for microelectronic applications.

PECVD has replaced CVD because it is carried out at temperatures suitable for use with Al- or Cu-based metallization. PECVD produces films of acceptable quality for device applications, and used in applications when its high dielectric constant is unimportant. Thick films can be crack resistant. In addition, they exhibit good step coverage and adhesion to Al.

PECVD nitride was first reported by Sterling and Swann (1965) who prepared it from SiH_4 and NH_3 in a tubular reactor. It became a commercially viable material when the radial flow reactor of Reinberg was introduced in 1973. It has since been deposited in a wide variety of systems, among them the capacitively coupled, dual-frequency and, now, high-density reactors.

The deposition reaction is



$$SiH_4 + NH_3\ (\text{or } N_2^-) \rightarrow SiN_xH_y + H_2$$

Although stoichiometric (Si_3N_4) films have been deposited, PECVD films are most often Si-rich. Nitrogen-rich films have also been prepared. PECVD nitrides have been referred to as "plasma SiN," but, as shown above, are better characterized as SiN_xH_y to emphasize the nonstoichiometry, when it exists and, more important, the fact that they usually contain a sizeable amount of H; stable films with a H-content as high as 40 at% have been deposited. The deposition rate, stoichiometry (Si/N ratio), H content, and bonding (Si–H, N–H), as well as the chemical (e.g., etchability in HF-based solutions) and physical (e.g., stress, density, refractive index, coefficient of thermal expansion (CTE), electrical properties) characteristics of the film depend on the precursors (e.g., NH_3, N_2, mixtures), deposition conditions (e.g., RF power, temperature, pressure, excitation frequency, electrode spacing, substrate bias), and reactor configuration. There are so many important variables that correlation among the reported results is often impossible.

SiN films have been made with either compressive (C) or tensile (T) stress. As the deposition or anneal temperature is raised, the films become tensile, the H-content and etch rate in HF-based

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solution lower, and the density higher. Deposition at lower temperature or using low-frequency (high-energy) ion bombardment produces films having a compressive stress, although the lower total H-content is decreased. According to Martin et al. (1988) and Pearce et al. (1992) the Si–H content decreased significantly while that of N–H increased slightly as the low-frequency power density increased. Pearce et al (1992) concluded that "the inclusion of $N–H_2$ structures in PECVD nitride is responsible for the compressive stress state in the film." Claasen (1987) postulated that the compressive stress in films deposited using high-energy ion bombardment/low temperature was due to implantation damage (which was not annealed out) resulting in an expansion of the deposited film. At higher temperatures, desorption of H becomes dominant and the films are densified and the stress becomes tensile.

Silicon nitride can be reactive ion etched in fluorinated plasmas. In the absence of polymerizing species (e.g., in CF_4 or CF_4/O_2) etching is neither anisotropic nor is it selective to Si or SiO_2. The RIE rates of SiN_xH_y films in a polymerizing F-based etchant decrease as films become Si-rich (Stamper and Pennington, 1993). Although the steady-state RIE rates in CF_4/H_2 of both kinds of silicon nitrides were similar, under process conditions for high selectivity of oxide to nitride, there was a longer initial etch transient for SiN_xH_y limiting the etch-stop ability for the plasma-deposited film (Lindstrom et al., 1992).

A comparative study of PECVD nitride films has been published by Kanicki and Voke (1986) and Kanicki and Wagner (1987). Other useful sources are Sinha et al. (1978), Claasen et al. (1985, 1987), Tsu et al. (1986), Hirao (1988), Landheer et al. (1991), Parsons et al. (1991), Taylor (1991), Ito et al. (1991), Kikkawa and Endo (1992), Pearce et al. (1992), Nguyen et al. (1992), Stamper and Pennington (1993), and Cottler and Chapple-Sokol (1993).

4.2.11 Silicon Oxynitride

PECVD silicon oxynitrides are used to some extent. The ratio of oxygen to nitrogen in the film determines the properties of the films; these will lie between those of the pure oxide and nitride. The ratio of the source gases will determine the ratio in the films.

4.2.12 F-Doped Plasma SiN

As in the case of SiO_2, F-doping reduces the dielectric constant of silicon nitride; values of ~ 4 to 6.5 have been reported (Fujita et al., 1984, 1985, 1988; Chang et al., 1988; Livengood and Hess, 1988). SiF_4, Si_2F_6, NF_3, and F_2 have been used as F-sources and the Si-sources have been SiH_4, SiF_4, and SiF_6. It is assumed that Si–F bonds exist, but the IR absorption band is obscured by that of Si–N (Fujita and Sasaki, 1988). The fluorinated nitrides have smaller amounts of H and greater thermal stability with respect to H-loss, and higher density, resistivity, and breakdown strength than the conventional PEVCD SiN films. Films with a very high F-content hydrolyzed to SiO_2 on exposure to moisture.

4.2.13 Boron Nitride

This discussion of BN is included here because it appears to have been the inspiration for the development of SiBN films, discussed below. B-rich BN films were reported to have a low dielectric constant, i.e., < 3, but were very unstable in moist environments. However, a review of the literature unearthed an exceptional variability of results. The value of ε ranged from 2.7 to 7.7 and there was no clue from the deposition method, conditions, or choice of precursors to account for the variation. Most recently, Nguyen et al. (1994) prepared stable films with good moisture resistance in a PECVD reactor, using diborane/NH_3 (400°C) and borazine/N_2 (300°C); ε varied from 4 to 5, depending on deposition conditions. Thus it seems clear that BN would not be likely to replace SiO_2

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as the interlevel dielectric, because of its dielectric constant. Other properties, such as its etch characteristics, i.e., anisotropic profiles with excellent selectivity over silicon oxide and nitride, or its ability to act as a polish stop in CMP may be factors influencing its use. It should be noted that some of the previous reports of a very low value of ε may have been due to measurement error. If an n-type Si substrate is used for the capacitance measurement, B may be implanted during PECVD deposition, forming a p–n junction; this causes inaccurate capacitance measurements and thus an inaccurate value of ε.

4.2.14 Films Containing Si, N, and B

The instability of BN led to the idea of SiBN films. These may be considered Si-doped BN films with better moisture resistance or B-doped SiN films with a lower dielectric constant. The films were prepared by PECVD by using mixtures of the hydrides in an Ar plasma, and by varying the ratio of the hydrides the ratio of the constituents in the films could be varied; N–H, B–H, Si–H, B–N, and Si–N were all detected in the IR spectra of the films (Maeda and Makino, 1987). Addition of B reduced ε, the refractive index, and the etch rate in HF-based etchants. However, when the dielectric constant was reduced to a value substantially lower than that of SiO_2 by increasing the B-content, the films became hygroscopic, making them unusable.

4.2.15 Films Containing Si, N, B, and O

O-doping of PECVD SiBN reduces the dielectric constant of the films still further. The films were prepared by the addition of N_2O to the mixture of the hydrides. ECR (Maeda and Arita, 1990a,b) as well as conventional PECVD (Maeda, 1990, 1993) were employed. The minimum value of 3.3 was attained when the ratio $[O]/2[Si] = 1$; increasing the O-content resulted in an increase in ε instability and susceptibility to moisture and a decrease in dielectric strength. It was postulated that the B–N groups are replaced by the more polar B–O groups at high O-doping. The reproducibility, stoichiometry control, stability, etc., of the quaternary film require further study, but no further work on this material has been reported.

4.3 SPIN-ON GLASSES (SOGs)

4.3.1 Introduction

Two types of SOGs, polysilicates and polysiloxanes, are discussed. The reactions involved in their formation are hydrolysis and condensation. The properties of the polymer and the final film are functions of the starting material, the reaction conditions, and the nature and constitution of the solvent, so that it has been possible to prepare a variety of materials with somewhat different characteristics.

There are many differences among them but they have some properties in common. After curing they are all porous to some extent. Since the dielectric constant of films decreases with increasing porosity it might be expected that the SOGs could serve as low-ε films. However, they all readily absorb moisture from the environment (Harada et al., 1990), and moisture in a film more than cancels the effect of the porosity. Moisture is easily desorbed during subsequent metal deposition, leading to the so-called "poisoned" vias and contacts (Chiang et al., 1987), blistering of Al-based wiring (Hirashita et al., 1990), and distorted metal, and poor step coverage in vias (Ting et al., 1988). These effects may be minimized or even eliminated by prolonged *in situ* heating or possibly *in situ* sputter cleaning before metal deposition (Ting et al., 1988; Wolters and Heesters, 1990). However, the continued evolution of water during sputter cleaning can negate the effect of sputter cleaning when the growth rate of Al_2O_3 (the source of the high resistance) exceeds the

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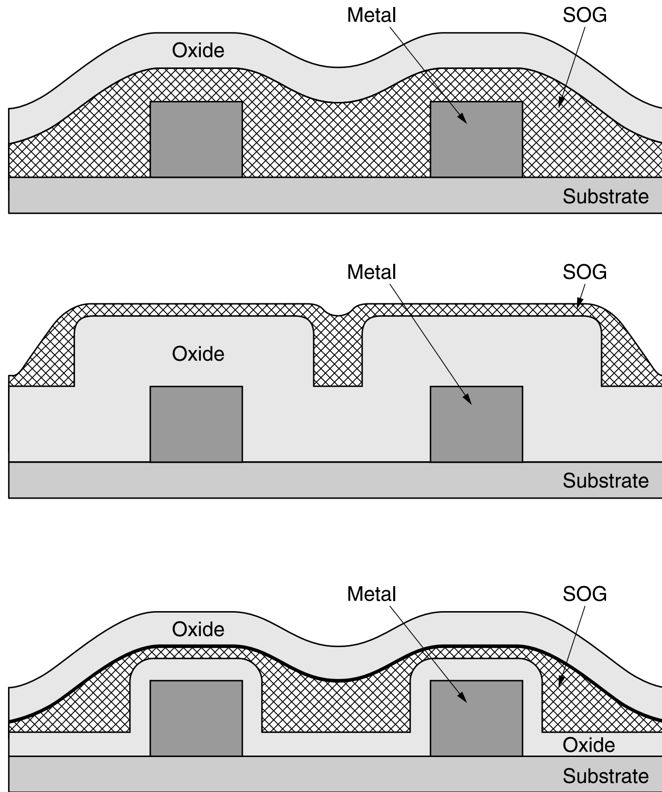

Figure 4.13 Composite structures of SiO_2 and SOG. Top: SOG in direct contact with metal; center: SOG as outer film; bottom: SOG sandwiched between two oxide layers.

sputter etch rate so that an *in situ* preheat before sputtering may be necessary. All these additional steps add to the cost. Most SOGs shrink when cured so that the film stress is tensile and thus thick films crack, limiting their applicability as interlevel dielectrics. SOGs, therefore, were rarely used alone as permanent dielectric layers but were combined with deposited stable oxide films. Several configurations for composite structures are shown in Figure 4.13.

4.3.2 Polysilicates

The starting material is an ester; TEOS is a common reactant but other esters have also been used (Smolinsky et al., 1989a). All the Si atoms in the molecule are bonded to O atoms; these, in turn, may be bonded to Si, H, or organic groups (R). Curing at ~425°C eliminates the organic groups but not the Si–OH. The structure after curing is shown in Figure 4.14.

Silanol groups in the structure increase the dielectric constant of the film. Polysilicates also have a pronounced tendency to crack with increasing thickness. Thick films can be formed by applying several thin coats, curing between successive layers, increasing the process time/cost.

4.3.3 Polysiloxanes

In these SOGs, Si atoms are bonded to C atoms as well as to O atoms; usually less than one Si is bonded to a C atom. One example is ACCUGLASS 512, prepared by the cohydrolysis of TEOS

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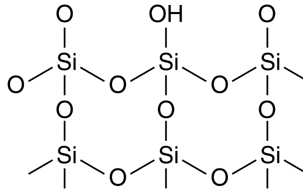

Figure 4.14 Structure of a polysilicate film after cure.

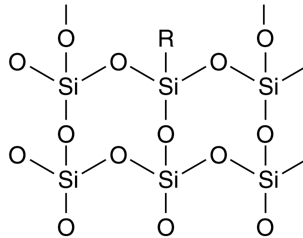

Figure 4.15 Structure of a polysiloxane film after cure.

and methyl-substituted alkoxanes (Rutherford et al., 1991). After curing at ~425°C, organic groups are still present. The generic structure of a polysiloxane after cure is shown in Figure 4.15.

The presence of the organic groups in the matrix provides greater flexibility and results in lower dielectric constant and in lower tensile stress compared with silicate SOGs, making it possible to apply thicker films without cracking. Polysiloxanes absorb/ desorb less water than the polysilicates. Nevertheless desorption of water trapped in a polysiloxane film was cited as the cause of metal blistering and void formation in Al interconnections (Hirashita et al., 1990). Outgassing of water during metal deposition results, as noted before, in high-resistance vias and contacts. The organic constituents can be oxidized easily, resulting in cracking (Harada et al., 1990). This is a serious problem since ashing is often necessary (e.g., resist stripping after via etching).

4.4 LOW DIELECTRIC CONSTANT FILMS

4.4.1 Introduction

To achieve the circuit speed now demanded of the newer chips, a low dielectric constant (ε) film is now required. Reducing ε decreases one of the contributors to the RC delay and reduces the cross talk due to capacitive coupling of adjacent metal lines.

Silicon dioxide is the ideal interlevel dielectric material. It is thermally stable, hard, tough so that it is compatible with CMP and wire bonding, resistant to organic solvents and moisture, exhibits low electrical leakage, adheres well to metals (except Cu) and itself, and has a low coefficient of thermal expansion and a low compressive stress. In addition, it is easily masked, etched, and impervious to resist strip processes. The film quality, deposition systems, and basic processes have been constantly improved over a long period of development and usage.

Despite its virtues, the high dielectric constant of SiO_2 (~4) makes it unsuitable for the newer high-speed chips. The high polarizabilty of the Si–O bond is responsible for the high dielectric constant. The tight bond between highly electronegative F and Si results in a reduced polarizability.

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Thus incorporation of F into the silica network, forming F-doped SiO_2 (Section 4.2.7) lowers its dielectric constant (to a limited extent).

Before the introduction of F-doped oxide, organic polymeric films, polyimides, were used to replace SiO_2. Films currently under investigation are those with substantially lower dielectric constants. This has been accomplished by decreasing the density of a film with a silica backbone, e.g., in silsesquioxanes in which the bond rearrangement during curing creates voids, or incorporating the light atoms C and H atoms into the structure to form, for example, SiOC:H films. Another way of reducing the density is to form a porous network as in the xerogels. Polymer films, other than polyimide, have also been studied and fluorinated polymers have the double advantage of low density and C–F bonds of low polarizability. A disadvantage of all fluorinated dielectric films is that F can be released during thermal processing, corroding metals and causing interface problems. The use of oxide–nitride barrier films and the removal of F from the surface layers have been proposed to minimize this concern.

To meet the ultimate goal of a dielectric constant < 2 pores are templated into films whose dielectric constant is ~2.5 to 3.0. A variety of low-ε films have been developed commercially; new ones appear frequently. Many are variations of the same basic film, differing in the specific organic side chains, method of preparation, etc.

The films are either spin-on dielectrics (SODs) or deposited by CVD (PECVD); the advantages of each method, e.g., cost, performance, etc., have been debated. They have a variety of names, some are nonspecific generic names (e.g., HOSP for hybrid organo siloxane polymer), some catchy but uninformative (e.g., Black Diamond, SiLK which contains no silicon, etc.).

The methods used to characterize these films are discussed in Chapter 2.

Since new films are introduced quite frequently, not all of them can be discussed in the following sections. It is not clear how many of them have been or will be incorporated into current or future devices. Unfortunately none of the newly developed materials have all the thermal, mechanical, and electrical properties of SiO_2 and therein lies the challenge of materials development and process integration.

4.4.2 Polyimides (PIs)

4.4.2.1 Introduction

As mentioned above, PIs were the first organic low-ε films to be considered seriously as replacements for SiO_2. They were chosen initially not because of their lower dielectric constant ($\varepsilon \sim 3.0$ to 3.7), but because of their ease of application (spin-on), good planarization and gap-filling properties, low defect density, and, compared with other polymeric films, superior thermal stability. Many, however, exhibited mechanical, electrical, and thermal anisotropy (e.g., Elsner et al., 1990; Herminghaus et al., 1991).

There were extensive efforts by, for example, DuPont, IBM, and Hitachi devoted to the development of various PIs as well as widespread and thorough investigation of the properties and uses of the films. They were superceded, at first, by F-doped SiO_2. The technology roadmaps predict the use of organic or porous inorganic films of significantly lower ε, some with less thermal stability but more isotropic.

4.4.2.2 Synthesis and Structure

The most common process for synthesizing PI films is by reacting nearly equivalent amounts of a diamine and a dianhydride in a suitable solvent to form the polyamic acid precursor, which is spun on the wafer and heated (cured) to carry out the imidization reaction to form PI. A schematic diagram of the reaction is shown in Figure 4.16. Thicker films are formed by spraying.

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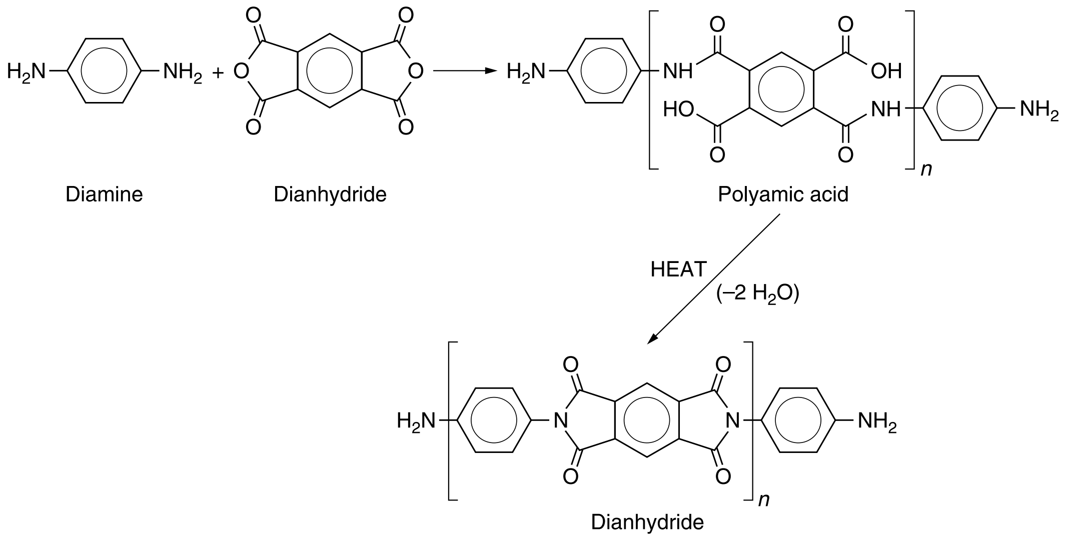

Figure 4.16 Generic sequence for forming polyimide.

Thermal conversion of polyamic acid to PI films imparts thermal stability and mechanical rigidity to the films. For a given solution viscosity (determined by the solids content and the molecular weight distribution of the polyamic acid) the spin speed determines the film thickness. The coated film is first dried at ~100°C to evaporate some of the more volatile solvents and to make the film more viscous and the substrate easier to handle. The final temperature of ~350 to 400°C is reached by ramping or in a stepwise manner. The final heat treatment removes all solvents and completes the imidization reaction. The completion of the imidization reaction has been studied by IR spectroscopy (Lee and Craig, 1980), weight loss (Numata et al., 1984), wet etch rates (Ginsburg and Susko, 1984), change in dissipation factor (see Chapter 2, Section 2.6.4), and microdielectrometry (Day and Senturia, 1984).

The polymer chain is formed by stepwise addition of monomer units, in what is referred to as a condensation process; the diamine and dianhydride form an alternating structure. Since the monomers form a chain with alternating units, the chains that are formed in the beginning of the reaction can have larger number of monomer groups and the ones that are formed toward the end of the reaction are likely to have fewer monomers (or lower molecular weight) units.

The molecular weight distribution of the chains in the precursor is controlled by the purity of the starting materials, their proportions, the reaction time and temperature, stirring, and end-cap additives used to stop the chain growth. Gel formation is a result of undesirable polymerization; gels are manifested as particulates (defects) in the finished film.

A wide variety of PIs have been synthesized. A good discussion of the many choices of anhydrides, amines, and solvents is given in Sroog (1976).

One typical example is that formed by the reaction of pyromellitic dianhydride (PMDA) with oxydianiline (ODA) to form PMDA-ODA polyamic acid precursor. The solvent used is *N*-methylpyrrolidone 2 (NMP) in which PMDA, ODA, and PMDA-ODA are soluble. Other suitable solvents are dimethylacetamide (DMAC), dimethylsulfoxide (DMSO) but NMP is preferred for reasons of safety.

Edwards (1965) and Sachdev et al. (1992) in their patents discuss methods of making aromatic PIs as well as the use of offset polymerization, i.e., the use of slightly unequal amounts of each monomer to control molecular weight and capping the end of the chain with a terminating agent.

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St. Clair and St. Clair (1992) teach the use of aliphatic polyol solvents to prepare aromatic PIs. Numata et al. (1987) teach the formation of low-CTE PIs; the chains have a rod-like structure and are highly oriented. Fluorinated PIs with isotropic, lower values of ε (<3) and CTE were prepared and characterized by Auman (1995). Low-ε nanofoam (porous) PIs were synthesized by Carter et al. (1995) and Cha et al. (1996).

4.4.2.3 Thermal Properties

The thermal stability of cured PI is determined using thermogravimetric analysis (TGA). Either the weight loss (usually in N_2) is monitored as the sample is heated at a constant ramp rate (typically 10°/min) and the temperature at which catastrophic failure occurs is noted, or the sample is held at a constant high temperature for an extended period of time and the weight loss measured. This is illustrated in Figure 2.33. Completeness of curing and an absence of outgassing during high-temperature processing, i.e., metallization and annealing, is an important requirement.

Another important specification is the glass transition temperature (T_g) since these organic materials do not have well-defined melting points. T_g is defined at the highest temperature reached before the onset of flow in the absence of a mechanical load and for use in a semiconductor device should be ≥350°C. Some of the strongly crosslinked PIs show no T_g but merely degrade upon heating. The relationship between T_g and temperature/time used for curing the PI was investigated by Palmese and Gillham (1987).

The value of CTE for most PIs is ~10 to 40 ppm/°C; the CTE of Si is 3ppm/°C and that of SiO_2 is 0.5 ppm/°C. Since the thermal stresses are driven largely by CTE mismatch, this is of great concern. Many of the new PIs have been synthesized to have CTE values of < 10 ppm/°C (Numata, et al., 1984; Auman, 1995). The stress due to thermal mismatch during a thermal excursion is discussed in Chapter 2. To a first approximation, the stress is linearly dependent on the difference between the expansion of the film and that of the substrate. There is, therefore, a strong motivation to match the CTE of PI to that of Si. It might be equally beneficial to match the CTE in the direction vertical to that of the metallization. Tong et al. (1991), using a laser interferometer measured CTE in the vertical direction (out-of-film plane) and concluded that for PMDA-ODA, the vertical CTE is 2 to 3 times larger than the in-plane CTE.

A large difference in the CTEs in the in- and out-of-plane direction implies that the deformation of PIs that are matched along the plane of the substrate may be substantially higher in the out-of-plane direction. Since the stress that organic films can support is typically low, the mismatch strain from the metal film in the in-plane direction is accommodated in the first 1 to 2 μm thickness of the polymer film. This is clearly an advantage for thick polymer film applications, as the deformation is localized within the film.

The behavior of the polymer can change from elastic to plastic during cycling of the film/substrate between room temperature and a high process temperature. As the thermal stress exceed the yield strength, stress relaxation occurs and is usually complete at high temperature.

Measurement of film stress is described in Chapter 2. The effect of thermal cycling on the stress of a BPDA-PDA film is shown in Figure 4.17 (Chen et al., 1998). As seen in the figure, the PI film is totally relaxed and stress-free at 400°C, but upon cooling the film experiences residual stresses. Since the stresses are relaxed, catastrophic failure is avoided. The stress relaxation is by plastic deformation, however, so that the thin film insulator may exhibit other problems such as extrusion and creep.

Thermal conductivity determines the heat dissipation from the devices and the resistive losses of the interconnection metallization and, hence, the maximum temperature of the chip. Organic insulators typically have thermal conductivities significantly lower than that of SiO_2. Jin et al. (1996) measured the conductivities of SiO_2 and PI by the method illustrated in Figure 2.31 and found that PI had a thermal conductivity of 2.4 mW/(cm °C), compared with a value of 11.5 mW/(cm °C) for plasma SiO_2. A low-thermal-conductivity insulator can result in higher

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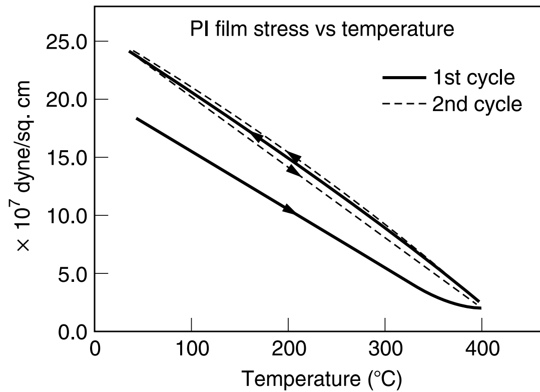

Figure 4.17 Changes in film stress due to thermal cycling of BPDA-PDA PI film. (Courtesy of Chen, S.T., C.H. Yang, F. Faupel, and P.S. Ho, *J. Appl. Phys.* 64, 6690, 1988.)

device operating temperatures; this can lead to device degradation and cause interconnection failures.

4.4.2.4 Adhesion/Interface Reactions

The basic concepts and methods of measuring adhesion are discussed in Chapter 2.

An adhesion strength exceeding 25 g/mm, obtained using the peel test, is considered adequate for PIs; higher values may be required for specific applications. Adhesion tests are used to evaluate the effectiveness of adhesion promotors and surface treatments. Exposing PI films to a plasma containing O_2 and CF_4 resulted in a substantial number of $F-C=O$ groups on the surface, which appeared to improve the adhesion.

Chromium and titanium bond well to PI surfaces and are often used as glue layers. Using XPS, the chemical interaction between Cr, Cu, Pd, and Ni over PI was studied and it was shown that metal atoms bonded to the C, N, or O atoms in the PMDA monomer (Chou and Tang, 1984). Burkstrand (1979a,b, 1981), based on XPS studies, concluded that adhesion of metallic films to PI is directly related to the electronegativity of the metallic film, with Cu $<$ Ni $<$ Cr. Haight et al. (1988), studying adhesion of Cr and Cu to polyimide by XPS, suggested that, based on the energy spectrum, Cr had two types of bonding whereas Cu had a single weak interaction or bonding. LeGoues et al. (1988) showed that Cr–PI formed a well-defined interface, but Cu–PI interface was broken by the precipitation of Cu in PI. On annealing, Cu precipitate coarsens, indicative of the poor stability of the Cu–PI interface. Kim et al. (1990) found PI/metal was different from metal/PI. When PI is spun on a metallic surface, the polyamic precursor creates a stronger metal–PI bond than when metal is deposited over a cured PI surface.

Faupel et al. (1989a,b) studied the interaction and diffusivity of Cu and Cr in PMDA-ODA, using an isotope of Cu as a tracer. The diffusivity of Cu ranged from 10^{-15} to 10^{-14} cm^2/sec in PMDA-ODA in the temperature range 200 to 300°C; the diffusivity in PI is an order of magnitude higher than that in SiO_2 (McBrayer et al., 1986).

Absorption of moisture, which varied linearly with relative humidity, probably results in oxidation of the interfaces, thereby causing delamination. The relative ease of moisture absorption and diffusion in PIs has been well documented (Sacher and Susko 1979, 1981; Denton et al., 1985); at room temperature, the diffusivity of water in PMDA-ODA is 10^{-9} cm^2/sec, so that it will take only a few seconds for water to diffuse through a film 1 μm thick. In addition, release of moisture trapped within PI or at the PI/metal interface was held responsible for bubble formation in a PI film (Mitchell and Goodner, 1984; Peek and Wolters, 1986).

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4.4.2.5 Mechanical Properties

The mechanical properties include stress–strain behavior at different temperature, CTE, Poisson's ratio (ν) and the elastic (Young's) modulus (E). Methods used to determine these properties can be found in Chapter 2. The earlier work on thick polymers showed the effect of structural anisotropy on the resulting anisotropy of mechanical properties (Gupta and Ward, 1968; Hadley, 1975). Since the spin-on films tend to have preferred structures in the plane of the film and perpendicular to the film's surface, the mechanical properties need to be measured in both the in-plane and out-of-plane directions. The measurement of these properties is difficult as the films are very fragile. Despite the complexity and limited data, finite element methods were used to obtain approximate stress–strain distributions in the device structures (van Andel and Gootzen, 1989). Thicker free-standing films (~10 μm) were used in a tensile pull tester apparatus (Srikrishnan et al, 1990; Chen, 1995) to measure stress–strain behavior at different temperatures. The stress–strain data for BPDA-PDA and PMDA-ODA are shown in Figure 4.18.

The ductility increases and yield stress decreases appreciably at high temperatures and strength. The ductility was about 35% for BPDA-ODA and about 60% for PMDA-ODA at room temperature. However, BPDA-PDA exhibited higher toughness (area under stress–strain curve) compared with PMDA-ODA which is desirable.

The CTE of PIs is covered in Section 4.4.2.3.

Poisson's ratio for PIs is about the same as that of other insulators, i.e., ν ~ 0.3 to 0.5 (Bauer et al., 1988). The elastic moduli, however, are significantly lower than that of SiO_2 but higher than that of most of the newer low-ε films. For example, Chen (1995) measured the out-of-plane value of E for BPDA-ODA to be about 1 GPa at 20°C, much lower than the in-plane value of 11.7 GPa. This is in contrast to PMDA-ODA for which E is 4 GPa in both directions. Chen (1995) attributed the

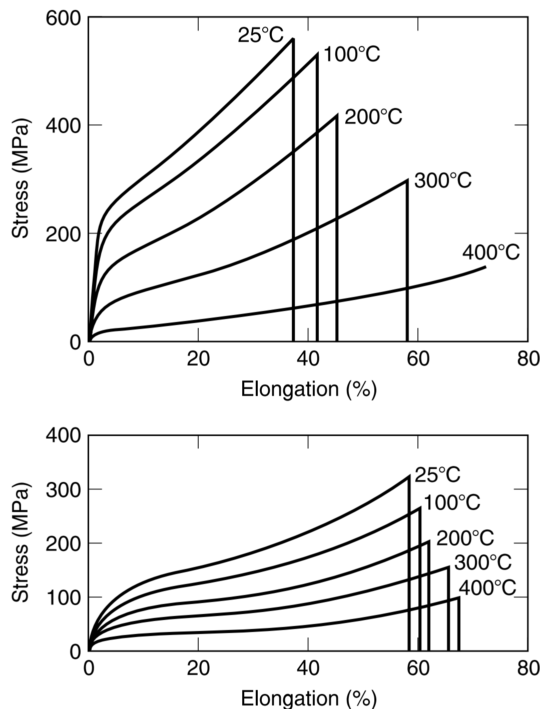

Figure 4.18 Stress vs. elongation (strain). Top: BPDA-PDA PI film; bottom: PMDA-ODA PI film. (Courtesy of Chen, S.T., C.H. Yang, F. Faupel, and P.S. Ho, *J. Appl. Phys.* 64, 6690, 1988.)

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BPDA-PDA behavior to the weaker bonding in vertical planes compared with the stronger covalent bonding in the in-plane structure. Auman (1995) measured in-plane mechanical properties of rod-like fluorinated PIs prepared using different monomer groups; the values of E ranged from ~4 to 10 GPa.

4.4.2.6 Electrical Properties

This section discusses electrical conduction, ε, dissipation factor, the time-dependent breakdown (TDDB) of the dielectric film, and the effect of ionic impurities and moisture on these properties. Most published data are on thin PI films and usually in the out-of-plane direction; some recent measurements in the in-plane direction have become available.

4.4.2.6.1 Electrical Conduction

Smith et al. (1987) reviewed electrical conduction in PIs, in particular PMDA-ODA and BTDA-ODA/MPDA using a capacitor structure. The PIs showed a strong current transient when the voltage is impressed, especially at temperature below 100°C. The charging and discharging is fully reversible and the decay current followed a $(\text{time})^{-0.8}$ relationship. The charging and discharging behavior was attributed to the alignment of the weak dipoles in the PI with the externally applied field. The charging and transport current increased with moisture uptake. Above 150°C, the current is primarily transport or leakage. Figure 4.19 shows *I–V* behavior of BPDA-PDA at three different temperatures (taken at 0.5 V/cm).

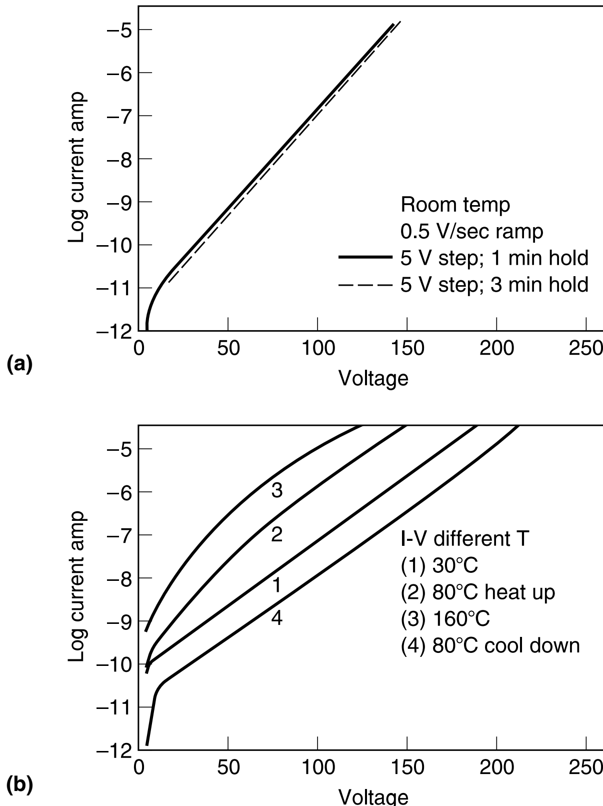

Figure 4.19 *I–V* curves for BPDA-PDA PI film: (a) film at room temperature, voltage ramped in 5 V steps; (b) effect of thermal treatments.

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The current at a given electric field increases at higher temperature, as observed for other insulators. However, when the film was heated from 30 to 80°C, the current at 80°C was larger than when the film was cooled down from 160 to 80°C. A likely explanation is that the film at 80°C on heat-up probably had more moisture than the film that cooled down to 80°C from 160°C. Several studies (Sacher, 1979; Sawa et al., 1980; Rothman, 1980; Chang et al., 1982) have proposed that the transport current in PI to be primarily due to H^+, H_3O^+, Na^+, etc. Neuhaus et al. (1985) found that, below 200°C, the transport current was similar for Na^+-doped and undoped films; they suggested that at high temperatures ionic impurities totally dominate leakage.

The rapid diffusion of ionic impurities can cause device instabilities if the PI is used adjacent to a device such as a gate of a field effect transistor (Bergeron et al., 1984; Brown, 1981). Sato et al. (1973) showed that the instability can be avoided by using PIs with low ionic impurities. Beuhler et al. (1989) showed that fluorinated polymers with even high Na^+ did not cause device instability, the assumption being that diffusivity is very low or the Na^+ ions are tied down locally.

4.4.2.6.2 Breakdown

Electrical breakdown of an insulator usually occurs when the localized electrical fields exceed a critical value, causing a large current flow which results in excessive heat and melting or vaporizing of the electrode. In the case of inorganic materials, the breakdown invariably occurs at local weak spots, the shorting is usually irreversible. Rothman (1980) reported that PIs (PMDA-ODA, Skybond) have a breakdown strength of 5 to 8 MV/cm comparable with SiO_2, whereas others (Homma et al., 1988) reported a lower breakdown voltage of 3 to 5 MV/cm. In Rothman's study, the leakage current density corresponding to breakdown field was 2 to 3 orders of magnitude larger than SiO_2. In most of the studies, the breakdown criterion was not defined explicitly. Figure 4.20 shows a cumulative histogram of the behavior of many Al-dot capacitors using PI (BPDA-PDA) or PECVD SiO_2 as the dielectric For both PI and PECVD oxide, the breakdown voltage was defined as that at which a breakdown spike was sensed or the current reached 1 μA (~0.5 mA/cm^2). In the case of PI, the current of all capacitors increased monotonically, reaching the predetermined maximum value and in all cases of PECVD oxide a breakdown was noted.

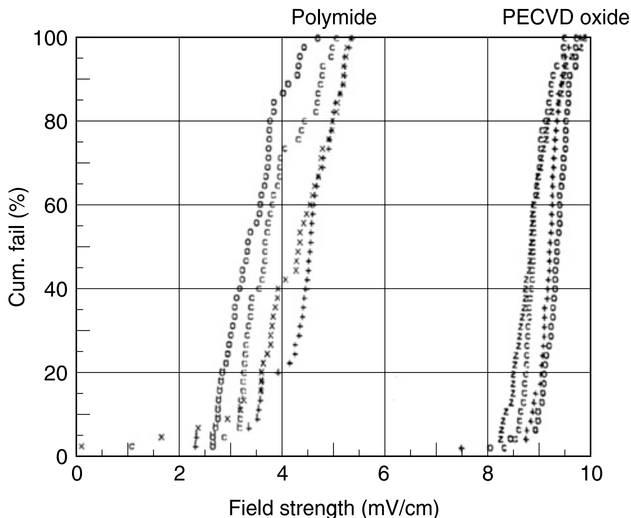

Figure 4.20 Cumulative failures vs. field strength: comparison of PI and PECVD SiO_2.

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Samuelson (1982) noted that both PIQ and PI2545 had a thickness-dependent breakdown characteristic; this was attributed to the existence of pinholes. Samuelson (1982) used statistical breakdown measurements (shorts) at low fields to show that the pinhole probability for a 1.2 μm PI film was 7.5 in a million. This not only attests to the high uniform quality achievable with spin-on PI, but also explains the high current density supported by PI before breakdown, especially if the film is cast from a high-purity solution.

4.4.2.6.3 Dielectric Constant

Most of the measurements of ε of PI thin films have been made in the range of 10 kHz to 1 MHz. Depending on the chemical group, ε of the PI films was in the range 2.5 to 4. Denton et al. (1985) showed that ε of PMDA-ODA when dry was 3.5, and increased by as much as 10% when soaked in water; thus exposure to ambient moisture may also result in an increase in ε. There has been extensive study of ε in many of the new PIs in both in-plane and out-of-plane directions. Auman (1995) studied several rod-like fluorinated PIs and showed that their dielectric properties were isotropic, with $\varepsilon < 3$. Ip and Ting (1995) used serpentine metal lines to measure the values of ε both in-plane and out-of-plane for a large number of low-ε organic insulators and found that in-plane dielectric constants were higher than out-of-plane ones by 0 to 14%.

4.4.2.6.4 Dissipation Factor

This is discussed in Chapter 2, Section 2.6.4.

4.4.2.7 Patterning of PIs

Etching of organic and low-ε films is covered in Sections 4.7 and 4.8.

4.4.2.8 Conclusion

Polyimides were the first materials to be considered as an alternative to SiO_2 as *the* interlevel dielectric. Although they did find their way into some commercial products, they have since been displaced.

4.4.3 F-Doped SiO_2

The synthesis, properties, etc., of this material are covered in Section 4.2.7. Although the push is toward even lower dielectric constant films for high-speed applications and interest in SiOF, therefore, diminishing, it may be revived if integration of the newer films proves too complex or too costly.

4.4.4 Parylenes

Parylenes (poly-*p*-xylylene) are semicrystalline aromatic polymers prepared by vapor deposition polymerization. No solvents are used and no curing is required. The usual precursor is the dimer di-*p*-xylene which is sublimed, pyrolized at a high temperature to form the monomer, and finally condensed at room temperature or below (Gorham method). The steps in the synthesis of an unsubstituted parylene are shown in Figure 4.21.

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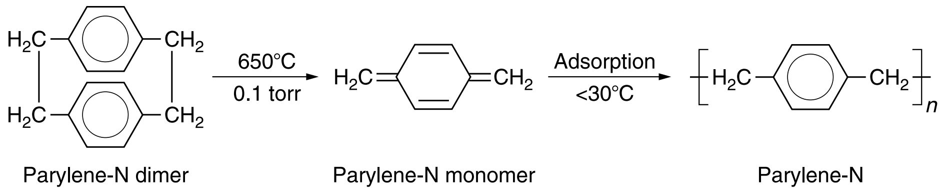

Figure 4.21 Synthesis of parylenes.

There are a number of parylenes, both unsubstituted (or normal parylene-N) and those with organic and halogen substituents. They all have low dielectric constants (< 2.8), low stress, low moisture permeability, and are relatively thermally stable. Parylene-G (the fluorinated parylene) has the lowest dielectric constant but unfortunately the precursor is in limited supply.

Parylenes were used as encapsulants on printed circuit boards and their use as interlevel dielectrics was suggested by Najid (1988). Most work has been done using parylene-N since it is most readily available. The deposition rate increases with increasing source temperature and chamber pressure, although at high pressure the film quality is degraded, possibly due to gas-phase reactions. Lowering the source temperature produced smoother films but altered no other film properties (Plano et al., 1997). The rate increases with decreasing chuck temperature, indicating the rate-limiting factor is condensation on the monomer (Selbrede and Zucker, 1997). Increasing the pressure also increased the deposition rate but when the pressure was too high (> 80 mtorr) the films became cloudy. Good films could be deposited at high rates when an electric field was applied (Yanog et al., 1996). Higher molecular weight films are deposited at the lower temperatures thereby increasing the thermal stability (Ganguli et al., 1997). Young's modulus was at its maximum value (~0.5 GPa) for films deposited at ~0°C, decreasing rapidly as the temperature was increased. The films must be annealed before processing to stabilize the thermal stresses (Ryan et al., 1997).

The parylenes are soft as are all organic films and are deeply scratched during CMP. The damage was eliminated by depositing more parylene which, because of its excellent gap-fill property, filled the scratches; the excess was removed by plasma etching (Wang et al., 1998).

By mixing reactive parylene-N monomer with a volatilizable comonomer, a random polymeric film can be formed on the substrate (Taylor et al., 1997). A copolymer of parylene-N and tetravinyl-tetramethyl-cyclotetrasiloxane has improved adhesion to SiO_2, improved thermal stability (after an initial cure), and a lower dielectric constant (close to ~2.1) than the homopolymer The reduction in dielectric constant was attributed to separation of the benzene rings in the parylene-N backbone, lack of crystallinity, and reduction in density. It was postulated that, since the comonomer is crosslinkable, the stability and adhesion was not compromised.

Wary et al. (1996), Harrus et al. (1997), and Ganguli (1997) studied a fluorinated parylene, parylene AF-4 in greater detail. The film is usually deposited using the Gorham method but Ganguli et al. (1997) produced the monomer directly from 1,4-bis(trifluoromethyl)benzene as the precursor.

There are volatile components in the as-deposited film; they were removed by heating in the range 250 to 400°C, but after the film was stabilized the weight loss at 450°C in N_2 was 0.08 wt%/h. The stability is somewhat better than that of parylene-N. The refractive index stabilized after a small increase following an initial anneal. The birefringence was measured using a prism coupler: $RI_{out\text{-}of\text{-}plane} = 1.5482$, $RI_{in\text{-}plane} = 1.4522$, indicating dielectric anisotropy. The out-of-plane dielectric constant was 2.28. The Young's modulus was 2.7 GPa and the CTE was 180 ppm at 25°C. The film grows from the substrate surface and is uniform and conformal. The adhesion to the substrate, overlayers, and previously deposited parylene layers is excellent.

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4.4.5 Poly(arylene ether)s (PAEs)

Both fluorinated and nonfluorinated PESs have been suggested for use as dielectric materials for MLM. Several fluorinated PAEs were patented by Mercer and Sovish (1992). The basic repeat unit is shown in Figure 4.22.

The compounds are formed by a condensation reaction between decafluorobiphenyl and a variety of aromatic biphenols; the resulting thermoplastic polymer consists of linear chains. The materials have been developed by Allied-Signal (now Honeywell Electronic Materials) as FLARE™ (which appears to be an acronym for fluorinated arylether) (Hendricks et al., 1995). The spun-on films contain no moisture and none is evolved during the cure cycle. The dielectric constant has been reported as ~2.4 to 2.6 (Hendricks et al., 1995) and as 2.84 (Lau et al., 1997). The tensile stress (~30 to 60 MPa) and the moisture absorption (<0.2%) are low, but CTE is high (73 ppm/°C); thermal stability after curing at 450°C (2 hours in N_2) is excellent. Adhesion promoters are needed for some substrates. The major drawback for this version, FLARE™ 1.0, is a low T_g (~280°C). Modification of the synthetic method produced a new version, FLARE™ 1.51 whose T_g is <350°C; it has a slightly higher ε (2.6 to 2.8) but lower CTE (33 to 63 ppm/°C) (Lau et al., 1996).

Nonfluorinated PAEs were patented by Burgoyne et al. (1997). The generic structure of the repeat units of the polymer is shown in Figure 4.23, where Ar_1, etc., are divalent arylene radicals and $m = 0$ to 1.0 and $n = 1.0 - m$. A commercially available version, from Schumacher/Air Products, is PAE-2, whose structure is given in Figure 4.24.

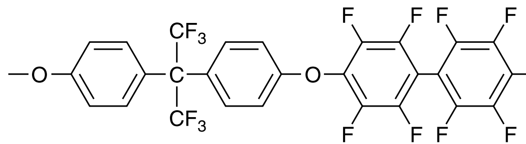

Figure 4.22 Repeat unit of fluorinated poly(arylene ether)s. (From Mercer, F.W. and R.C. Sovish, U.S. Patent 5,115,082, 1992.)

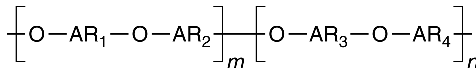

Figure 4.23 Repeat unit of poly(arylene ether) polymer. (From Burgoyne, Jr., W.F., L.M. Robeson, and R. Nicholas, US Patent 5,658,994, 1997.)

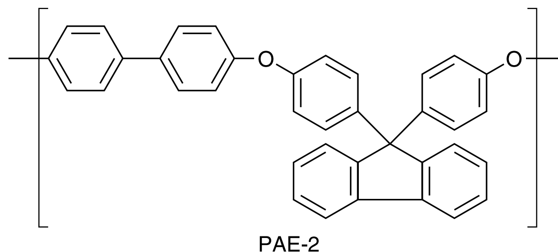

Figure 4.24 Structure of PEA-2. (From Burgoyne, Jr., W.F., L.M. Robeson, and R. Nicholas, US Patent 5,658,994, 1997.)

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A solution of PAE-2 in cyclohexane has very low chain branching and a tight molecular weight distribution. The solution is spin-coated with no need for an adhesion promoter. Multiple applications, with a soft-bake between applications, are required for films > 1.0 μm. The film is cured at 425°C in 20%O_2/80%N_2 to crosslink the PAE-2 to increase T_g and enhance the structural rigidity of the film. The refractive index (n) of the film is ~1.67 and the dielectric constant (ε) is 2.4 ± 0.4, indicating no (or very little) frequency dependence of ε due to the absence of easily polarizable groups. The moisture resistance is related to the presence of ether linkages, and the thermal stability to lack of hydrocarbon groups (Vrtis et al., 1997).

Another version of a PAE, also based on the Burgoyne patent, has been developed by Schumacher/Air Products: Velox™. It requires only minutes on a hot plate at 400°C, in air, to crosslink the film and achieve T_g > 425°C.

There is some confusion in the nomenclature of PAEs since one version of FLARE™, FLARE™ 2.0, is nonfluorinated. It was developed to improve T_g still further (>450°C) without any other significant changes in the film properties (Lau et al., 1997).

4.4.6 Fluorinated Amorphous Carbon Films (α-C:F)

These are aliphatic polymers whose structures are derived from that of polytetrafluoroethylene (PTFE). PTFE is a linear chain of CF_2 groups, as shown in Figure 4.25. It has the lowest dielectric constant of any nonporous material (1.9), attributable to the low polarizability of the C–F bond. It has good thermal stability (< 1% weight loss/h at 450°C) (Cruden et al., 1999a), low moisture absorption, and is relatively chemically inert. Its poor adhesion can be managed by the use of adhesion promoters. However, the uncrosslinked chain is flexible so that it has very poor mechanical properties; it is has a low yield stress (12 MPa), low elastic modulus (0.5 GPa), low softening temperature (250°C), and a high CTE (>100 ppm/°C) (Morgen et al., 2000). Thus it is unsuitable as an interlevel dielectric. Modification of the structure to increase the mechanical strength while maintaining the low dielectric constant and thermal stability has been the aim of material development.

The most common method of deposition for α-C:F films has been PECVD in both capacitively coupled (e.g., Endo and Tatsumi, 1995; Lau and Gleason, 1999; Agraharam et al., 2001) and high-density plasmas (e.g., Endo and Tatsumi, 1996,1997; Labelle et al., 2000; Han et al., 2001), using both continuous (e.g., Endo and Tatsumi, 1995; Agraharam, 1999) and pulsed modes (e.g., Labelle et al., 1997; Lau and Gleason, 1999; Labelle and Gleason, 2000). Thermal CVD has also been reported (Limb et al., 1996).

A wide variety of precursors have been tried. Some examples are: $CF_4 + CH_4$, $C_2F_6 + H_2$ (Endo and Tatsumi, 1995), C_3F_6O (hexafluoropropylene oxide) (Limb, 1998), CH_2F_2 (Labelle and Gleason, 1999), CF_3CHF_2/Ar (Agraharam et al., 1999), $C_2H_2F_4$ (Labelle and Gleason, 2000), C_4H_8 (Agraharam et al., 2001), $C_4F_8 + C_2H_2$ (Takeishi et al., 1997), and $C_4H_8 + H_2$ (Takada et al., 2001). All the precursors yield CF_x fragments by electron-impact dissociation in the plasma. Although the

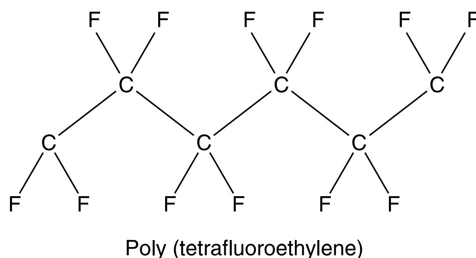

Figure 4.25 Structure of polytetrafluoroethylene.

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fluorinated precursors often contain H (and thus have low global warming and ozone depletion potentials) and in some cases H may be provided by an additive, e.g., C_2H_2, the H-content of those films is reported to be low; this was attributed to the elimination of HF (Agraharam et al., 1999). C_3F_6O is an excellent source of CF_2 and since the other product of decomposition is a stable aldehyde that is pumped away, no significant amount of O is incorporated into the film. When O has been detected in α-C:F films, it is believed to have been the result of postdeposition oxidation (Agraharam et al., 2000).

In the continuous mode, ion bombardment of the growing films creates reactive sites and is an important factor in crosslinking and film growth (Agraharam et al., 1999). In the pulsed mode (which can be high/low power or on/off power) during the high or on part of the cycle, the precursors are fragmented and the substrates subjected to ion bombardment, but in the low or off times, as in a downstream reactor, there is reduced or no ion bombardment. In this part of the cycle growth continues with the long-lived reactive neutrals dominating the process. Theil (1999) has described pulsing as an approximation of thermal CVD at a lower temperature. Pulsing affords a measure of control of ion bombardment; Labelle et al. (1997) showed that the dangling bond (free radical) concentration decreased rapidly with increased "off" time and then leveled off. If dangling bonds contribute to dielectric loss, their reduction may improve the dielectric properties of the film; the interaction with atmospheric oxygen and water (aging effects) may also be suppressed. Pulsing also changes the nature of the deposited film. With C_3F_6O as the precursor, Limb et al. (1998) found that, in changing from the continuous to the pulsed mode, the CF_2 content of α-C: F films increased, eventually becoming the dominant species (65% vs. 34%) for long off times. The deposition rate decreases with increasing substrate temperature, suggesting reactant adsorption is the rate-determining step. The F/C ratio was lower in films deposited at higher temperature (Agraharam et al., 2000). In the continuous mode the rate increases with increasing input power (Agraharam et al., 1999). In the pulsed mode the deposition rate increases with increasing duty cycle ($t_{on}/t_{on} + t_{off}$) indicating the importance of plasma processes (Cruden et al., 1999). However, there is an initial increase in rate with increasing off time during which the role of the neutral species is important (Labelle et al., 1998). The deposition rate is higher in a C_4H_8 plasma than in CF_3CHCF_2 (PFE); this has been attributed to the fact that the primary precursor derived from PFE is CHF_2, whereas linear fragments are formed from C_4H_8 and may be incorporated directly, resulting in a higher rate (Agraharam, 2001). The highest rate/cycle was obtained using $C_2H_2F_4$; the higher C-content may favor longer chain segments for incorporation (Labelle et al., 1998).

An example of the dependence of film structure on the choice of precursor is shown in Table 4.5a. These films were deposited in the pulsed mode of 10 on/100 off (Labelle et al., 1998, 1999). Some of the properties of films deposited in the continuous mode are given in Table 4.5b (Agraharam et al., 2001).

The F/C ratio of tetrafluoroethylene is 2; it is <2 in all the PECVD α-C:F films. The lower F/C ratios indicate crosslinking in the film. It has been possible to produce films with different total F/C ratios and relative fractions of CF_3, CF_2, CF and $\underline{C}$–CF ($\underline{C}$ is a quaternary C, i.e., a nonfluorinated C), C–C, and C=C and with different structures, i.e., with different degrees of crosslinking and branching, and density. The higher the F/C ratio, the lower the dielectric constant, but the worse the thermal stability. The larger the relative concentration of CF_3 and CF_2 to CF, the lower the ionic and dipolar polarization and thus the lower the dielectric constant. Decreased density also lowers the dielectric constant (Han et al., 1999, 2001).

Decomposition of α-C:F films during high-temperature (e.g., 400°C) processing in IC manufacturing can lead to evolution of F which can interact with metals (Ti, Ta, etc.), and degrade adhesion. There have been conflicting reports about the effect on ε of heating at or above 400°C. Both Theil et al. (1997) and Yang (1998) reported a decrease in ε, related to a decrease in density. Han et al. (2001) however, found that a loss of F was accompanied by an increase in density; both factors led to an increase in ε and n. However, at very high degrees of crosslinking the stability increases but

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Table 4.5a Dependence of Film Structure on the Choice of Precursor

	C_3F_6O	$C_2H_2F_4$	CH_2F_2	$CHClF_2$
% CF_3	18	8	4	7
% CF_2	55	21	12	39
% CF	14	25	24	24
% C–CF	13	46	60	30
F:C ratio	1.78	0.91	0.60	1.22
n^2	1.84	2.07	2.24	2.25
ε	2.0	2.4	2.4	2.4
Tan δ	0.009	0.018	0.012	0.012

Table 4.5b Properties of Films Deposited in the Continuous Mode

Precursor	CF_3CHF_2	C_4F_8
Dissociation fragments	CF_3, CHF_2	C_2F_4, C_3F_6
F:C ratio	1.10–1.20	1.17–1.32
n	1.41–1.42	1.38–1.39
ε	2.28–2.25	2.18–2.33
Tan δ	0.023–0.099	0.013–0.035
Thermal stability (5% weight loss)	297–320°C	298–314°C

the dielectric constant rises rapidly as well (Cruden et al., 1999a,b). Increased deposition temperature and the use of a plasma with a high H-content (from the precursor or added as, for example, a hydrocarbon) produces a film with a lower F/C ratio, i.e., higher degree of crosslinking and thus greater stability. However, as can be seen in Table 4.5b, even in films with a relatively low F/C ratio (moderate crosslinking), the temperature at which decomposition sets in is too low for practical application (Takeishi et al., 1997). Agraharam et al. (2000) also noted a decrease in thermally labile CF_3 end groups in films deposited at higher temperature and a lower low-weight loss for films deposited on a grounded electrode instead of on the powered electrode (1% vs. 3%). Labelle and Gleason (2000) improved the stability of films deposited using $C_2H_2F_4$ in the pulsed mode by increasing the flow rate of precursor, attributed to a reduction of CF_3 groups in the film. Cruden et al. (1999a) found that, under identical deposition conditions, films prepared with $CF_2{=}CF_2$ as the precursor were more stable than those using $CF_3{-}CF{=}CF_2$, CF_2HCF_2H, $CF_2HCF_2CF_2CF_2H$, and C_3F_6O due their high unfluorinated content (but therefore higher dielectric constant).

There appear to be two regions of weight loss. At low temperature (~100°C) low molecular weight trapped species or loosely bonded chain segments are lost. At higher temperatures polymer degradation occurs.

Although it has been shown that the choice of precursor and deposition conditions can produce films with somewhat different properties, as pointed out by Banerjee et al. (1999), the basic structures are not significantly different and none prepared thus far are adequate as low dielectric constant interlevel dielectrics.

4.4.7 Silsesquioxanes (SSQs)

These are spin-on resins having the general formula $(XSiO_{1.5})_n$, where X is H or an organic group and $n = 2, 3, 4, \ldots$. Hydrogen silsesquioxane (HSQ) and methyl silsesquioxane (MSQ) have been developed commercially and are used as interlevel dielectric films.

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4.4.7.1 Hydrogen Silsesquioxane (HSQ)

The oligomers from which these resins are derived have either a linear double chain (ladder) (Figure 4.26a) or a cage structure (Figure 4.26b). The film structure may be considered as an expanded version of SiO_2, with the excess volume being responsible both for the lower dielectric constant but inferior mechanical properties when compared with SiO_2.

The resins formed from the cage oligomer are not fully formed cages but a random structure of partially formed cages of various sizes, as illustrated in Figure 4.26c. The IR spectrum of the resin indicates that the Si–H bond environment is more randomly distributed in the resin than in the oligomer (Laboda et al., 1998).

The film formed from a soluble HSQ resin by sol–gel processes (spin-coating and annealing) is an amorphous hydrogenated silicon oxide (α-SiO–H) in which one of the O bonded to Si is replaced by a H atom. The film has a three-dimensional glassy structure with a siloxane (–Si–O–Si–) backbone (Cook and Liniger, 1999).

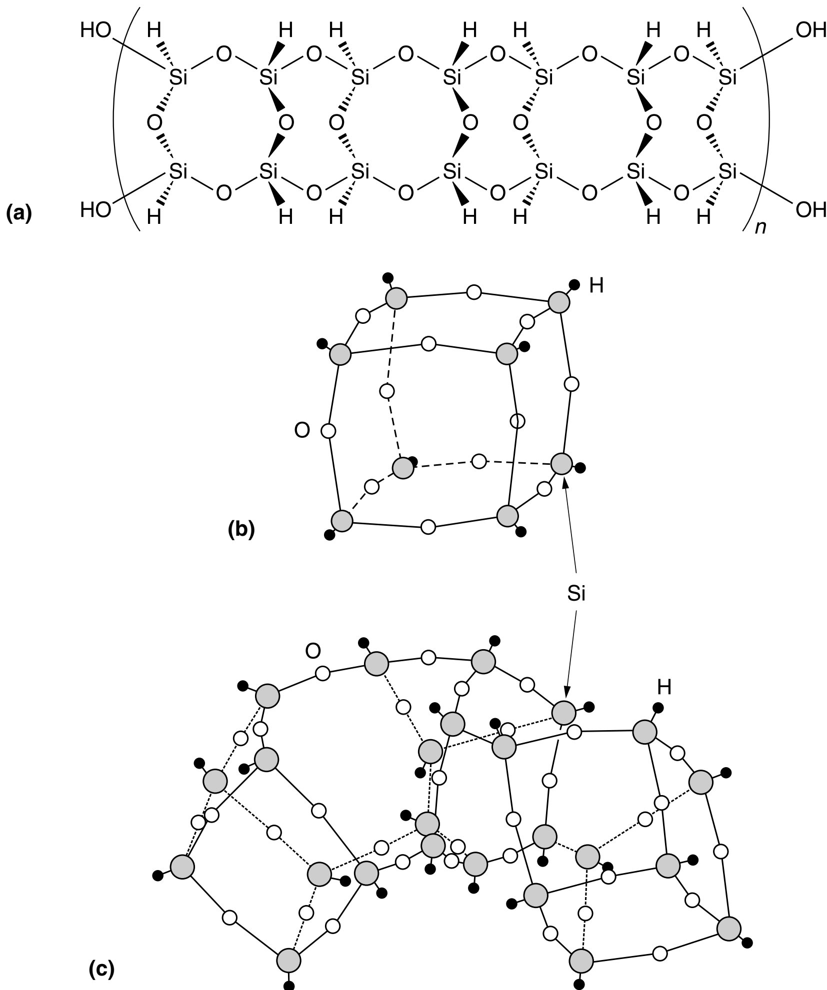

Figure 4.26 (a) Schematic of a ladder HSQ. (Adapted from Hacker, 1997.) (b) Schematic of a cage HSQ and (c) resinous material. (Reproduced from Laboda, M.J., C.M. Grove, and R.F. Schneider, *J. Electrochem. Soc.*, 145, 2861, 1998. With permission of the Electrochemical Society, Inc.)

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The first HSQ (derived from the cage oligomer resin) to be reported was the Dow-Corning flowable oxide FOx (Pineda, 1990). FOx was a gap-filling, planarizing material with a dielectric constant of ~4. Subsequently Ahlburn et al. (1995) reported that a dielectric constant of 3 was possible when the right process conditions (not specified) were used. With the advent of damascene processing, the gap-fill properties are no longer important, but a dielectric constant ≤ 3, now routinely realized, is responsible for the interest in it as an interlevel dielectric film. FOx has high thermal stability, high hardness, and low outgassing. Since it does not have Si–C or C–C bonds it does not cause via poisoning (Siew et al., 2000). However, there is a tendency for it to absorb moisture from a humid environment.

The IR spectrum of the HSQ film shows the presence of Si–H bonds and an $SiO_{4/2}$ (i.e., Si bonded to four shared O atoms) bond environment. Siew et al. (2000a) have summarized the processes occurring during the thermal cure (in inert atmosphere) following spinning of the resin solution:

1. $<200°C$: solvent loss
2. 250 to 350°C: network redistribution involving the exchange of Si–O and Si–H bonds between neighboring SSQ oligomers, and $SiO_{4/2}$ formation, and SiH_4 and H_2 evolution
3. 350 to 435°C: Si–H dissociation, increased evolution, expansion with accompanying reduction in density, refractive index, and dielectric constant
4. $>435°C$: collapse of porous network, contraction, increase in density with accompanying increases in refractive index and dielectric constant

Therefore, ~ 400°C appears to be the optimum cure temperature.

Oxidation of Si–H bonds increases the incorporation of SiO_2 bonds in the film structure and the formation of –OH, resulting in a higher dielectric constant. Thus it is imperative that even small amounts of oxygen be excluded from the annealing atmosphere (Laboda and Toskey, 1998).

Zhao et al. (1999) reported that the stress in an HSQ film (measured after the thermal stabilization cycle) was tensile (~35 MPa) and the CTE, measured using the two-substrate bending beam method was 20.5 ppm/°C. The biaxial modulus $E/(1-\nu)$ was 7.1 GPa. Assuming a value of ~0.25 for the Poisson ratio (ν), the Young's modulus (E) was ~5.3 GPa.

Under the influence of bias and elevated-temperature stress, Cu diffuses more readily in HSQ than in SiO_2. Various modifications of an HSQ film have been suggested to prevent this. One of these was forming a thin SiN_x layer using an NH_3 plasma (Liu et al., 2000a). Another is the use of a D2 plasma which is postulated to passivate the dangling bonds exposed in the structure of the HSQ film, decreasing the diffusion paths of Cu through the HSQ (Liu et al., 2000b).

Petkov et al. (1999a,b) studied several changes in the structure of HSQ due to annealing, water absorption, and exposure to an O_2 plasma using Doppler broadening PALS as a probe for voids formed between the cages. The voids were distributed uniformly. They correlated the number of open-volume defects with the dielectric constants of the films. Long-term and/or high-temperature annealing in N_2 resulted in smaller and/or fewer voids, i.e., the films were densified and the dielectric constants increased. They determined that exposure to a humid environment did not change the porosity but that the water molecules diffused through the structure and occupied the open void volume. Oxidation of the films in an O_2 plasma proceeded from the film surface to the substrate and increased ε. A decrease in ε after subsequent annealing in FG was attributed to void formation at the film/substrate interface.

A ladder HSQ was studied by Albrecht and Blanchette al. (1998). They stated that it undergoes the same redistribution of bonds as does the cage structure. Hacker et al. (1998) reported on a commercially available ladder HSQ called *Accuspin* [R]T-23. They agreed that the ladder HSQ was more thermally stable than the cage structure, but they disagreed about its dielectric constant. According to Albrecht and Blanchette (1998), after a 400°C cure it was ~4 whereas Hacker et al. reported it to be lower than that of the caged HSQ, i.e., 2.8 to 3.0.

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4.4.7.2 Methyl Silsesquioxane (MSQ)

The methyl-substituted SSQ films, MSQs with a methyl group on every Si atom, have also been called organosilicate glasses, OSGs.

MSQ films have a low dielectric constant (2.7) and good resistance to moisture absorption. However, when exposed to an oxygen plasma during resist stripping, the Si–CH_3 bonds are converted to Si–OH and Si–O bonds. The film becomes hygroscopic so that the dielectric constant and leakage current increase. Several processes have been developed to enhance the resistance of MSQ to this damage. Two of these are H_2 (Chang et al., 1999a) and N_2O (Chang et al., 1999b) plasma treatments.

4.4.7.3 Methyl Hydrogen Silsesquioxane (MHSQ)

A methyl hydride SSQ (MHSQ) called HOSP[R] for hybrid organic siloxane polymer (available form Allied Signal, Inc.) has also been developed. The dielectric constant of HOSP is 2.5. Figure 4.27 compares the FTIR spectra of SiO_2 and HOSP; it shows the peak at 1160 cm^{-1} of the cage-like Si–O stretching mode, typical of the cage SSQs (Hwang et al., 2002). It was concluded that HOSP is a mixture of closely crosslinked network Si–O and sparse cage-shaped Si–O structures. The spectrum also shows the peaks attributed to Si–H and to various C-containing groups.

"During curing, HOSP is polymerized by opening the cage-shaped oligomers and is partially transformed into $SiO_{4/2}$" (Hwang et al., 2002).

An NH_3 plasma treatment, converting the organic HOSP surface to an inorganic SiN_x layer, increases the resistance of HOSP to moisture absorption, oxidation during ashing, as well as Cu penetration (Liu et al., 2001). Replacing oxygen with N_2/O_2 in downstream ashers or using an O_2 plasma in conventional etch reactors reduce the damage. The susceptibility to oxidative damage has driven the search for stripping solvents. A proprietary material, ACT K115, appeared to be suitable (Dunne et al., 2000).

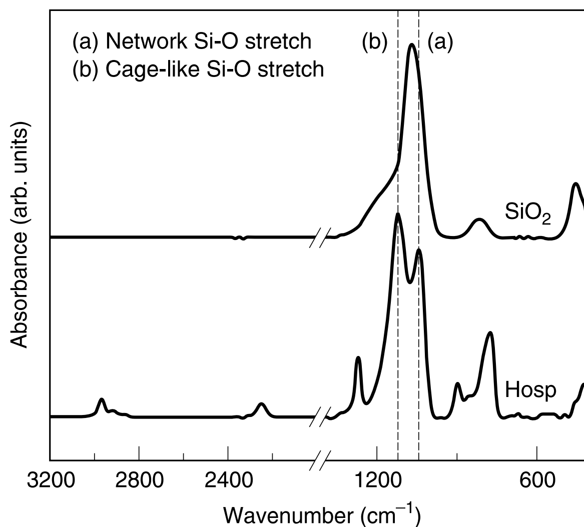

Figure 4.27 FTIR spectrum of HOSP. (Reproduced from Hwang, S.-W., G.-R. Lee, J.-H. Min, and S.H. Moon, *Jpn. J. Appl. Phys.*, 41, 5782, 2002. With permission.)

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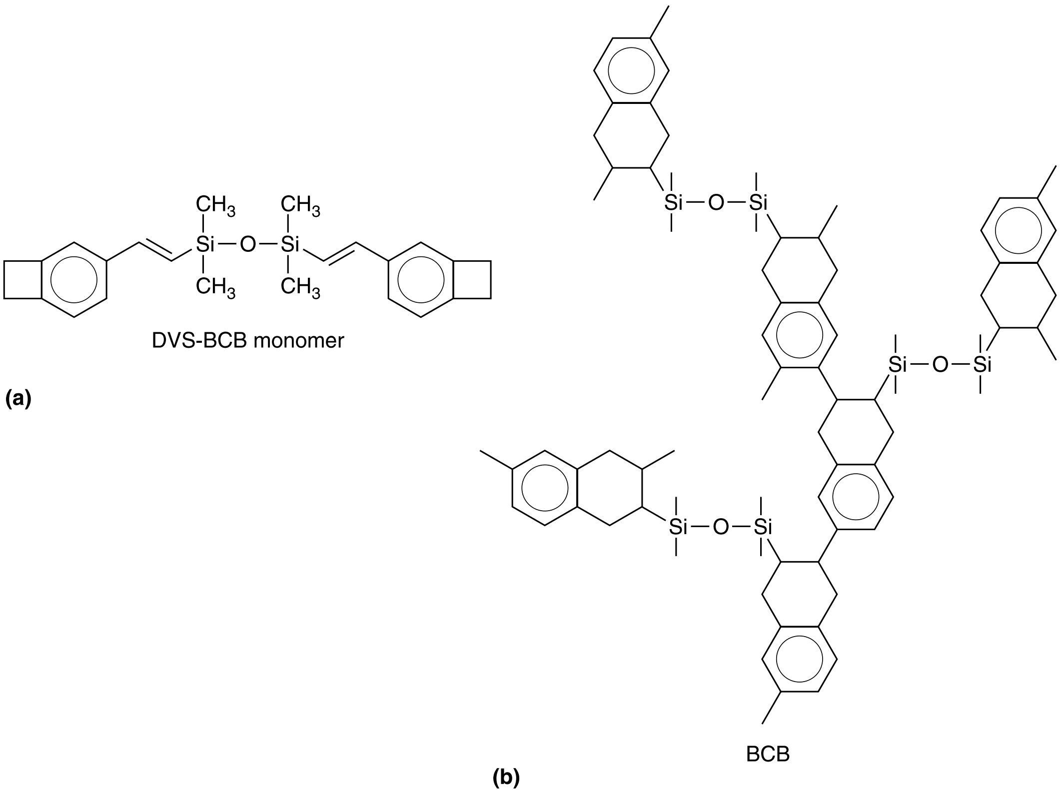

Figure 4.28 Schematic of DVS-BCB: (a) monomer; (b) crosslinked structure.

4.4.8 Bisbenzocyclobutene (BCB)

This is a thermosetting polymer used chiefly as a copolymer with divinylsiloxane (DVS-bisBCB); the coplymer is sometimes referred to simply as BCB. The material has been developed as a spin-on film for interlevel dielectric applications by Dow Chemical Co. as Cyclotene™.

The monomer and crosslinked polymer are shown in Figure 4.28. As seen in Figure 4.28b, the BCB polymer crosslinks during curing forming an isotropic rigid three-dimensional network. There is no evolution of any byproducts. Films with a wide range of solids content and molecular weights can be prepared.

The dielectric constant of Cyclotene™ 5021 is 2.7 and is stable over the temperature range 30 to 190°C. The thermal stability limit upon exposure to air is ~350°C but higher temperatures may be tolerated when the film is capped with SiO_2 (Case et al., 1996).

4.4.9 Polynorbornene

Polynorbornene is a polyolefin; the generic structure is shown in Figure 4.29. The R group can be tailored to provide specific properties, e.g., adhesion and good elongation to break. Varying the composition of R and the number of chains containing it can also affect the dielectric constant.

Alkoxysilane was incorporated as a side chain and improved both adhesion and elongation to break but did increase ε. Thus a copolymer of alkoxysilane norbornnene and alkyl norbornene was synthesized. The flexible alkyl chains lowered the modulus and increased the elongation

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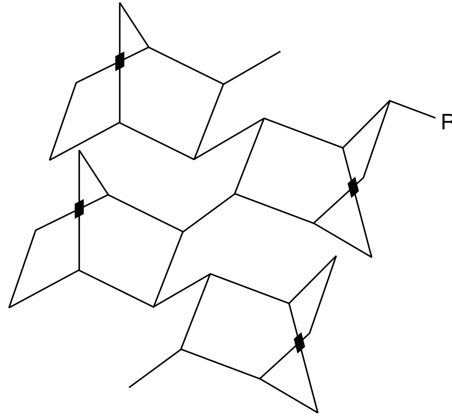


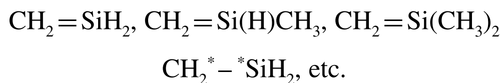
Figure 4.29 Generic structure of polynorbornene.

still further while the improved adhesion was maintained. The stress was about half that of the alkoxysilane norbornene. The value of ε was ~2.5 and the films were isotropic (Grove et al., 1997).

4.4.10 Amorphous Silicon Oxycarbide (α-SiC–O:H)

A schematic of the chemical bonding of this low dielectric constant organosilica film is shown in Figure 4.30. Since it contains a backbone of Si–O–Si as well as organic groups it has also been called an OSG as is MSQ (which is somewhat confusing). Shamiryan et al. (2001) characterized the film as microporous (pore size < 2 nm). The Si–CH_n bridging groups, absent in MSQ, increase the mechanical strength relative to that of MSQ. The range of dielectric constants reported for these films was 2.6 to 3.3. An SiC–O:H film available from Novellus is called Coral™.

A widely used method of film preparation is by PECVD of methylsilanes, $(CH_3)_xSiH_{4-x}$, and an oxidant in a capacitively coupled parallel plate system (Grill and Patell, 1999; Grill et al., 2000; Laboda, 2000a,b; Laboda and Seifferly, 2000; Yau et al., 2000; Wu et al., 2001) and in a downstream reactor (Nara and Itoh, 1997). According to Laboda (2000a) these compound precursors are superior to a mixture of separate C and Si precursors because “film formation occurs via reactions of unique Si–C compounds known as silenes (neutrals) and silylenes (radicals)” generated in the plasma:



$$CH_2{=}SiH_2,\ CH_2{=}Si(H)CH_3,\ CH_2{=}Si(CH_3)_2$$
$$CH_2^*-{}^*SiH_2,\ \text{etc.}$$

so that the incorporation of C into the film is very efficient. The H-content of the films ranges from ~17 to ~30 at% but no OH bonds were detected by IR spectroscopy (Laboda, 2000b). The higher the carbon content of the film, the lower the dielectric constant, stress, and moisture absorption. Laboda (2000a) characterized the lower C-content (<18 at%) film as methyl-doped SiO_2 and the higher C-doped film as silicon oxycarbide (a-SiCO:H) with about equal proportions of C–Si–C and O–Si–O. These films can be etched in F-based plasmas and are compatible with wet cleaning processes. The thermal stability is comparable to SiH_4-based oxides and nitrides and there little stress hysteresis with thermal cycling. The absence of –OH groups may be responsible for their higher resistance to attack by oxygen ashing, relative to other OSG films, but they are susceptible. According to Laboda (2000a) Si–CH_3 bonds are oxidized, forming Si–O–Si bonds so that the films are densified. Furusawa et al. (2001), however, postulated that ashing resulted in porosity with

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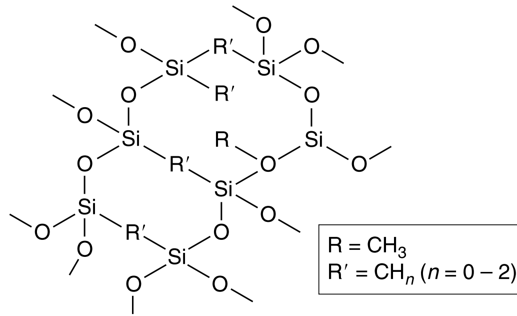

Figure 4.30 Linkages in a generic Si–C–OH material. (Reproduced from Furusawa, T., D. Ryuzaki, R. Yoneyama, Y. Homma, and K. Hinode, *Electrochem. Solid State Lett.*, 4, 631, 2001. With permission of the Electrochemical Society, Inc.)

subsequent moisture absorption; moisture absorption on the sidewalls leads to via poisoning. Whatever the mechanism, ashing results in an increased dielectric constant and a leakier film. Exposure to a low-pressure O_2 plasma forms a thin dense protective oxide.

Lee et al. (2000) found that the dielectric constant increased with increasing RF power; they concluded that ion bombardment decreased film porosity. Shamiryan et al. (2001) reported that a film deposited by the oxidation of trimethylsilane (3MS) with a dielectric constant ~2.7 and refractive index of 1.41 to 1.43 had a porosity of 18%, with 45% of them closed. They also calculated that the refractive index of the film skeleton (pore walls) was 1.53, intermediate between SiO_2 and CVD SiC.

Additional porosity was introduced into a SiOC:H film by etching it in a dilute solution of HF (Shamiryan et al., 2001). The HF appears to etch the bulk of the film slightly, leaving its composition very nearly the same, but to etch the pores isotropically, thereby increasing the porosity. The relative volume of open pores increased with increasing HF exposure.

Silicon oxycarbide films have also deposited by PECVD of methyltriethoxysilane and a nonoxidizing gas (Furusawa et al., 2001). Grill et al. (2000) proposed the use of organsilicon precursors having a ring structure, such as tetramethylcyclopentasiloxane in a continuous or pulsed plasma PECVD process.

Yang et al. (2000) reported that PECVD using SiH_4 and a mixture of hydrocarbon gases (not specified) produced films that were equivalent to those using the organosilanes. Grill et al. (2001) formed a dual-phase film by incorporating C–H bonds into SiC–O:H. Shioya et al. (2000) prepared PECVD films they called porous silica with dielectric constants of 2.6 to 3.0, using hexamethylsiloxane (HMDSO, which has –Si–O–Si– bonds in its molecule) and N_2O.

4.4.11 Diamond-Like Carbon (DLC) Films/Fluorinated DLC

Both hydrogenated DLC and fluorinated DLC (FDLC) have been studied as low-ε films. The films were deposited by PECVD in parallel-plate reactors, DLC from a pure hydrocarbon and FDLC from a fluorocarbon or a fluorocarbon plus hydrogen. The DLC films having low ε were not thermally stable and had high internal compressive stresses. Deposition conditions in which there was higher ion energy bombardment resulted in films containing less H and more crosslinking: higher thermal stability, stress, and ε.

FDLC films with $\varepsilon = 2.8$ were as stable as DLC films with a higher ε and had lower, although still high, stress (< 200 MPa). In order to obtain the low ε, a high F-content is needed, raising concerns about reactions between F and the materials adjacent to the interlevel dielectric. The films lose mass after exposure to 400°C but after a first anneal at that temperature were stabilized against

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further change. Stabilized FDLC films could be prepared to have an ε value <2.5, making them, perhaps, a candidate as an interlevel dielectric (Grill et al., 1998).

4.4.12 Low-*k* Flowfill

This is an extension of the CVD Flowfill™ process with the same gap-fill and planarization features. In this case, H_2O_2 was reacted with methyl silane (CH_3–SiH_3) substituting for SiH_4, to form a methyl-doped silicon oxide. Since the CH_3 group does not react with H_2O_2, it remains bonded to Si within the oxide lattice (McCatchie et al., 1997). The films were annealed in N_2 for 30 min after deposition. The value of ε decreased with an increasing concentration of CH_3 in the film; the minimum value was ~2.7. The density of a film with a high concentration of CH_3 groups was 1.6 g/cm^3 (vs. 2.2 g/cm^3 for the original Flowfill film); this lowered density is a factor in reducing ε. The bonding structure shown by Lu et al. (2002) is that of MSQ. The films were thermally stable to ~500°C. The hydrophobic nature of the film resulted in negligible moisture absorption during storage. The hardness of the film was 2.4 GPa (vs. 12.3 GPa for PECVD SiO_2); this was significantly higher than that of organic and aerogel films. Exposure to an O_2 plasma degraded the film properties significantly; Si–CH_3 and C–H peaks in the IR spectrum decreased dramatically and the oxide network became more like that of a normal CVD SiO_2. N_2 and H_2 plasmas had no affect on the films. McCatchie et al. (1998) reported that the value of ε of this film depended on the base layer (e.g., nitride vs. oxide); a possible explanation for this is a change of structure at the interface (Sermon, 2003).

4.4.13 Trade-Name Films

These are classified in this way because the chemical structures have not been revealed.

4.4.13.1 SiLK

SiLK (a trademark of the Dow Chemical Company) is a spun-on thin-film organic dielectric material containing neither Si nor F. It is an aromatic hydrocarbon, but no further details of its structure are available. The oligomeric solution of SiLK is applied using convention spin-coating equipment and cured at 400 to 450°C in N_2. No catalyst is required for polymerization and no water is evolved in the process. The fully cured films contain little water and preliminary annealing decreases the amount still further; they absorb <0.25 wt% water at room temperature and 80% relative humidity. The content of volatile organic compounds is low but low mass fragments can be thermodesorbed. Thermal desorption is more intense for films cured at 400°C but the desorbing species are the same at both temperatures. At high temperature there is evidence of polymer degradation.

The films are isotropic: $n = 1.63$ and $\varepsilon = 2.65$. The other properties of interest are : $T_g > 490$°C, room temperature CTE = 66 ppm/°C, tensile stress ~ 60 MPa, $E = 2.45$ GPa, and hardness ~ 0.38 GPa. The strength and toughness are almost as high as that of SiO_2. The material flows well, planarizes, and fills narrow gaps (Townsend et al., 1997; Shaffer et al., 2000).

In order to pattern SiLK using RIE in an O_2-based plasma, a hard mask is required. An SiO_2 hard mask, deposited using SiH_4 and N_2O, was the main source of the higher content of water in an SiO_2/SiLK composite than in SiLK. NH_3 was also detected during thermal desorption. A F-based plasma is used to etch the hard mask and the SiLK layer in O_2/N_2. Thermodesorption increased further after these processes. Baklanov et al. (1999) concluded that the desorbed species are mainly from the SiO_2 layer. However, since they are reduced drastically by a short bake ($\geq$350°C in vacuum or N_2) the adsorption does not appear to be an impediment to integration.

Several versions of SiLK are available, SiLK G for gap-fill and SiLK I for damascene application; they have the same polymer base but are dissolved in different solvents. SiLK H was developed more recently to combine the advantages of the previous versions with no degradation of

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its other properties. Deposition of a hard mask, either SiO_2 (TEOS and SiH_4 precursors) or SiN, did not increase ε. The adhesion of the masks was good; there was no delamination after annealing. The dielectric constant was stable up to 450°C; above that temperature it increased, probably due, as indicated above, to decomposition of the organic backbone (Passemard et al., 2000).

4.4.13.2 Black Diamond

Black Diamond is a low-ε PECVD film developed by Applied Materials. It is formed by partial oxidation of an organosilane molecule (not specified) which results in an open network; the density is thus less than that of SiO_2. The film consists primarily of Si and O with a small amount of C. The film properties are: $n = 1.42$, $\varepsilon = 2.5$ to 3.0, tensile stress = 4 to 8 MPa, CTE = 5 to 10 ppm/°C, film thermal conductivity ~ 0.3 to 0.4 that of SiO_2, hardness about half that of SiO_2, thermal shrinkage < 2% at 450°C, acceptable adhesion, crack threshold > 2 mm, and T_g (estimated) > 450°C (Yau et al., 2000).

4.5 BARRIER DIELECTRIC FILM: α-SIC:H

Although included in this chapter, as the title of the section states, α-SiC:H films are *not* used as interlevel dielectrics. They have high dielectric constants compared with SiO_2 and the low-ε films discussed above. However, films of this type have dielectric constants ≤ 5, low compared with Si_3N_4 or plasma SiN, the frequently used barrier/etch-stop film materials (ε ~ 7).

Laboda et al. (1994) described PECVD of α-SiC:H films from organosilicon precursors, silacyclobutane ($H_2CH_2SiCH_2CH_2$, SCB) or methylsilane (CH_3SiH_3, 1MS), using either a 0.125 or 13.56 MHz frequency RF source. The C content of the film deposited from SCB was higher (C/Si > 1) than from 1MS (C/Si < 1), but in both cases it was lower than in the precursor. Thus the lower dielectric constants of the SCB films (~3.7 vs. 4.3) were not surprising. For both precursors, films deposited at the higher frequency had the lower values of ε. The compressive stress and H bond density are comparable to those of plasma SiN films. Dilution of the precursor with Ar resulted in films with higher dielectric constants and refractive indices and less bound H.

More recently, a PECVD α-SiC:H film, named BLOk™ (Applied Materials, Inc.), has been described (Xu et al., 1999). The precursor was an organosilcon gas (not identified). The C/Si ratio in the films was ~1 and the C, Si, and H bonding is given as C–H, Si–H, Si–CH_3, Si–$(CH_2)_n$, and Si–C. The dielectric constant was ≤ 5 and did not change upon annealing at 400°C, the stress was compressive (50 to 150 MPa), and the films are resistant to moisture uptake, cracking, and delamination. No bulk diffusion of Cu into the BLOk™ film was observed. The interfacial region of Cu/BLOk™ is less than 200 Å.

Shioya et al. (2000) deposited PECVD barrier layers, with dielectric constants of 3.2 to 5.0, using hexamethyldisiloxane (HMDSO) and methane (CH_4) or HMDSO + CH_4 + N_2O. As the CH_4 flow rate is increased, the refractive index, density, compressive stress, and Young's modulus increase.

4.6 POROUS DIELECTRIC FILMS

4.6.1 Introduction

Although materials such as HSQ may be considered porous due to the free space generated by bond rearrangements as the resin is cured, here we discuss materials such as xerogels and those in

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which pores are produced in low dielectric constant materials by the use of sacrificial additives. The most important property of a porous material is its density relative to the dense film from which it is derived: $\rho_{rel} = \rho_{porous\ film}/\rho_{dense\ film}$.

The added porosity reduces the dielectric constant. The effective dielectric constant may be modeled as a two-component system consisting of the voids (air) and the connecting material (pore walls). If the structure is modeled as capacitors in parallel and assumes that the pore wall is identical to the dense material, the relationship between P (porosity, i.e., the fraction of the volume occupied by pores which are assumed to contain air) and ε_{eff} is given by

$$\varepsilon_{eff} = (1 - P)\varepsilon_{matrix} + P\varepsilon_{air}$$

Gibson and Ashby (1997) arrived at this linear relationship stating "foaming (i.e., forming a porous solid) reduces the dielectric constant simply because ε scales as the fraction of space filled by the solid." A parallel model appears to be valid for porous HSQ (limited data, see Table 4.6) and for wood (Gibson and Ashby, 1997).

The relationship between P and ε for a series model is given by

$$1/\varepsilon = 1/\varepsilon_{matrix} + (1/\varepsilon_{air} - 1/\varepsilon_{matrix})P$$

Xiao et al. (2001a,b) compared the parallel and series models for an aeogel. The parallel model required some modification but (as others had found) the series model did not appear to be at all applicable. They presented an empirical relationship $\varepsilon_{eff} = 3.99 - 3.86P + 0.89P^2$ for films assuming $\varepsilon_{SiO2} = 4.0$ (with slightly different constants for other values of ε_{SiO2}) and showed agreement with measured values. They found porosity the major factor to affect ε_{eff}; pore shape, size, and distribution had only a small effect.

The porosity of the film can be calculated using the Lorentz–Lorenz equation:

$$P = 3(n_d^2 - n_p^2)/(n_d^2 - 1)(n_p^2 + 2)$$

where n_d and n_p are the refractive index values of the dense and porous versions of the film.

The assumption that the pore walls and the dense film have the same properties (density, refractive index, dielectric constant) may be invalid. In the case of xerogels, for example, the density of the pore walls has been found to be ~40 to 50% lower than bulk SiO_2 (2.26 g/cm^3) (e.g., Smith et al., 1995; Wu et al., 2000; Murray et al. 2002). Agreement between experimental values of the dielectric constant and those calculated assuming a higher density for the pore walls than that found experimentally may possibly be explained by the presence of polarizable species on the internal pore surfaces (Jo et al., 1997).

Although SEM and TEM have been used for pore size determination, more reliable methods for characterization of the structure of porous films are Rutherford backscattering (RBS), forward recoil scattering (FRES or ERD), specular x-ray reflectivity (SXR), small-angle neutron scattering (SANS), positronium annihilation spectroscopy (PALS), and ellipsometric porosimetry (EP), described in Chapter 2. Jo et al. (1997) reported that the distribution of pores in a xerogel film was completely random with respect to an applied electric field.

Unfortunately, the elastic modulus (E) is usually reduced even more drastically than the dielectric constant:

$$E_{eff}/E_{matrix} = (\rho_{rel})^n$$

The value of n for porous silica (xerogels) is ~3.5 (Gross et al., 1993). Approximately the same value applies to porous HSQ films (see Table 4.6). Ma et al. (2000) compiled values for n for a variety of aerogls; n varied from 2.6 to 3.7. They developed a computer model for perfectly connected structures and arrived at a value of n which they applied to aerogels. They suggested that the "high value for the exponent (~3.6) was largely because of a reduction in the connectivity of the material with decreasing density."

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Table 4.6 Properties of a Series of Porous HSQ Films

Dielectric Constant	1.6–1.8	1.9–2.1	2.0–2.3	2.5–2.6
Density (g/cm^3)	0.62	0.9–1.0	1.1	1.2
Pore size[a](Å)	39	20–24	17–20	—[b]
Porosity (%)	>60%	56–60	45–55	25
Modulus[c] (GPa)	0.5–1.7	2.0–3.0	3.0–5.0	6.0–10.0

[a] Determined by SXR + SANS.
[b] Poor scattering; pore size not determined.
[c] Determined by nanoindentation.

The model of Gibson and Ashby (1997, 2000) predicts $n \sim 2$ for open-cell porous material and showed the agreement between this model and the results obtained by several investigators for a variety of films. Ma et al. state that "$n = 2$ is valid only when the connectivity remains unchanged upon variation of the density."

Gibson and Ashby (1997, 2000) also modeled the relationship between E and ρ_{rel} for closed cells:

$$E_{eff}/E_{matrix} \sim \phi^2(\rho_{rel})^2 + (1 - \phi)\rho_{rel}$$

where ϕ is the measure of the amount of material in the cell strut vs. cell face. For an open cell, $\phi = 1$.

Thus, whatever model describes a given system, E is degraded significantly and CMP processing is compromised. The ability to withstand stress without cracking is also reduced. However, the stress in the porous films is lower than in the initial dense material.

To reduce the impact on mechanical properties when striving for a very low dielectric constant, i.e., to minimize the needed porosity, the matrix itself should be a material with a low dielectric constant. As emphasized by Siew et al. (2000b) "the porosity should be no higher than needed to achieve the dielectric goals."

It is generally agreed that the pores should be small and tightly distributed in size. Closed pores are preferred to limit the incursion of ambient substances and improve mechanical stability but it is not clear just how this structure can be guaranteed. There is disagreement about whether it is porosity itself or the size, shape, and connectedness that determine the ultimate dielectric constant.

As holes are etched into the porous films, pores in the sidewall are exposed to the volatile etchants and etch products interconnect the porous network. The impact of an opening into the sidewall on the stability of the bulk of the film has not been discussed in the literature. The integrity of a thin barrier metal lining the sidewalls may be compromised due to the open pores (Sun et al., 2001).

4.6.2 Silica Xerogels

Silica xerogels are usually prepared by the hydrolysis and condensation of alkoxysilanes, most often TEOS, during which Si–O–Si bonds are formed, eventually evolving into a three-dimensional open network of silica walls. The dielectric constant of these nanoporous films, consisting of SiO_2 and air, has been reported to be less than 2. The sol is spun onto a wafer and after gelation has occurred the liquid in the gel is removed. When the liquid is removed above its critical temperature and pressure (supercritical drying) the film is called an aerogel. When the liquid is removed by simple evaporation, it is called a xerogel (Gesser and Goswami, 1989). Ambient drying has entirely replaced supercritical drying for film formation for semiconductor devices because it is simpler, less hazardous, and cheaper. It has often been inferred that these films are simply a mixture of SiO_2 and air, i.e., the pore walls are identical to bulk SiO_2. However, as indicated in Section 4.6.1, the skeleton density has been found to be significantly lower.

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Several xerogel films, the Nanoglass™ series, are available commercially (Honeywell Electronic Materials).

The processing steps when using an alkoxysilane precursor include hydrolyzing the sol in the presence of a catalyst, spinning, gelation of the spun-on film, aging, surface modification, and drying. There are many recipes in which different precursors with different solids content, shrinkage-prevention schemes, processing times, etc., are used.

Initially the precursor was dissolved in a mixture of water and ethanol but Smith and Ackerman (1998) proposed adding a higher boiling point (slower evaporation rate) solvent, such as ethylene glycol to the mixture. The catalyst may be an acid (e.g., HCl), a base (e.g., NH_4OH), or as described by Gnade (1995), a two-step acid–base process. A solvent-saturated atmosphere is often used during spinning to prevent rapid evaporation which would result in film shrinkage (low porosity) and tensile stress buildup (cracking and/or delamination) but the use of a glycol may make this precaution unnecessary. The use of a glycol also improved the mechanical strength of the final xerogel film. Gelation time depends on the temperature, choice of catalyst, and catalyst concentration. Aging that follows increases the ability of the film to withstand the capillary pressures forces during drying and thus controls shrinkage and increases the mechanical strength of the film (Jin et al., 1998). Several procedures for aging the wet film have been described. In one, the wafers were stored in an atmosphere saturated with ethanol for one day at 37°C (Gnade et al., 1995) or the wet gel was kept at 50°C for one day and then at 100°C for another day (Deshpande et al., 1996). In another, the gels were held at a slightly elevated temperature in a solution of NH_4OH and ethanol for times between 30 minutes and 24 hours (Nitta et al., 1998, 1999). According to Nitta et al., a longer aging time results in a higher porosity and lower dielectric constant, but if it is too long the porosity decreases. An enhanced aging process that was completed in less than an hour was described by Smith et al. (1998). The wet gel thin film was kept in an atmosphere of saturated water vapor at a temperature above the boiling point of the low-boiling-point pore liquid to replace it with water and then the temperature was raised to > 100°C and the pressure to > 1 atmosphere for less than one hour. For example, saturated steam at 2.3 atm and 125°C aged a wet gel film in ~5 minutes. An aging catalyst such as NH_3, HF, NaOH, or methylamine may be added to the water vapor.

After aging, the film is treated with a surface-modifying (silylating) agent (Smith et al., 1995; Deshpande et al., 1996) to replace the surface Si–OH groups by inert CH_3, making the film resistant to moisture absorption. Trimethylchlorsilane (TMCS), hexamethyldisilazane (HMDS), and methyltrioxysilane (MTAS) have been used for this purpose. The Nanoglass™ employing HMDS has been labeled K2.2A10, that employing MTAS K2.2-A10C (Case et al., 2000). However, the extent of silylation must be limited to prevent excessive filling of the pores with organic species, thereby increasing the dielectric constant (Nitta et al., 1998, 1999). Excess surface modifier is removed by a solvent-exchange step. The film is then dried.

Thus these xerogel films, although often called porous silica, are not pure SiO_2 (and air). C, from the CH_3 groups deposited by the modifier on the inner pore surfaces, is detected by RBS; there may be organic contaminants from the precursor material as well. For example, the composition of a xerogel (porosity 58%, pore size 10 to 15 nm, $\varepsilon = 2.2$) was $SiO_2(CH_3)_{0.3}$ (Standaert et al., 1999). Smith et al. (1995) reported that the skeletal density of a xerogel film (as well as the bulk density) decreased as the concentration of the modifier (TMCS) increased until saturation is reached.

Cho et al. (1996) described an alternative process. The wafers are heated to a temperature between 100 and 400°C and the OH groups removed by exposure to H_2 or forming gas. This step is followed by baking in a F-containing atmosphere to bond F to the pore walls to improve the dielectric properties.

Ramos et al. (1998) reported a nanoglass process in which the steps of deposition (< 30 sec), edge bead removal (< 15 sec), gelation, aging, and silylation (<120 sec), and hot-plate bake to remove pore fluid (< 120 sec) fulfilled the requirement that the throughput of coaters be of the order of 60 wafers/hour. However, no details were given.

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After the xerogel process is completed, the final step is the deposition of a cap layer, usually a PECVD SiO_2 layer. Shulz et al. investigated the effect on the xerogel film of exposure to SiH_4 and N_2O during SiO_2 deposition 300°C and found that the N_2O did not remove the CH_3 groups introduced during the silylation process. Deposition of the cap layer had negligible effect on the dielectric constant, leakage current, or breakdown voltage of the xerogel films. However, if TiN was deposited directly on the xerogel film, the dielectric constant was increased.

The films are thermally stable but exposure to an oxygen plasma during ashing results in film shrinkage. Kondoh et al. (1998) attribute this to the fact that O_2 can readily penetrate the open network and remove the hydrophobic groups introduced during silylation; the resulting hydrophilic silica capillary surfaces aggregate spontaneously. This easy penetration also can explain that fact that the etch rate in an NF_3 afterglow, compared with that of thermally grown SiO_2, was much greater than expected from the difference in density.

Hendricks et al. (2002) expanded the choice of precursor for spin casting and gelling beyond the usual TEOS. Precursors consisted of a tetrafunctional alkoxysilane with at least one mono-, di-, or trifunctional alkoxysilane, acetoxy, or halogen-based silane, in a mixture of water and an organic solvent. In another process HSQ replaced the tetrafunctional precursor. The wet gelled film is aged in an acidic or basic vapor and the surface modified to make it hydrophobic. They also suggested the use of a silicon-based polymer precursor for coating the nanoporous dielectric film.

Photoinduced growth of a xerogel was proposed by Zhang and Boyd (2000). After spin coating, the film is exposed to 172 nm UV radiation in pure xenon to decompose the organic compounds in the sol–gel and convert it into the xerogel. No processing time for complete conversion was given. The dielectric constant of the film was a function of the substrate temperature: $\varepsilon = 3.30$ at 200°C, decreasing to 1.70 at room temperature.

Gnade et al. (1996) patented a process in which the porosity is varied in the vertical direction using two or more solvents of differing volatility or using two or more precursor solutions and applying and gelling them sequentially.

Bruinsma et al. (1997, 1999) formed mesoporous films by spin coating an aqueous solution of a silica precursor (TEOS) and a templating surfactant (cetyltrimethylammonium chloride, CTAC) and drying rapidly. The final step was calcination at 550°C. It was claimed that the pores are ordered and of a controlled size (~2 nm), determined by the silica to surfactant ratio. With CTAC/TEOS = 0.21, the film porosity was ~64%. A highly porous film had a refractive index of 1.16 indicating low values of ε are likely. The calcination temperature of 550°C is incompatible with IC processing, but it is likely that a more suitable surfactant can be found.

A different colloidal sol–gel spin-coat process using colloidal silica, potassium silicate, and formamide was proposed by Birdsell and Gerhardt (1998). It required no special precautions during gelling. After gelation the film was leached in deionized water to remove the alkali ions and then dried. Increasing the amount of colloidal silica decreased the pore size, dielectric constant (to ~2), and the dielectric loss. However, there appears to be no further work in this direction.

The density (porosity) of the film on which the refractive index, dielectric constant, thermal conductivity, and mechanical strength depend is a function of all the processing variables. Porosity (P or π) values of ~50 to 90% a have been reported, with dielectric constants as low as ≤ 2. Typical values of E for such films are 2.5 to 4 GPa ($E_{SiO2} = 72$ GPa), consistent with a scaling factor of ~3.5. A scaling factor of 3 to 4 has been reported by several investigators (e.g., Smith et al., 1995; Moner-Girona et al., 1999). Using EP, Kondoh et al. (1998) determined that the average pore size of a xerogel film with a porosity of 67% was ~5 nm; the pore sizes were tightly distributed and the pores were interconnected. As the film density is decreased (porosity increased) pore sizes increased (Jin et al., 1997; Ramos et al., 1998; Gidley et al., 1999; Murray et al., 2002). Jin et al. also noted that the smaller pores were more tightly distributed. Wu et al. (2000) investigated a Nanoglass™ K.2.2A10B film ($\varepsilon = 2.2$) using SXR and SANS. They determined the pore wall density of a film with a porosity of ~53% was 1.16 g/cm^3. The average pore size was 6.5 nm and ~22% of them had

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connective paths to the surface, as opposed to the total interconnection reported by others. The CTE was determined to be 60 ± 20 ppm/°C. Murray et al. (2002) studied a range of xerogel films using SAW, EP, RBS, and nanoindentation. Values of ε ranged from 1.7 to 2.3, porosities from 36 to 55% (all pores interconneced), and mean pore radii from 2.2 to 4.2 nm, and the density of the skeleton was 1.4 g/cm^3. Smith et al. (1995) reported a wall density of 2.08 g/cm^3 for a xerogel whose bulk density was 0.42 g/cm^3.

Differences in processing undoubtedly account for the variations in the results reported by different investigators. The etch rates of xerogel films in a CHF_3 ICP increased with increasing porosity, but when normalized with respect to porosity the rates were higher than that of dense SiO_2. This suggested that CHF_3, trapped in the pores, increased the etch rate (Jain et al., 1999).

The thermal conductivity of xerogels is very low, approximately one hundredth of that of SiO_2 (Sinha, 1997; Iguchi et al., 1998). Jin et al. (1997) stated that xerogels have a higher thermal conductivity than polymer dielectric films but this is not always a valid comparison. The differences among these films depend on the porosity of the xerogel and the nature of the polymer.

They adhere well to Si and deposited SiO_2 films. As expected, diffusion of Cu through these films is orders of magnitude faster than that in bulk SiO_2.

4.6.3 Organically Modified Xerogel

A film was prepared by mixing ethanol sols of acid-catalyzed TEOS and base-catalyzed MTES (methyltriethoxysilane). The sols were hydrolyzed for a day before mixing, spun on in the ambient atmosphere, baked at 100°C, soaked in an HMDS/toluene mixture, and finally cured at 450°C in air and 400°C in N_2. The film consisted of highly porous clusters (due to base catalysis) in a dense matrix (acid catalysis) with a hydrophobic surface (HMDS). The dielectric constant decreased and the porosity increased as the MTES/TEOS ratio increased; the lowest value was ~2 with a porosity of ~57%. The porosity was calculated from the ratio of the SXR-determined density to the density of dense silica. The existence of a C–Si bond and a CH_3 unit and the very low concentration of water were determined by FTIR. A pore size of <10 nm and the possibility that the pores were closed were deduced from TEM micrographs (Yu et al., 2002).

4.6.4 Porous HSQ

Voids have been introduced into HSQ by adding a high boiling point solvent to the resin (e.g., Moyer et al., 1999; Donaton et al., 2000; Iacopi et al., 2001, 2002). After coating, the solvent-rich film is subjected to ammonia and moisture so that the film gels in the presence of the solvent. After gelation, the temperature is raised and the solvent removed leaving a silica-like film containing mesopores (defined by IUPAC as pores 2 to 50 nm in size). The pore volume can be controlled by the amount of high-boiling solvent incorporated into the resin. A final cure is needed for full crosslinking within the film. The ratio of ammonia to water and the (undefined) chamber conditions determine the best treatment time. As the treatment time increases, the modulus increases, the Si–H content decreases, and the refractive index decreases and then rises. A compromise must be reached between the improved mechanical properties and the decreased resistance to moisture due to the loss of Si–H. Properly cured films exhibit good resistance to moisture uptake and are thermally stable. The resulting film is said to be more crack resistant, has a modulus of 2 GPa, and a lower tensile stress than dense HSQ (~20 MPa). A 50% porous HSQ film made by Dow Corning (called XLK™) has a dielectric constant of ~2. The pores in XLK™, measured using EP and PALS, are uniform, 4 to 5 nm in size, and are interconnected (Iacopi et al., 2002).

Deis et al. (2000) prepared a series of porous HSQ films by varying the ratio of solvent to resin. Some of their results, showing the decrease in density and modulus and increase in porosity and pore size with decreasing dielectric constant, are given in Table 4.6.

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The interconnected pore structure reduces the resistance of the film to CMP processes and increases its sensitivity to plasma exposure during etching and resist stripping, to wet chemicals, and to penetration by barrier layers (Sun et al., 2001). The film porosity decreases after exposure to hydrogen and oxygen plasmas. After exposure to a C_2F_6/H_2 plasma, the adsorption/desorption isotherm indicated reduced pore volume; it was postulated that fluoropolymer was deposited in the pores.

Several PECVD films were used to seal the pores of the XLK™ films.

The precursors of the capping films can diffuse rapidly through the pores and modify the film. SiO_2 deposition requires an oxidizing plasma in which Si–H bonds may be oxidized, making the film susceptible to an irreversible moisture uptake if not completely sealed by a thick SiO_2 layer deposited using a low N_2O flow. However, there is evidence of slow moisture absorption through the sides of a groove opened in such an SiO_2-capped stack indicating, perhaps, diffusion of oxidizing species through the pores during capping. The moisture is desorbed to a large extent by short anneal at 450°C. When SiC:H (see Section 4.5) is used as a capping layer, C-containing bonds are detected in the top 1000 to 1500 Å of the XLK film. This suggests that the precursor reactants penetrated and diffused into the pores during deposition of SiC:H, partially closing the ones at the surface. There are also more Si–H bonds; together with the $C–H_x$-like bonds, the result is enhanced hydrophibicity. No moisture is absorbed through the sidewalls of a groove etched into such a composite film, indicating that while the XLK film is extremely susceptible to oxidation it itself is hydrophobic (Iacopi et al., 2002).

Another process involves the use of a porogen, a sacrificial material, bonded to the HSQ resin and thermally decomposed to form voids (pores) in the final product. Polybutadiene was chosen as a porogen by Siew et al. (2000b). The thermal treatment involves three processes: decomposition of the porogen, diffusion of the byproducts through the matrix, and curing of the matrix. It must be tailored to prevent the formation of percolation pathways (which form if the gas pressure in the pores exceeds the strength of the matrix, i.e., if the decomposition product formation is much greater than the rate of diffusion) with an instantaneous weight loss. A two-stage process consisting of a 10°C/min ramp to 400°C (held for 30 min) followed by an increase to 450°C at 5°C/min (held for 1 h) prevented the pressure buildup while the HSQ continues to cure. The pore size was ~50 nm.

4.6.5 Porous MSQ

Several processes have been developed to increase the porosity of MSQ films in order to lower the dielectric constant. They all involve the use of porogens.

One porogen used to template pores into MSQ is a polymer, a six-arm star poly(caprolactone) (PLC) (Remenar et al., 1998; Nguyen et al., 1999). A solution of the MSQ and porogen is spun onto the wafer and cured to form a highly crosslinked hybrid which is decomposed at elevated temperature (430°C for 2 h in N_2). As the fragments diffuse out of the matrix, a porous film results. The porosity increases and the dielectric constant decreases with increasing porogen in the hybrid. Below 25 to 30 w/w porogen, the films were reported to have a closed-cell structure and the pore size was estimated to be ~20 to 25 nm. At greater porogen loading, the increasingly interconnected pores collapsed and phase separation occurred so that no further improvement was possible. The lowest dielectric constant obtained was 1.9 to 2.1. The surfaces of the pores are hydrophobic and the films exhibited a high breakdown strength.

Gidley et al. (2000), using PALS, described the films as having a "complex, partially interconnected, pore structure" and there is a bimodal pore distribution of small pores (~1.5 and 3.5 nm).

Substituted norbornene polymers have also been used as sacrificial porogens to form pores in MSQ films. The cure cycle was: hot plate, 2 min at 180°C, 1 min at 250°C, furnace cure in N_2, ramped at 3°C/min to 425°C for 1.5 h. The pore size, determined by TEM, was reported by Kohl et al. (1999) to be 70 nm and by Padovani et al. (2001) to be 5 to 20 nm and nearly spherical and

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closed. The dielectric constant was reduced from 2.7 to 2.2 for a film prepared with 30% loading of the porogen. The porous films were significantly more resistant to crack propagation but the modulus and hardness were reduced. The concentration of porogen affected the number of pores but not their size.

Ryan et al. (2001) demonstrated that these mesoporous films were more readily damaged during integration processing than the nonporous films made with the same precursor.

When a composite of MSQ and a triblock polymer, poly(ethylene oxide-b-propylene oxide-b-ethylene oxide (PEO-b-PPO-b-PEO), is heated slowly to >400°C, the MSQ matrix is first cured and then the block polymers are calcined, generating pores. The dielectric constant of the resulting film depends chiefly on the amount of copolymer in the composite; with 30%, the dielectric constant is ~2.0. Higher curing temperatures (e.g., 500°C) and the use of higher molecular weight MSQ as the starting material result in improved mechanical properties but the mechanical properties of the original MSQ are degraded. The pore size and pore structure depend on the properties of block polymer although the dielectric constant of the film does not; it is determined by the porosity. The pore structure (open or closed, shape, and size) of the various films was not described, although it was postulated that these factors may affect the breakdown strength of the film (Yang et al., 2001).

Bauer et al. studied thin films of porous MSQ films (porogen not specified) using RBS, FRES, SXR, and SANS. The porosity and pore size were determined by SANS and the connectivity by changes in SANS when samples were placed in solvents that can penetrate open and interconnected pores. Some of their results are given in Table 4.7.

Liu et al. (2002) discussed a porous OSG based on MSQ which has CH_n ($n = 1, 2$) groups bridging the siloxane matrix (Chemat Technology, Inc.). The porosity was 50% and $\varepsilon = 1.9$. To suppress O_2 ashing damage the film was first exposed to an H_2 plasma to passivate the porous inner structure, then ashed, and finally exposed to trimethylchlorosilane in which Si–OH groups are replaced by inert Si–CH_3 groups (Liu et al., 2002).

4.6.6 Porous Poly(aryl ether)

A PAE solution in cyclohexanone was modified by adding a specially prepared organic solution (not identified); after aging for one day, the mixture was spun onto the wafer, soft-baked for solvent evaporation and partial polymerization, with final curing at 400°C in air for an hour to form closed pores. The dielectric constant of the porous PAE was 1.9 and was stable during prolonged exposure to air. The film stress was tensile (80 MPa) and no hysteresis was observed during thermal cycling; the CTE was larger for the porous film than for the dense PAE, and $T_g > 350°C$. XTEM was used to evaluate the structure of the film. The typical pore size was ~3 nm and small pores tended to aggregate and form bigger pores; the porosity was ~40% (Tsai et al., 1999).

Nanoporous PAEs offered by Schumacher/Air Products, Velox-ELK™ and PolyELK™, have been described by O'Neill et al. (1999) and Markley et al. (2000). The parent polymer is structurally

Table 4.7 Properties of Thin Films of Porous MSQ

Sample	Density[a]	Density[b]	Porosity	Connectivity	Wall Density[c]	Pore Size (Å)
1	1.016	1.082	0.20	1.07	1.35	27
2	0.850	0.939	0.26	0.57	1.266	49
3	0.852	0.833	0.33	0.55	1.234	61
4	0.689	0.727	0.37	0.23	1.55	62

[a] Mass density: RBS/FRES.
[b] Mass density: SXR.
[c] Wall density: SXR/SANS.

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similar to that of Velox™ but the cure temperature is lower. The pores are produced by introducing a developer during the spin process. The films are soft-baked at 200 to 300°C and then cured under N_2 to 425°C for < 5 min. The pores were closed (PALS). There was a dense surface layer and after a transition to a porous layer, the pore size increased slightly with depth. The properties of both films are similar. The value of ε for a film of > 30% porosity was < 2.0, the pore size ~ 20 nm, $T_{gVelox\text{-}ELK} > 425°C$, $T_{gPolyELK} > 490°C$, the thermal stability and adhesion acceptable, and E was estimated to be > 2 GPa.

4.6.7 Porous SiLK

The porosity of SiLK was increased by the incorporation of solid organic porogens with subsequent heat treatment (Shaffer et al., 2000). The thermal degradation temperature determined the choice of the porogen. The dielectric constant used to evaluate the effect of porosity on the mechanical properties was calculated using the series model.

4.6.8 Polyimide Nanofoams

These materials were prepared from block copolymers, one of which, the dispersed phase, was thermally labile. The size and shape of the pores corresponded to the morphology of the initial copolymer. Thin films of the foamed material had high thermal stability and a dielectric constant approaching 2 (Carter et al., 1995a).

4.6.9 Porous Silicon Oxynitride

The precursor for this spin-on film was perhydropolysilazane (PPSZ) solution plus acrylic polymers (for foaming, i.e., for forming a porous structure) and aluminum ethylacetoacetate (catalyst promoting the oxidation of PPSZ after a prebake). The film structure was tailored by altering the amount of catalyst.

The process flow was (1) precursor preparation, (2) spin-on, (3) ramp-up prebake on hotplate to 300°C (< 10 min total), and (4) N_2 furnace cure at 400°C for 30 min. From spin-on to final cure, the processing time was about 1 hour. The composition is Si/O/N/C = 40/55/5/0.5 at%. The film structure was an aggregate of small granules of 5 to 30 nm in diameter. The films were resistant to moisture absorption; ε increased slightly during the first days of exposure to room air but then remained unchanged for long periods. The density of the film was controlled by the acrylic polymer loading; the tensile stress and dielectric constant increased with increasing density. For a film of density of 0.78 g/cm^3, the refractive index was 1.12, $\varepsilon = 1.6$, tensile stress was 17.5 MPa, and crack resistance was $\gg$5 μm.

4.6.10 Interpenetrated SOG (IPS)

This film has also been described as a hydrogen methyl siloxane-based porous SOG.

These low-density films were prepared by the hydrolysis of a SOG precursor and silica in the presence of an organic oligomer (neither the SOG nor oligomer was given). After an anneal at 400°C in N_2 no OH groups were detected by IR, indicating that the pore surfaces were hydrophobic. The films were studied using N_2 adsorption, EP, SANS/SXR, and PALS. As the film density was decreased (from ~1.5 to 0.6 g/cm^3) the dielectric constant decreased and the average pore size (measured by N_2 adsorption) increased from ~2.5 to ~7.7 nm, and the stud-pull strength decreased (from ~70 to 10 MPa). The steepest changes occurred as the density was lowered below ~0.7 g/cm^3. The average pore size distributions were relatively narrow but the spread increased as the pore size increased. The pores were found to be nominally fully interconnected (Muraguchi et al., 1999; Kondoh et al., 2001).

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4.6.11 Orion™

The film is deposited in a PECVD system with additional curing for stabilization. Neither precursors nor process conditions were given. The composition of the film was given as Si (20.5):C(14.5):O(31):H(34) with a porosity of ~20% with a pore size of 1 to 4 nm. The value of ε was 2.16, increasing to 2.31 after a 600°C anneal. The film adhered well to TaN which was not driven into the film under bias as were Al and Cu (Fang et al., 2002).

4.6.12 Air Gaps

Several schemes have been proposed in which air gaps are formed between the metal lines to reduce the intralevel capacitance to its lowest level since this is the major contributor to RC delay for very closely spaced conductors (Anand et al., 1997; Shieh et al., 1998, 1999; Kohl et al., 1998; Bhusari et al., 2000; Lin et al., 2000). Since the capacitance of the interlevel dielectric is less of a factor in the RC delay, a standard dielectric can be used to sandwich the air gaps for structural integrity and thermal conductivity.

Shieh et al. (1998, 1999) depended on the poor gap-fill capability of a PECVD SiO_2 process to produce the voids and SiO_2 as the full thickness interlevel dielectric for structural integrity and thermal conductivity and reported a 40% reduction in capacitance when compared to a full SiO_2 structure.

Arnal et al. (2002) relied on the poor gap-fill property of SiH_4-based PECVD SiO_2 deposition to form voids. They pointed out the need to encapsulate completely the air gap in SiO_2 to prevent penetration into the gap during subsequent processing. Therefore, the gap was capped by TEOS-based SiO_2 which fastened the air gap not far above the metal lines. They reported a reduction of 50% in the parasitic capacitance between adjacent lines.

Anand et al. (1997) proposed forming the gaps by depositing carbon by sputtering and after trench etch, metal deposition, and planarization, forming a thin bridge layer of sputtered SiO_2, and finally removing the carbon by ashing in a furnace at 450°C for 2 hours in an O_2 ambient. The bridge layer has to meet several criteria: it must withstand the ashing temperature, must not react with the carbon during deposition or ashing, and must be thin and have a low dielectric constant. The effective dielectric constant of a structure using a bridge layer of sputtered SiO_2 ($\varepsilon = 4.2$) $<$ 50 nm thick was calculated to be 1.2. The manufacturability and stability of such a structure are questionable. In addition the extremely poor thermal conductivity of air contributes to the increased temperature of longer wires.

As pointed out by Bhusari et al. (2000), the size and shape of voids resulting from poor gap fill are limited. They also depend strongly on the line-to-line spacing. The use of a sacrificial thermally decomposed polymer was proposed by Kohl et al. (1998). The spin-on polymer was polynorbornene with the monomer functionalized with a triethoxysilyl group for improved adhesion and possibly a controlled rate of decomposition. The polymer/metal structure can be formed by a damascene process or by coating the polymer over etched metal lines. The overcoat was PECVD SiO_2 deposited at 200°C. The encapsulated polymer was decomposed in N_2 using a heating protocol with a final temperature of 400°C; the residue (C, O, Si) was estimated to be ~100 Å thick. The decomposition products diffuse through the overcoat at a rate controlled to prevent rupture of the overlying oxide. The oxide thickness used was 5 nm, too thick for use in ICs; it is not clear whether that was done for the purpose of demonstrating how readily the decomposition products out-diffuse or whether this thickness was needed for mechanical support.

The effective dielectric constant (ε_{eff}) of an air gap encapsulated between parallel metal lines was simulated for two aspect ratios and several overcoat thicknesses as a function of the dielectric constant of the overcoat (Figure 4.31). It was concluded that it would be difficult to drop ε_{eff} below 2.0 using fully densified SiO_2 and an air gap. To accomplish this an overcoat with a lower ε is required.

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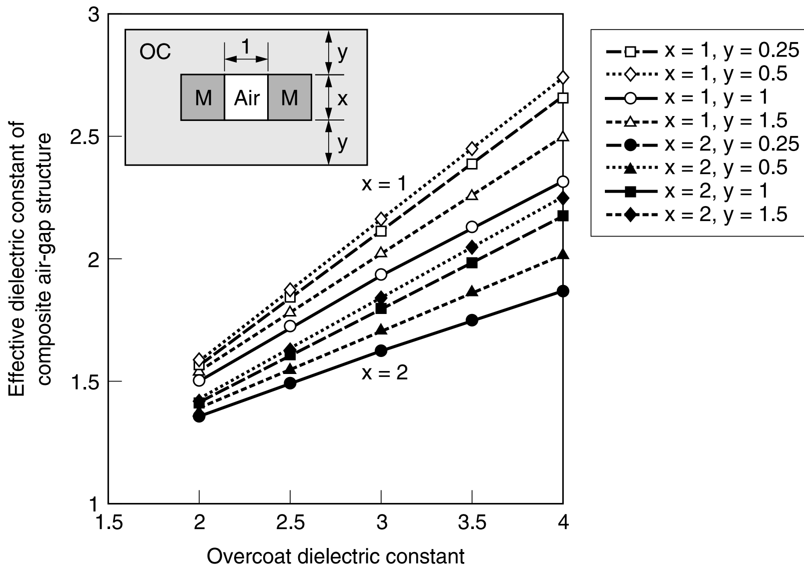

Figure 4.31 Effective dielectric constant of composite air-gap structures vs. dielectric constant of the overcoat. (Reproduced from Kohl, P.A., Q. Zhao, K. Patel, D. Schmidt, S.A. Bidstrup-Allen, R. Shick, and S. Jayaraman, *Electrochem. Solid State Lett.*, 1, 49, 1998. With permission of the Electrochemical Society, Inc.)

Similar results were obtained by Bhusari et al. (2000) using a copolymer of butylnorbornene and triethoxysilylnorbornenene as the sacrificial polymer.

4.7 PLASMA-ASSISTED ETCHING OF ORGANIC FILMS

The earliest use of plasma-assisted etching of an organic layer in O_2 was stripping (ashing) photoresist in a high-pressure, isotropic barrel (tunnel) reactor The conditions are such that there is essentially no ion bombardment of the substrate; resist removal at relatively low temperature (i.e., no external heat) is the result of the spontaneous (thermally activated) reaction between the organic material and species generated in the plasma, which according to Steinbruchel et al. (1986) is chiefly O atoms.

The introduction of the directional low-pressure RIE systems made it possible to use an O_2 plasma to etch patterns into organic films. One early application was etching vertical-walled features into the underlayer of a multilevel mask structure (e.g., Moran and Maydan, 1979), described in Chapter 1, Section 1.5.8.8. Another was etching vertical vias in polyimide, the earliest organic interlevel dielectric (e.g., Soller et al., 1984). Still another was forming an undercut profile in the hard-baked underlayer of a trilevel mask for lift-off metallization (Franco et al., 1975) described in Chapter 5, Section 5.6.4.1. To prevent or minimize undercut, low pressure (e.g., 0.5 Pa; Soller et al., 1984), low substrate temperature (e.g., about –30°C, Namatsu, et al., 1982; –75°C, Etrillard et al., 1994), or both (e.g., Namatsu et al., 1982) were reported to be necessary. These conditions appear to be reasonable since O_2 can etch an organic material spontaneously (i.e., isotropically). The concentration of reactive neutrals is decreased and the energy of the (directional) ions is increased at low pressure and the spontaneous etch rate is reduced at low temperature. Deposition of reaction byproducts on the feature walls has also been invoked to account for anisotropy (e.g., Pilz et al., 1990).

Higher pressures were used to obtain the undercut profile of a lift-off stencil.

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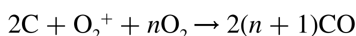
As reactor design advanced, RIE of organic films was carried out in dual-frequency (e.g., Janowiak et al., 2000), magnetically enhanced (Pilz et al., 1990), and high-density systems (e.g., Joubert et al., 1989; Carl et al., 1990; Juan and Pang, 1994). Ion (Vanderlinde and Ruoff, 1988) and neutral (Panda et al., 2001) beam systems have been used to elucidate mechanisms.

Evidence has been offered that the structure of the polymer influenced its etch rate in O_2. Wrobel et al. (1988) correlated the etch susceptibility with the degree of unsaturation; Lamontagne et al. (1991) found that aromatic polymers were resistant to etching in an O_2 plasma.

Organic films can also be etched in H_2 (Robb, 1984) and N_2/H_2 plasmas (Fuard et al., 2001a); CH_4 is a possible volatile etch product. Anisotropy in H_2 can be achieved at pressures much higher than those required in O_2 but the rates are substantially lower. An ion-assisted mechanism was proposed.

There is disagreement over whether O (atom) or O_2 (molecule) is the etchant in a low-pressure O_2 plasma. However, ion bombardment (O^+, O_2^+) is a necessary component of the etch and is often postulated to be the rate-limiting factor (e.g., Selwyn, 1986; Jurgensen and Rammelsberg, 1989; Baggerman et al., 1994). Thus the plasma density and ion energy are important parameters.

It has often been assumed that O concentration is the main etchant (e.g., Soller et al., 1984). Joubert et al. (1989) stated that under ion bombardment, the rate was controlled by the concentration of O in the plasma; the only role of O_2 was to supply O. Selwyn used laser-induced fluorescence to measure the ground-state concentration of O during etching and concluded that O atoms are the etchant but ion bombardment is rate controlling. However, Collart et al. (1995) declared that "O does not play a significant role in the chemical etch mechanism" in an RF O_2 discharge. Steinbruchel et al. (1986) found that etch rates did not correlate with either the ion flux or the density of O atoms in the plasma but with the consumption of O_2. They concluded that "etching of an organic polymer in a low pressure O_2 plasma is an ion-enhanced reaction, probably with O_2 as a major neutral reactant." Pelletier et al. (1988) used the phrase ion-induced chemical reaction. They termed the mechanism "chemically enhanced physical sputtering" in which the role of ions is product removal. Hartney et al. (1989) concluded that the etch rate of a hydrocarbon film correlated most directly with the supply of O_2 to the surface although O atoms are responsible for the initiation of etching by extracting H (Hartney et al., 1988). Baggerman et al. (1994) showed that the etch rate depended on the energy-flux density of the ions and energetic neutrals. The etching mechanism is ion induced and it is mainly O_2 that oxidizes the polymer surface. Gokan and Esho (1984) stated that the main reaction for C-consumption was



$$2C + O_2^+ + nO_2 \rightarrow 2(n + 1)CO$$

showing the role of both O_2 and ions.

CF_4 was added to O_2 to increase the concentration of O, the assumed etchant. Although the etch rate did increase, it did not track the increase in the increased number density of O in the plasma. The rate increase was attributed to the reaction of F with the polymer surface, although too high a concentration inhibited etching by competing with O (Egitto, e al., 1985). Radical generation by ion bombardment was proposed as the initiation step (Egitto et al., 1992).

O_2 has been used as the sole etchant (Pilz et al., 1990) in fabricating tri-level masks. It was found that the RIE rate was a function of the aspect ratio (AR) of the feature. Sidewall passivation, a result of resputtering from the bottom to the walls of the features, was essential to achieving anisotropy. Pilz et al. stated that their results were consistent with a model in which the etch rate was limited by the flow of neutral species (O_2, O) into the structure. However, Etrillard et al. (1994) found that no sidewall passivation was necessary when etching in a resonant inductive plasma reactor (RIPE) if the substrate temperature was reduced to –75°C and the RF bias on the wafer was high. However, they did not give the ER of the features. They concluded that ion-assisted desorption was the only phenomenon to play a significant role in etching.

Monget and Joubert (1999) obtained anisotropic profiles in a resist layer using SO_2/O_2 mixtures in a high-density plasma reactor. Anisotropy was attributed to deposition of a thin layer of S atoms

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on the polymer surface either as elemental S or bonded to C atoms of the polymer; the layer was deposited on the polymer on the bottom of the feature as well as on the sidewalls. It was thick enough to inhibit spontaneous (lateral) etching and reduced the etch rate when compared with pure O_2. However, the layer reacts with moisture to form sulfur-based acids, probably H_2SO_4; this is likely to limit the usefulness of this process.

4.8 REACTIVE ION ETCHING OF LOW-ε INTERLEVEL DIELECTRIC FILMS

4.8.1 Introduction

Etching high AR vias and trenches in low-ε interlevel dielectrics (not mask-making) is now the main challenge. ARs were relatively low in the investigations cited above. Maintaining a vertical profile as the feature sizes have shrunk, i.e., as the aspect ratios of vias and trenches (for damascene processes) increased, is of utmost importance. Since the etch rates of photoresist and an organic interlevel dielectric are similar, a hard mask (e.g., PECVD oxide, nitride, spin-on glass) must be interposed between this kind of interlevel dielectric and the imaging layer.

4.8.2 Films Containing No Silicon

Several processes resulting in straight-walled features have been reported; several did not mention any passivating layer while others found one essential. Juan and Pang (1994) etched high AR (>15:1) Ti-masked features in PI in O_2 in an ECR system with RF biasing. Anisotropy increased with increased RF power and decreased pressure. Anisotropy was 0.92 when the pressure was 0.5 mtorr.

Tacito and Steinbruchel (1996a) etched vertical features (0.8 μm) for a dual damascene process in (aromatic) parylene-N in pure O_2 at 10 mtorr. Higher pressures resulted in significant bowing.

Uhlig et al. (2000) showed a feature (AR ~ 5) etched in an aliphatic amorphous fluorocarbon film in an O_2 plasma. The walls were very slightly tapered; there was no bowing. The films were masked with SiO_2, and etched in substrate-biased ICP reactor at ~ 5 mtorr and room temperature. When the OCP power was increased to raise the etch rate, the sides were no longer straight (Uhlig, 2002).

Patterns (AR → 9) in (aromatic) SiLK films were etched in N_2/O_2 in etchers using both helicon and ICP sources (Fuard et al., 2001a,b). The wafers were biased, held at about room temperature, and the pressure was 2 to 7 mtorr. When the mixture was oxygen deficient (<40% O_2) and the ion bombardment energy high, the surface became graphitized, i.e., the aromatic hydrocarbon network was transformed into an amorphous C-backbone. The thickness of the layer is controlled by the competition between the rate of graphitization and the ion-assisted chemical etch rate. The sidewalls are coated with a layer formed by the redeposition of sputtered carbon clusters from the graphitized SiLK at the bottom of the feature. This results in better profile control; there is no undercut, although bowed profiles, due to deflection of ions to the sidewall, were usually observed. There was no dependence of the etch rate on the AR of the feature although there was a small increase in rate after the resist endpoint, indicating that resist byproducts had been deposited at the bottom of the feature. The bow position (position of widest opening) moved toward the top of the feature as AR increased. From this observation, it was concluded that differential charging was the major source of ion distortion, not mask faceting or the angular distribution of ions. Bowing can be minimized by having an adequate source of C throughout the etch. Inclusion of CH_4 in the feed gas and increasing the thickness of the resist accomplished this.

Janowiak et al. (2002) etched features (0.25 to 0.5 μm) in (aromatic) SiLK in a dual-frequency capacitively coupled reactor at 100 to 300 mtorr. H_2/N_2 was inadequate in terms of rate and profile.

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Adding O_2 increased the rate but there was inadequate sidewall protection during overetch. The best results in terms of rate and profile were obtained using a $N_2/O_2/C_2H_4$ mixture. The C_2H_2 was added for profile control; since polymer was deposited at the bottom of the feature as well, the etch rate decreased. The ratio of O_2 to C_2H_4 must be low to maintain a vertical profile. The etch rate increased significantly when the resist coating the hard mask is cleared requiring even greater profile control. It was found that C_2H_2 was superior to CH_4 in controlling the profile during overetch. Lower substrate temperature (e.g., 10°C) improved the profile and a moderate power minimized faceting of the hard mask The same process was used successfully to etch FLARE™, a fluorinated aromatic polymer.

Ar/O_2 and N_2/O_2 were used to etch (aliphatic) PTFE, (aromatic) parylene-N and F, and PAE-2 polymer films in an inductively coupled reactor (Standaert et al., 2001). Substrate bias was applied to the wafer which was kept at 10°C and the pressure was ~4 mtorr. The etch rate of PTFE is several times higher than that of the other films. Oxygen is an important etchant, but whether it is O_2 or O could not be determined. Although acetylene (C_2H_2) is a reaction product, it is not the dominant one; CO, CO_2, and H_2O are the primary products as C and H are abstracted from the polymers. In the absence of ion bombardment, the hard mask is undercut and the walls are bowed, due to reflection of O and O_2 from the feature bottom. Increasing the RF bias minimizes lateral attack but, more important in an Ar/O_2 plasma, is passivation of the sidewalls by redeposition of O-deficient etch products. The passivating layer ("veil") was revealed after the residual patterning resist was ashed. ARDE was demonstrated for etching PAE-2 in Ar/O_2 mixtures. It was also observed that vertical etch profiles can also be obtained in O_2-deficient N_2/O_2 plasmas. Microtrenching was observed in some instances in this plasma; it was thought to be due to reflection of ions from slightly inclined sidewalls.

4.8.3 Films Containing Silicon

4.8.3.1 Introduction

When organosilicon polymer films are subjected to RIE in O_2, the surface is converted to a porous SiO_2 layer (Watanabe and Ohnishi, 1986). Thus for hybrid low-ε films, as well as for SiOF, the etchant must contain a halogen (usually F).

4.8.3.2 SSQs

Narrow features (0.36 to 0.62 mm) were etched in resist-masked HSQ and MSQ films in fluorocarbon plasmas in an inductively coupled reactor with RF biasing of the substrate; the pressure was 6 mtorr and the wafer held at 10 to 20°C (Standaert et al., 1999). Using CHF_3 as the etchant, the walls were straight in MSQ but were slightly curved in HSQ, suggesting inadequate sidewall passivation. In a weakly polymerizing gas such as CF_4, the etch rate depends mainly on the ion energy and the etch rates are higher than that of SiO_2. More polymerizing gases, such as CHF_3 and C_3F_6, were also used. In C_3F_6, the SSQ films etch more slowly than does SiO_2. The more polymerizing gases deposit fluorocarbon polymers which inhibit the flux of ions and neutral species at the interface of the dielectric films. Neutral species (F) become more important as the fluorocarbon film thickness increases. In these etchants, H and C limit the etch rate. This was explained as due to the consumption of F by the C and H in the SSQs being less than in the case of the xerogel.

4.8.3.3 Xerogels

A porous film etches at a higher rate than does a dense film of similar composition (Jain et al., 1999). The enhancement is less in more polymerizing gases, a result, probably, of deposition of

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fluorocarbon material into the pores. Standaert et al. (2000) defined a normalized etch rate ER_{norm} as (1 – Π)ER where Π is the porosity of the film and ER is the measured etch rate. Although the etch rates of xerogel films (porosity 58% and 69%) were higher than that of SiO_2 in both CHF_3 and C_4F_8, ER_{norm} was lower than the SiO_2 rate.

This was attributed to the accumulation of fluorocarbon material in the large pores. Thus the etch rate enhancement due to porosity disappears. Addition of O_2 to C_4F_8 increased the etch rate of the xerogels significantly until a fluorocarbon-depleted etching regime was reached, whereas that of SiO_2 decreased monotonically. The O_2 suppresses fluoropolymer deposition in the pores; at the O2-content corresponding to the maximum etch rate, there is no fluorocarbon deposition. A 30% porous xerogel film was patterned using CHF_3 in an inductively coupled plasma; the sidewalls were slightly bowed.

The etch rates of xerogel films in a CHF_3 ICP increased with increasing porosity, but when normalized with respect to porosity the rates were higher than that of dense SiO_2. This suggested that CHF_3, trapped in the pores, increased the etch rate (Jain et al., 1999).

4.8.3.4 F-doped SiO_2

Nitride-capped TEOS-based SiOF films were etched in C_3F_8 in an inductively-coupled plasma with rf biasing of the substrate. The rate increased linearly with increasing F-concentration in the film, probably due to the additional source of F from the films. As the F-content in the film increased, the difference in etch rate for different size features decreased, and at 10% F was no longer evident. With increased F-content of the film, the sidewalls became sloped and the top of the etched feature became larger than expected for an anisotropic etch. This was attributed to the fact that polymer formation was inhibited (Allen, 1997). Standaert et al. (1999), however, achieved straight walls in resist-masked $SiO_{2.1}F_{0.1}$ films using CHF_3; micotrenching was observed. They reported that, in CHF_3, smaller features etched more slowly than did the larger ones, but the depth vs. time curve did not exhibit the curvature which is the signature of RIE lag (Gottscho et al., 1992).

4.8.3.5 BCB

Vertical trenches (dimensions not given) were formed in SiO_2-masked BCB films in CF_4/O_2 plasmas in a hexode reactor. As long as the pressure was held at <10 mtorr, straight walls were formed at all compositions. The corners were tapered; the angle was similar to the facet angle of the mask. This was attributed to the presence of a thin silicon oxide film on the sidewalls of the BCB.

When the CF_4 content was low, there was significant roughening of the surface which was no longer apparent when the CF_4 concentration was increased to 30% (Tacito and Steinbruchel, 1996b).

Vitale et al. (2000) examined F_2/O_2 and Cl_2/O_2 as etchants for BCB in an inductively coupled plasma. BCB films could not be etched in either O_2 or Cl_2 in the absence of ion bombardment, but were etched rapidly in Cl_2 or Cl_2/O_2 with ion bombardment. Thus it was proposed that RIE of BCB in Cl_2/O_2 plasmas would be anisotropic without the need for sidewall passivants. Although photoresist etches very rapidly in these plasmas, the etch rate ratios of BCB to oxide and nitride is very high in Cl_2/O_2 plasmas (as high as 80 for nitride in 40% Cl_2/O_2). These results suggest that Cl_2/O_2 might be a good choice for etching high AR features in Si-containing polymers. However, since BCB was etched rapidly in F_2 plasmas without ion bombardment, the F-based system would most probably result in undercutting.

The ideal profile of a dual damascene structure is shown in Figure 4.32. Problems specific to etching these structures are discussed in the section on integration.

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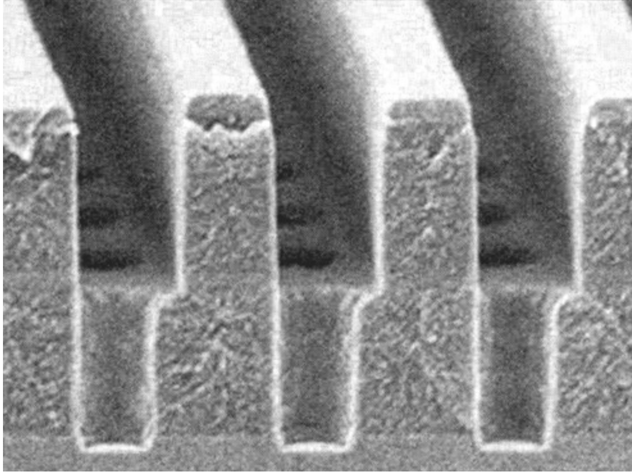

Figure 4.32 SEM cross-section of a dual-damascene structure in a spin-on low-ε film. (Courtesy of Dow Chemical Company, Midland, Michigan.)

4.8.3.6 SiCH

The behavior of SiCH in polymerizing gases in an IPC reactor was similar to that of Si but, compared to Si, the surface polymer was slightly thinner and the etch rate slightly higher. The etching of both oxide and nitride was selective to SiCH (Standaert et al., 2004). Thus, compared with Si_3N_4, α-SiCH not only lowers the dielectric constant of the stack but has the potential to be a better etch stop.

4.8.4 Resist/Residue Removal

Since O_2 plasmas modify the low-ε films, increasing ε, simple ashing is no longer feasible. In addition to resist removal is the need to clean etch residues: sidewall and bottom surface passivating films and Cu redeposited during barrier etch without distorting the etched profiles and modifying dimensions. Low-pressure, directional O_2, N_2/H_2, or $N_2/H_2/O_2$ (2 to 3%) RIE has been used for stripping but the rates are low. A wide range of liquid cleaners has been developed to be used alone or in conjunction with a plasma process to solve both the resist and etch residue problems. These materials and processes are discussed more fully in the section on integration.

4.9 CONCLUSIONS

The search for an interlevel dielectric material with the reliability of SiO_2 and the lowest possible dielectric constant continues. Perhaps it may be recalled that it took a while and a lot of work to bring deposited SiO_2 to its present state. An equivalent low-ε material probably will not be realized. Nevertheless, the number of new entries into the field, each with a promise of improvement in some property, is very large, and the competition is fierce.

Modification of processing and design, to accommodate the less-than-perfect material, will likely be the route to the desired performance.

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CHAPTER 5

Metallization

Geraldine Cogin Schwartz and K.V. Srikrishnan

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5.1 INTRODUCTION

Among the factors involved in choosing a metallization system is, as in the case of dielectrics, a need to decrease signal propagation delay for high-speed logic devices. Al and its alloys have been the metals of choice for many years and their processing is well established, but their resistivities (ρ) (2.65 $\mu\Omega$ cm for Al, higher for alloys) are not the lowest among the known conductors.

The alternative of using thicker Al (alloy) films to reduce the line resistance is of limited value as this results in an increase in the line-to-line capacitance. Figure 5.1 illustrates this point; it shows that the benefit of increased thickness soon becomes negligible. This figure also shows the deleterious effect on the RC delay of the use of higher ρ materials as an underlay for Al and as an encapsulant for Cu. The beneficial effect on RC delay of low-ε insulators can also be seen readily.

Another factor determining the choice of metal is the need for increased wireability (i.e., more wires in a unit area and more levels of metal) and for planarization and gap-fill. The increased interest in CVD metals has been prompted by their hole-filling capability. CVD metals are used to form the vertical interconnects, called "plugs" or "studs" by filling straight-sided via holes etched through the interlevel dielectric. Switching from vias tapered for better metal step coverage (by PVD processes available at the time) to vertical ones saves space which can be used to increase

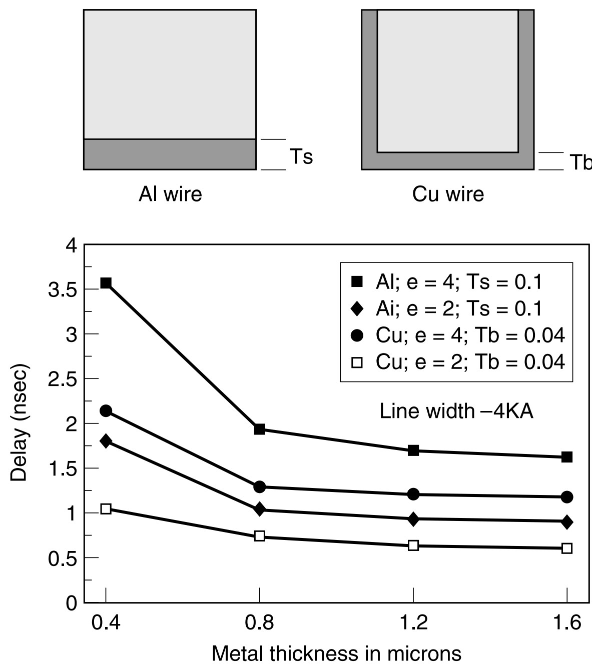

Figure 5.1 Interconnection delay as a function of metal thickness (AR) for Al and Cu, for a pitch of 0.8 μm and a length of 10 mm; and without an additional layer and for insulators with different values of ε. The metal structures are shown at the top. (Adapted from Bohr, M.T., IEDM 95, 1995, p. 241.)

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wiring density (reduced wire–wire space). CVD metals can also be used to fill both the vertical via holes and trenches in the damascene process (see Chapter 6). The ability to fill vertical vias was the motivation for developing CVD W for stud applications (Section 5.5), despite its higher ρ. Innovations in metal patterning made possible the smaller features on the chips. There were advances in physical vapor deposition methods, driven by this same need to form smaller features on chips.

Copper, a metal with lower resistivity, is now used in chip production for achieving higher speeds and increased wiring density and reliability. The method of deposition of the bulk of the conductor has also changed from CVD and PVD to electrodeposition. Also where a cost saving can be demonstrated, Cu is used even if not required for the above reasons.

5.2 ALUMINUM

5.2.1 Introduction

In the earliest days of integrated circuits (ICs), pure Al was used as the interconnection metallization. Al has a low resistivity (2.65 μΩ cm at 20°C), could be etched in solutions which did not attack the underlying films, and adheres well to other metals and to dielectric films; photoresist as well as metals and dielectric films adhere well to it. It forms a very stable, refractory, adherent oxide on its surface. It is easily evaporated (m.p. 659.7°C) and can be sputtered or deposited by CVD processes. Although pure Al eventually became inadequate, due to interaction with Si and inadequate electromigration resistance (see Chapter 7), CVD Al has nevertheless been investigated because of its superior hole-filling properties.

5.2.2 CVD of Aluminum

The basic advantage of using CVD Al is that good step coverage and void-free filling of small-diameter high-aspect-ratio (AR) holes can be realized at low temperatures. The use of CVD Al plugs in place of the CVD W plugs reduces the via resistance significantly.

In this section the focus will be on the deposition processes, i.e., on the precursors, mechanisms, etc. Plug fill and planarization by CVD Al are discussed in more detail in Chapter 6. There are several precursors for CVD of Al, one inorganic and a variety of organic ones.

5.2.2.1 Blanket Deposition

5.2.2.1.1 Inorganic Precursor

This method, rarely used, is based on the transport of inorganic Cl^- in an LPCVD reactor. Although $AlCl_3$ is sufficiently volatile, it cannot be reduced to form metallic Al. The method used is the disproportionation reaction:

$$3AlCl \rightarrow 2Al + AlCl_3$$

where the AlCl is formed either by the reaction

$$AlCl_3\,(g) + 2Al\,(l) \leftrightarrow 3AlCl$$

in which $AlCl_3$ must be vaporized and transported to the LPCVD reactor without condensation or else formed *in situ* by the reaction:

$$3HCl\ (\text{in Ar or } H_2) + Al\,(l) \rightarrow AlCl_3 + 3/2H_2$$

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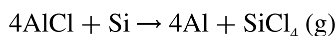
This is an atypical CVD process since the hot reactant gases decompose on a cool surface. Deposition occurs on both Si and SiO_2, and dopant incorporation is possible. It was claimed that the films were pure, adherent, had a random texture, and were smoother than those deposited using an organic precursor. Proper activation of the surface is a problem. Exposure to $TiCl_4$ has been shown to be successful (Levy et al., 1985). The activation reaction is the hydrolysis of $TiCl_4$ by the surface hydroxyl groups (Bakardjiev et al., 1976).

5.2.2.1.2 Organic Precursors

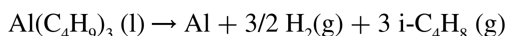
5.2.2.1.2.1 Introduction An organic source of AlCl, diethylaluminum chloride (DEAlCl), has been reported (Sasaoka, 1989). On Si, the reaction has been given as



$$4AlCl + Si \rightarrow 4Al + SiCl_4\ (g)$$

There are several others; those used most commonly are triisobutyl aluminum (TIBA or TIBAL; $((CH_3)_2CH–CH_2)_3Al$) and dimethylaluminum hydride (DMAH; $(CH_3)_2AlH$), used almost exclusively for selective deposition. Trimethylaluminum (TMA; $(Al_2CH_3)_6$) has been used as a source for pyrolysis (e.g., Biswas, 1983), PECVD (e.g., Kato et al., 1988; Masu et al., 1990), and photolysis (e.g., Higashi and Steigerwald, 1989). Various alanes, whose generic formula is $(R)_3N{:}AlH_3$ have also been used as Al sources (Sasaoka et al., 1989). Some examples are: R = methyl (TMAA), (Beach et al., 1989; Gladfelter et al., 1989), ethyl (TEAA) (Lehmann and Stuke, 1992), and dimethylethyl (DMEAA) (Tsai et al., 1994).

5.2.2.1.2.2 TIBA This is a volatile compound, explosive in contact with water, mildly toxic, and pyrophoric (but not when diluted with a saturated hydrocarbon). The films are deposited in a hot-wall LPCVD reactor. The overall deposition reaction (pyrolysis) at ~250°C is:



$$Al(C_4H_9)_3\ (l) \rightarrow Al + 3/2\ H_2(g) + 3\ i\text{-}C_4H_8\ (g)$$

The detailed chemical reactions have been discussed by Bent et al., (1989). The surface β-hydride elimination is the rate limiting step.

$$Al(C_4H_9)_3 \rightarrow AlH(C_4H_9)_2 + i\text{-}C_4H_8$$

Activation to prevent random nucleation on both metal and dielectric surfaces has been accomplished by exposure to $TiCl_4$ vapor (Cooke et al., 1982; Levy et al., 1984; Piekaar et al., 1989), use of *in situ* sputtered TiN as a seed layer which also improved surface roughness and eliminated pinholes (Cheung et al., 1990; Lai et al., 1991), and photonucleation, i.e., laser dissociation of TIBA (Tsao and Ehrlich, 1984; Higashi et al., 1987; Mantell, 1988).

One of the major problems is surface roughness, increasing with film thickness, causing lithography problems. In the initial stages of growth, hemispherical islands are formed and these coalesce when their density becomes high enough. It is implied that a higher nucleation density would result in smoother films (Cooke et al., 1982).

Amazawa et al. (1988, 1999) introduced a new reactor in which two heaters were used, so that the temperature of the gaseous reactants impinging on the front side of the wafer was higher than that of the substrate; they called this a "super hot wall CVD region." The benefit was a smooth film produced because the substrate surface was supersaturated, generating a high density of nuclei. The resistivity reported for the Al films ranged from ~2.8 to ~3.4 μΩ cm. Any C-contamination was found only at the surface.

5.2.2.1.2.3 DMAH This compound has a higher vapor pressure than TIBA. It is used with H_2 as a carrier gas. Al was deposited successfully on any conductive surface (with no mention of any pretreatment) without nucleation on adjacent SiO_2 (Tsubouchi et al., 1990). The difficulty of

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depositing Al on oxide surfaces was thought to be due to the ease of oxidation of the depositing Al on such surfaces.

Dixit et al. (1995) reported deposition of Al on CVD TiN in a single-wafer cold-wall reactor. At temperatures above 270°C, the reaction was transport limited. Below that temperature, the activation energy was 0.52 eV and had a half order dependence on DMAH concentration. The deposition rate was 4500 Å/min at 260°C and small, high-AR holes were filled without voids. They capped the CVD Al with PVD AlCu (see below for more details about CVD AlCu).

Deposition on SiO_2 or any other insulating surface by the DMAH/H_2 mixture required a short pretreatment with an H_2 RF plasma. This was done at low power density and at a low-frequency substrate bias, in a system in which the electrodes are so configured that the plasma does not touch the wafer surface. After extinguishing the plasma, deposition continued on all surfaces.

5.2.2.2 Selective Deposition

5.2.2.2.1 TIBA

UV laser photodeposition predisposes the surface to CVD of Al from TIBA, by forming a catalytic surface for subsequent growth. Thus, on the modified surface CVD film growth can occur at a lower temperature than on the oxide surface. This inhibition occurs because any absorbed Al becomes oxidized and does not promote further absorption. Thus the deposition is selective (Mantell, 1988). Maskless formation of the interconnection by CVD is possible by using a laser to expose an interconnection pattern and obtain CVD decomposition.

Pyrolysis of TIBA occurs much more readily on Al, Si, and other conducting surfaces than on dielectric surfaces. By means of molecular orbital techniques, Higashi et al. (1990) were able to elucidate the energy for crucial reactions and determine that the reaction was easier when the Al atom is bonded to other Al atoms than when bonded to O atoms. Thus there will be growth on Al and not on oxide. Mantell (1991) examined the β-hydride elimination reaction and concluded that it is suppressed on an oxide surface. Adsorption of more TIBA on that surface is prevented so that nucleation does not occur. However, if the surface temperature becomes too high, selectivity is lost because of homogeneous nucleation (Amazawa et al., 1988, 1999).

5.2.2.2.2 DMAH

Selective contact fill by Al directly on Si has been reported (Tsubouchi and Masu, 1992, 1993; Masu et al., 1994) but since the need for a barrier between Al and Si has been demonstrated, this makes the accomplishment of doubtful technical importance. Of more significance is the selective deposition on any conducting surface, e.g., TiN, Al. Sugai et al. (1993) found that although the deposition rate of Al on TiN decreased when the temperature was decreased, at the higher temperatures (e.g., 230°C), only islands of Al grew in a hole and capped the top, leaving a void. At 130°C, holes (0.3 μm in diameter, AR = 2.7) were filled solidly with Al. This was explained by the temperature dependence of the sticking coefficient.

Fabricating a direct, low-resistance Al to Al vertical interconnect in a small via hole requires removing the oxide on the lower Al surface. This was accomplished by reactive ion etching (RIE) in BCl_3/Ar and an *in vacuo* transfer to the CVD chamber. The native oxide on the Al surface not only inhibited selective CVD growth but also results in a high via resistance when Al is deposited by any method. The CVD Al was shown to grow from the bottom of the via (Kawano et al., 1994; Ohta et al., 1994).

Maskless patterning has also been performed using DMAH by forming a seed layer by laser-assisted CVD. This was done by scanning a focused laser beam (Cacouris et al., 1988) or by projection printing (Cacouris et al., 1990; Zhu et al., 1992). Photochemical CVD, using a deuterium

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lamp as a DUV source, was a two-step process: nucleation, and subsequent growth by a thermal process. The nucleation period decreased as the light intensity increased but was independent of the DMAH pressure; after nucleation, the deposition rate became independent of the light intensity but increased with increasing DMAH pressure, continuing to grow in the absence of radiation at about 200°C. It was concluded that during nucleation, photodissociation of adsorbates took place more slowly than adsorption of DMAH on the surface (Kawai and Hanabusa, 1993).

A surface electrochemical reaction model has been proposed in which free electrons on the surface catalytically contribute to the reaction. In the case of Si, a surface terminated H atom (supplied by the HF/water treatment) reacts with the methyl (CH_3) radical in DMAH to produce volatile CH_4; the H atom of DMAH remains on the newly deposited Al surface as a newly terminated H atom to react repeatedly with the CH_3 radical to deposit Al (Tsubouchi and Masu, 1992).

5.3 ALUMINUM ALLOYS

5.3.1 Introduction

Several elements have been added to Al to solve the problems encountered in its use for chip wiring. However, the disadvantage of the use of alloys is increased resistivity; the effect of such commonly used additives as Si, Cu, and Ti can be found, for example, in the CRC Handbook (CRC, 1983). When using such tables for comparisons, both the measurement temperature and any heat treatments must be taken into account.

The first problem was the interaction between the Si contact and the Al interconnection during thermal processing, leading to device failure. Si was added to the Al (Kulper, 1971) to try to minimize the problem. A comprehensive discussion of this issue, the consequences of the addition of Si and the use of barriers to isolate the contact from the overlying Al can be found in Chapter 3.

The next problem, discovered in the 1960s, was the failure of Al conductors during use, i.e., by electromigration. Addition of Cu extended the lifetime of pure Al lines (Ames et al., 1973). Finally, layered structures of AlCu and a refractory metal (Ti) were introduced to increase electromigration resistance still further (Howard et al., 1978) while allowing a substantial reduction in the Cu content without sacrificing reliability. The first stack was AlCu/Ti/AlCu which evolved to TiN/Ti/AlCu/ Ti/TiN. Some of the Al and Ti interacted forming $AlTi_3$. The Ti and TiN are deposited by CVD and the AlCu by sputtering. The details of the action of Cu and of the layered structures are covered in Chapter 7.

Other metals have been suggested as additives to improve the reliability of Al: Hf, Ta, etc. (Howard and Ho, 1977; Howard et al., 1978), Sc (Ogawa and Nishimura, 1991; Nishimura et al., 1993), Sm (Joshi et al., 1990), and C-doping of PECVD Al. However, only Cu and, later, the stack consisting of AlCu, Ti, and TiN have been used in production.

5.3.2 AlCu

5.3.2.1 Film Properties

AlCu films have been prepared by many techniques. For example, Cu was evaporated as a separate layer and incorporated into the film by heat treatment. Copper and Al have been coevaporated; however, control of the Cu content was difficult, so that excess Cu was usually incorporated as a safety measure. Excess Cu presented no problem when alloy films were patterned by wet etching, but did so when RIE replaced it. The proper concentration could be deposited reproducibly by sputtering from an alloy target and this became the method of choice.

Copper is almost always distributed nonuniformly in a codeposited film; it tends to segregate at the metal/substrate interface as $CuAl_2$ (θ-phase) particles (Denison and Hartsough, 1980;

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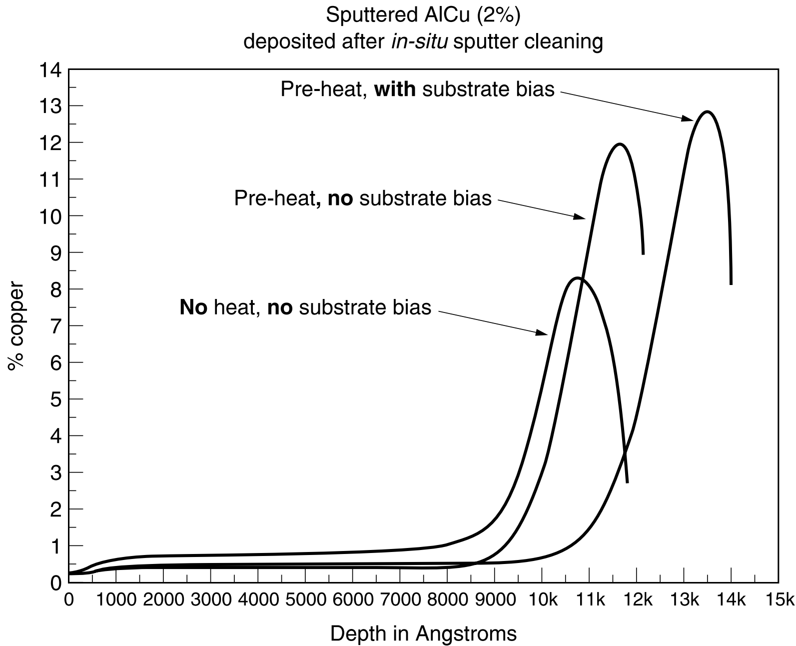

Figure 5.2 SIMS profile of Cu in sputtered Al–2%Cu: effect of processing conditions. (From Schwartz, G.C., J.M. Yang, M. Chow, P.M. Schaible, R.K. Lewis, and F. LeGoues, unpublished, 1986a.)

Burkstrand and Hovland, 1983; Schwartz et al., 1986a; Hara et al., 1986; Thomas et al., 1986). Segregation occurs in both sputtered and evaporated alloy films. Higher temperature and the use of bias during sputtering increased the pile-up, as seen in the SIMS depth profile of Figure 5.2. Copper appeared to be distributed uniformly after heat treatment; however, high-spatial-resolution profiling showed that there were θ particles extending throughout the depth of the film but concentrated in small regions, giving the appearance of uniformity for large area mapping (Burkstrand and Hovland, 1983). The θ particles formed at higher temperatures were larger than those formed at lower temperatures, leading to the suggestion that the θ particles forming at the interface grow by depleting adjacent regions of Cu (Thomas et al., 1986). LeGoues (1986) found that at lower temperatures, θ particles were distributed randomly throughout the lower half of the film, in Al grains and at grain boundaries; at higher temperatures an almost continuous layer of θ particles was formed.

No pile-up was seen when an AlCu film was deposited on an oxide-free layer of Al (Schwartz et al., 1986a; Ryan et al., 1988; Lloyd et al., 1990). The Cu distribution in AlCu/SiO_2 and AlCu/Al/SiO_2 is shown in Figure 5.3. Schwartz et al. (1986b) suggested that nucleation of θ phase was inhibited by diffusion of Cu into the underlying film. If the Al had a native oxide on its surface, the Cu segregated at the interface as it did on any oxide, and on W, Ti, Hf, and TiW.

5.3.2.2 CVD of AlCu

There have been two approaches to doping CVD Al films. In one, Cu is incorporated into the Al film by diffusion from a sputtered Cu source. A cluster system was used which incorporated a single-wafer sputtering module (DC planar cathode, magnetically enhanced) with Cu and AlCu alloy targets and the Al CVD reactor, using TIBA as the precursor. A film can be sputtered before CVD to act as a seed layer. If the alloying film is sputtered after CVD Al, $TiCl_4$ must be used to ensure nucleation of Al on the oxide surface. There was no external source for heating the composite film;

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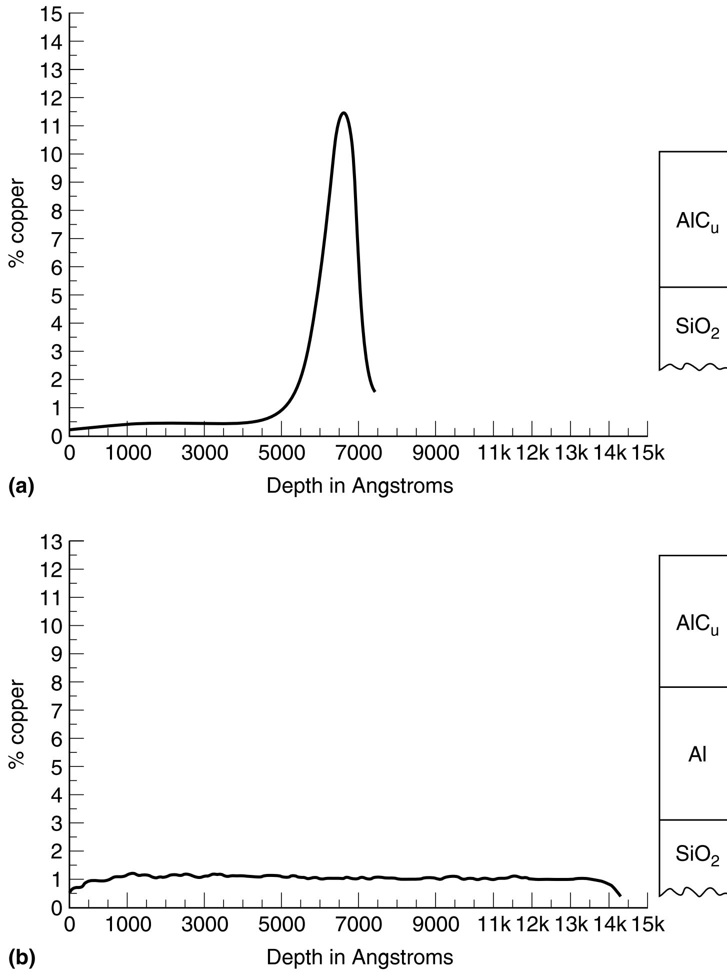

Figure 5.3 SIMS profile of Cu in sputtered Al–2%Cu deposited on (a) thermally oxidized Si and (b) $Al/SiO_2/Si$. (From Schwartz, G.C., P.M. Schaible, and G.R. Larsen, unpublished, 1986b.)

the only source was the CVD temperature itself. Cu diffused into the CVD Al film to approximate the solid solubility level at the CVD deposition temperature and was distributed uniformly throughout the CVD and sputtered films. If there is an excess of Cu in the alloy, it stays in the sputtered film. The Cu content of the CVD film can be controlled by heating the final film (Kwakman et al., 1990).

An alternative method is simultaneous CVD of Al and Cu. The details of CVD Cu are discussed in Section 5.4. DMAH and CpCuTEP (cyclopentadienyl Cu triethylphosphine) were the precursors used along with hydrogen as a carrier gas. The deposition was carried out in a cold-wall reactor; the substrate was placed on a graphite susceptor, heated by RF induction. The surface of the deposited films was mirror-like and the Cu was distributed uniformly throughout the films after annealing at 400°C for 30 min in H_2. No C or P was incorporated into the films. The deposition rate of Al was not affected by CpCuTEP; the Cu concentration was changed by changing the partial pressure of CpCuTEP. The film consisted of Al with $CuAl_2$ (θ-phase) precipitates in both the Al grains and in the grain boundaries; no Cu grains were observed. Thus the deposited film was truly an alloy and not a composite of Al and Cu grains. When the precursors were added simultaneously, the Al

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deposition was no longer selective; it was proposed that Cu was deposited first and acted as a nucleation layer for Al deposition and also to reduce interfacial resistance. Submicrometer vias, with a sputtered TiN underlayer, could be well filled with the alloy. Interconnections with vias were over-filled and a wiring level were formed by conventional RIE of the film overlying the via, has been described. The CVD alloy film was more resistive than a sputtered AlCu film of the same dimensions and Cu concentration (Katagiri et al., 1993; Kondoh et al., 1994). An alternative precursor, TMAAl, was used and three Cu precursors were investigated: (1) $Cu(hfac)_2$, (2) CpCuTEP, and (3) (hfac)CuTEM, using a cold-wall reactor and hydrogen as the carrier gas. The results obtained using (1) were not satisfactory; control of the Cu content was difficult, although the films were pure. Incorporation of Cu when using (2) was greater than when using it without the TMAAl; the authors postulated that a reaction occurred between the precursors or intermediate species. The Cu content was controlled by the temperature of the Cu source. The films were pure and no segregation occurred at the surface or film/substrate interface (1.8 wt% Cu), although small θ-phase particles were distributed throughout the film. Resistivities were 2.8 to 4.0 $\mu\Omega$ cm and the films were reasonably smooth. Similar results were obtained using (3) as precursor (Houlding et al., 1992).

5.4 COPPER

5.4.1 Physical Properties

As mentioned earlier, the use of a metal with a lower value of ρ for the interconnections decreases the delay time in ICs. The bulk value of ρ for Cu at 20°C is 1.678 $\mu\Omega$ cm, substantially lower than that of Al and its alloys. Cu is replacing Al alloys, not only for reducing signal delays, but also, as discussed in Chapter 7, because of its higher resistance to electromigration and stress-induced voiding.

As discussed below, however, there are several problems which must be solved in order to use Cu reliably in ICs.

5.4.1.1 Copper Surface

Copper does not form a stable surface oxide so that Cu is not protected against oxidative processes. The effect of the poor surface oxide on electromigration resistance is discussed in Chapter 7.

5.4.1.2 Adhesion

The adhesion between Cu and dielectric layers (e.g., SiO_2, polyimide) is poor. Improved adhesion has been realized in several ways, such as treatment of the underlying film surface before Cu deposition (Bachmann and Vasile, 1989; Chang, 1987; Ruoff et al., 1988), use of a high substrate temperature during deposition, sputtering instead of evaporation, and adhesion-promoting films (e.g., Cr, Ti, Ta). However, unless the improved adhesion is accompanied by inhibition of Cu migration, it is of little value since Cu diffuses rapidly in Si and through SiO_2 layers (see below). Thus, only adhesion layers which are also good barriers are of any practical value.

5.4.1.3 Oxidation

The susceptibility of Cu to rapid oxidation during resist stripping and to oxidation and corrosion when exposed to a hostile environment requires that the Cu be passivated. Several techniques have been reported. Doping with Mg (2 at%) reduced the oxidation rate of Cu. After annealing the

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film in Ar, the resistivity was essentially the same as that of pure copper, presumably due to the formation of a high-conductivity phase, Cu2Mg. Subsequent oxidation formed a thin MgO layer which stopped further oxidation; the protection was greater than for the unannealed film. The films adhered well to SiO_2 and showed good stability against diffusion into SiO_2 (as measured by RBS) and surface roughening (Ding et al., 1994c). Al doping of Cu achieved the same result, but thus far, with a greater impact on the resistivity. The mechanism proposed is that the Al diffuses to the surface, forming Al_2O_3, leaving the bulk as pure Cu. However, as mentioned above, increases in resistivity were observed (Nandan, et al., 1992; Ding et al., 1994a,b). Copper has also been passivated by forming silicides in a reaction with SiH_4 in a CVD reactor (Hymes et al., 1992) and by ion implantation of B and Al into the surface so that the resistivity remains unchanged while decreasing the oxidation rate by about an order of magnitude (Ding, et al., 1992). Coating the surface with a Cu_xGe_y phase by reacting Cu with GeH_4 in a LPCVD reactor passivates it as well (Joshi et al., 1995). Li et al. (1992a,b), Li and Mayer (1993), and Alford et al. (1994) suggested encapsulation of the Cu in refractory metal nitrides, formed by annealing in NH_3, preserving the resistivity of the bulk Cu line but requiring temperatures (550 to 750°C) higher than those usually considered compatible with interconnection processing.

5.4.1.4 Liners and Barriers

The deleterious effect of contamination of Si by Cu is the degradation of device performance; effective diffusion barriers are, therefore, required. Diffusion barriers for contact metallization are discussed in Chapter 3.

Copper also diffuses through dielectric layers with adverse effects. (McBrayer et al., 1988; Shacham-Diamand et al., 1993). SiO_2 was the dielectric material studied in detail. The flux is composed of neutral Cu atoms (thermal diffusion component) and, as determined by *C–V* measurements, positively charged Cu ions (McBrayer, 1988). This causes oxide charges and deep level electron traps and may cause the insulator to become conductive (Gardner et al., 1995). The leakage current increases with increasing temperature and is accelerated in the presence of an electric field. Electric field-aided diffusion is exponentially dependent on the electric field. Therefore, electrical measurements as well as physical detection methods (e.g., RBS, SIMS) must be made to determine the effectiveness of any barrier. The stages in the transport of Cu under bias temperature stress were described by Raghavan et al. (1995): (1) injection of Cu ions and diffusion of Cu neutrals into the dielectric, leading to charge build-up which then limits the ionic current, (2) thermal diffusion of both species leading to dielectric degradation and increasing leakage, and (3) increased injection of Cu due to neutralization of Cu ions leading to failure. Copper is found at the Si/dielectric interface of a Cu/dielectric/Si capacitor only after the last stage. An example, by Ragahavan et al. (1995) of the leakage current vs. time for one of these capacitors with thermal oxide as the dielectric is shown in Figure 5.4.

The source of the oxide had no influence on the results. If oxynitride and nitride were used as the dielectric, there was no gradual increase in the leakage current until an abrupt breakdown occurred. These findings agree with those of Chiang et al (1994). It was concluded that the presence of nitride has a significant retarding effect on the transport of Cu through a dielectric. Chiang et al. (1984) attributed the dielectric failure (increase in leakage) to be due to the thinning of the effective oxide thickness due to Cu diffusion.

Annealing the capacitors (at 150°C) in the absence of an electric field resulted in shorter times to failure under stress, due presumably, to the rapid diffusion of neutral Cu. Self-healing breakdown was observed at times; this was attributed to local heating from nonuniformly diffused Cu.

Diffusion of Cu through the low-ε materials is also a problem, although it has not been studied as it has been for SiO_2. Deposition of a barrier layer onto porous interlevel dielectrics (ILDs) can result in discontinuities in the barrier layer; an addition process step to smooth/seal the sidewalls may be required.

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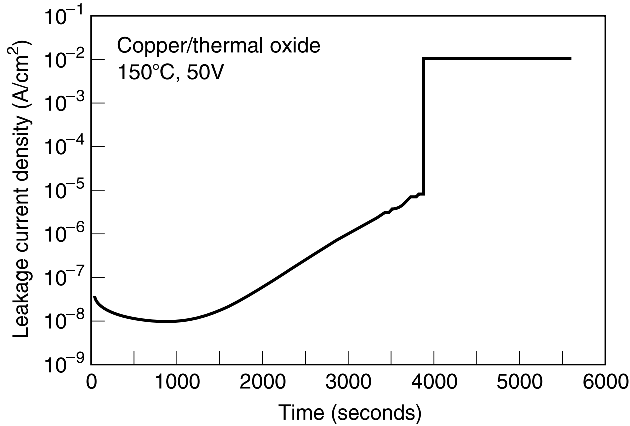

Figure 5.4 Leakage current vs. time for Cu on thermal oxide stressed at 150°C and 50 V. (Reprinted from Raghavan, G., C. Chiang, P.B. Anders, S.M. Tzeng, R. Villasol, G. Bai, M. Bohr, and D.R. Fraser, *Thin Solid Films*, 262, 168, 1995. With permission. Copyright 1995, Elsevier.)

5.4.1.5 Dielectric Liners and Barriers

SiN had the best barrier properties, followed by oxynitride. The use of these high-ε materials, however, runs counter to the need to decrease the RC delay. A newly developed barrier material, PECVD α-SiC:H (BLOk), has a dielectric constant of ~5, and thus a smaller effect on the RC delay than SiN. BLOk is, therefore, replacing SiN in dual damascene structures (e.g., Xu et al., 1999).

5.4.1.6 Metallic Liners and Barriers

5.4.1.6.1 Introduction

For many processing reasons, dielectric liners are not used except as barriers between wiring levels. A metallic barrier effective in preventing the diffusion of Cu (into Si and dielectrics) must also satisfy the following requirements:

- Prevent diffusion of impurities such as oxygen to copper surfaces and interfaces and to avoid copper oxidation or corrosion (general barrier)
- Provide good adhesion between the copper nucleating layer or copper films and the insulators
- Must have low electrical resistance, low thermal stress, low chemical reactivity with copper, and in some applications act as a nucleating surface for Cu deposition

In addition to these requirements, it is important that the selected liner material can be deposited to form continuous coatings in very thin layers (less than 500 Å and preferably about 100 Å) and into high-AR openings (3:1 or greater) in the insulators. These requirements can be appreciated when one realizes that copper metallization is being used exclusively in devices with 130 nm and smaller (down to 65 nm) feature sizes and applications. The specific liners for 65 nm and below features are in development, requiring even more stringent conditions. It is vital that the advantage of reduced overall electrical resistance of the interconnection not be lost if the gain from the lower electrical conductivity of Cu is squandered by the choice and thickness of the liner material. The

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reliability and yield advantages can also be lost if the liner films are imperfect and have discontinuities. Kaloyeros and Eisenbraun (2000) have an excellent review of ultrathin liners for copper metallization for gigabit applications.

5.4.1.6.2 Role of Microstructure

In order to minimize interdiffusion, the choice of the liner is driven by low intrinsic bulk diffusivity and also low grain boundary (GB) diffusivity of copper in the liner film. In most material systems, the GB diffusivity is orders of magnitude larger than bulk diffusivity. Therefore, the grain structure of the liner is important to minimize the GB diffusion contribution. It is desirable to form liners without grain boundaries or with a long diffusion path along interconnected grain boundaries. Although preferable, single-crystalline films are difficult to achieve in real applications. The next best solution is to form an amorphous film or one with fine grains where the grain size is much less than the film thickness. The expectation is that a grain boundary pathway is made larger than film thickness. The grain structure is, in turn, determined by the process (PVD or CVD) of liner deposition. In general, liner films deposited by CVD have more of an amorphous structure whereas PVD films are more crystalline. The degree of crystallinity or lack of it is determined by the choice of precursors, film thickness, temperature, etc., in CVD films and sputtering conditions, power, temperature, resputtering, etc., in sputtered PVD films.

5.4.1.6.3 Low Reactivity

The liners, being very thin, are susceptible to failure if they react chemically with or are soluble in the surrounding material, insulator, silicon, or copper. Ramberg et al. (2000) have approached the selection of a suitable barrier/liner for copper metallization using equilibrium thermodynamic principles. They looked for metals or compounds that have good interfacial stability (i.e., providing stable interfaces) with Cu and Si and, further, prone to forming amorphous phases. The latter requirement favors components that form phases with complex crystal structures and compositions, and with little mutual solid solubility. Based on this reasoning, the authors predicted that transition metal diborides and ternary compositions using transition metal nitride with silicon were good candidates. Among the pure metal barriers, chromium and tantalum had been used because of their low copper solubility and absence of intermetallic phases. Chromium was widely used in the packaging applications on ceramic substrate and PC boards. However, publications and research dealing with barriers for semiconductor interconnections have been mainly about Ta and TaN layers in some combination. Only limited data have been reported on other materials.

5.4.1.7 Metal Barrier Systems

5.4.1.7.1 Ta/TaN$_x$

Many properties of Ta suggested that it could be a good choice for a liner; it was a known material, highly refractory, had low resistivity, and was immiscible with Cu. Colgan (1984) concluded that a low-resistivity α-Ta (15 to 30 $\mu\Omega$ cm) was effective as a barrier to Cu at temperatures well above BEOL insulator deposition/anneal temperatures for many hours, and therefore was judged a suitable liner for Cu. An important aspect of the Colgan (1984) study was the use of thin layers of N-containing Ta as a nucleating surface to promote growth of the α-Ta phase in sputtering.

Yuan et al. (2003) reported that high-quality α-Ta films were grown by treating the SiO_2 surface with a Ar/N_2 plasma before deposition. Edelstein et al. (2001) used a PVD or IMP (ionized metal plasma) process for forming h.c.p./f.c.c. crystal structure TaN and α-Ta. Bilodeau et al. (2001) used a MOCVD process using pentakis(ethylmethylamido)Ta and NH_3 to deposit TaN films with a low

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concentration of C and O. The growth of the film was surface-reaction-limited below 300°C, provided highly conformal coatings but had a high resistivity, 850 μΩ cm. Van Der Straten (2002) reported growing ultrathin TaN films by a metal organic ALD process using liquid Ta-TBTDET (*tert*-butylimido tris(diethylamido)) and NH_3 as the reactants and observed a conformal and continuous film.

Burgess et al. (2002) deposited Ta and TaN films using IMP; the resistivity of as-deposited Ta (β-Ta) was about 170 μΩ cm and decreased to 75 μΩ cm when a small amount of N_2 gas was introduced into the sputtering ambient. The Ta(N) formed when the N_2 content of the plasma was increased further, had a slightly higher resistivity. Further N_2 increase led to stoichiometric TaN formation and the increase in resistivity was appreciable. β-Ta, substoichiometric TaN (TaN_x), and TaN films showed good step coverage for a 200 nm, AR = 2 trench. The IMP TaN_x film was microcrystalline showing a slight peak in x-ray diffraction analysis, and the TaN film was essentially amorphous (x-ray analysis). Sandwich layers of 15 nm thick films of IMP Ta and TaN with Cu were deposited on Si and annealed between 450 and 750°C for 30 minutes. The barrier breakdown temperature was characterized by the formation of Cu_3Si and $TaSi_2$ phases using x-ray diffraction. TaN was effective to 750°C, TaN_x to 650°C, and β-Ta to 550°C. The greater stability of the TaN film was attributed to the degree of noncrystallinity. Donohue et al. (2002) deposited α-Ta on a low-ε SiCOH substrate. When the substrate was bombarded by Ar, the grown film was β-Ta, whereas an exposure to a CH_4/CH_2F_2 plasma seemed to result in an α-Ta film. The study reported the electrical resistivity of α-Ta as varying from 18 to 25 μΩ cm and that of β-Ta varying from 170 to 210 μΩ cm. They also determined that the in-plane film stress for α-Ta was 1.2 to 1.4 GPa compressive, and for β-Ta was 2 to 2.5 GPa compressive.

Wang et al. (2002) studied Ta and Ta–N films deposited in a PECVD-IMP system by using various N_2/Ar ratios in the ambient. As the ambient N_2 increased, the nitrogen in the film also increased, the initial α-Ta and β-Ta phases gave way to the formation of b.c.c. TaN_x, h.c.p. Ta_2N (microcrystalline); and, at about 50% N_2, f.c.c. TaN (nearly amorphous) was formed. This work reported the resistivity values as: b.c.c. TaN_x, 49 μΩ cm; h.c.p. Ta_2N, 105 μΩ cm; and f.c.c. TaN, 228 μΩ cm and higher with higher N_2 content in ambient. In the Cu film deposited over the TaN_x film, the (111)/(200) Cu intensity ratio decreased with the increase in the nitrogen content in the TaN film.

Ou et al. (2002) studied the barrier properties of a 10 nm TaN film, deposited by PECVD, by measuring junction diode leakage. X-ray diffraction showed that the TaN film was polycrystalline and was an acceptable barrier up to 550°C, but failed at about 600°C for 1 h. When the TaN film was subjected to a plasma treatment in a N_2 and O_2 ambient, they found that thin surface layers became nanocrystalline, and became stuffed with impurities, increasing their barrier effectiveness to 750°C.

Lee et al. (2000) studied sandwich films of IMP TaN with either CVD Cu or IMP Cu films on SiO_2/Si substrate. They found that at 650°C there was Ta accumulation on Cu surface in the case of CVD Cu whereas there was none with IMP Cu, implying low interdiffusion in the case IMP Cu. This difference in behavior was attributed to the larger grain size in the CVD Cu film compared to the smaller grain size of IMP Cu film.

Tohru et al. (2001) reported that a higher agglomeration of Cu seed layer was due to the higher stress in TaN and Ta barrier layers; TaSiN barrier layer provided a lower stress film and reduced Cu seed agglomeration. Chen et al. (2001) found Cu dewetting from the FSG and OSG layer, when using TiN or TaN alone; the dewetting was avoided by using Ta/TaN or Ti/TiN layers. Wieser et al. (2002) found that implanting oxygen or nitrogen into Ta and Ta(Si) film increased barrier stability from 600 to 750°C (1 hour).

Shue et al. (2002) used ALD (atomic layer deposition) to form the TaN barrier in the Cu dual damascene process for 90 nm features using a low-ε dielectric film. The results of electromigration, stress migration, and bias temperature stress (BTS) testing all indicated that it was a robust barrier. Tiwari et al. (2002) measured the diffusion of Cu in single-crystalline and polycrystalline TaN

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films; the activation energy for Cu diffusion in single-crystal TaN was measured as 3.27 eV. The Cu diffusion in polycrystalline TaN was nonuniform. Traving et al. (2003) studied the scaling limits of Ta/TaN barriers for use with smaller feature sizes in the future. Their goal was to decrease the barrier thickness from 12 nm for 100 nm features to 2.5 nm for the 22 nm ones. The studies concluded that the PVD-formed Ta/TaN barriers are extendable. α-Ta with a low resistivity (20 to 30 $\mu\Omega$ cm) was formed even with a 0.7 nm TaN underlay film, and also when the N_2 content in TaN film was reduced (lower TaN resistance). The BTS results (450°C, 48 h) showed that the *I–V* behavior after stress was similar for Ta and Ta/TaN films over a wide range of thicknesses; films of 5 nm Ta and 2 nm TaN/10 nm Ta behaved similarly to 10 nm TaN/40 nm Ta.

5.4.1.7.2 TiN/Ti(Si)N

Chen et al. (2002) studied a highly textured, reactively sputtered, thin TiN film as a barrier. The (100) textured TiN film, deposited at lower reactive N_2 partial pressure (less than 0.23 Pa) changed to a (111) film at higher N_2 pressures (0.23 to 0.33 Pa). Both films were columnar and (111) textured and were found to be better Cu barriers in spite of larger grain size (30 nm). Lin et al. (2002) studied thermal reactions of Cu/TiN/Ti/FSG (fluorosilicate glass) or OSG (organosilicate glass) by annealing in vacuum at 400 to 900°C and concluded that the TiN/Ti stack was inadequate as a Cu barrier. Appreciable grain growth in the Cu film led to a lower resistance of the stack. At the higher annealing temperatures, there were patches of areas of missing Cu (dewetting) on both glasses. Accumulation of Ti on the Cu surface was observed for both glasses, with more accumulation in the case of FSG than OSG. A 10 nm thin Ti film, deposited using PECVD (less than 500°C, $TiCl_4$ and H_2) was annealed in NH_3 to form Ti/TiN (Wu et al., 2003). These films were effective barriers for Cu for at least 1 h at 500°C. The stack had a multilayered amorphous structure and the improvement in the performance of the barrier was attributed to the lengthened diffusion path.

Marcadal et al. (2001) claimed that by using a ternary Ti–Si–N layer, step coverage for sub-100 nm features was improved. The films were made by first thermally decomposing tetrakisdimethylaminotitanium (TDMAT), followed by plasma treatment in a gas mixture of N_2 and H_2 for 30 sec. When compared to a PVD TaN, the CVD TiSiN polish resulted in a smaller dielectric loss in CMP (chemical mechanical planarization, Chapter 6). This in turn preserved the Cu in the trenches and kept the resistivity increase to a minimum. Using TiSiN liner, the increase in a electrical resistivity of the damascene Cu was only 5% in case of oxide and only 20% for Black Diamond. Joseph et al. (2002) expanded on the Marcadal studies by flowing SiH_4 immediately after the N_2/H_2 plasma treatment of the MOCVD TiN film and by sandwiching two of these layers between Cu and Si. Using Auger and SIMS and etch pit studies they characterized the films both as-deposited and annealed. Carbon was distributed uniformly in the as-deposited TiN film. The plasma-treated films appeared to be densified and had a lower C content. Further exposure to SiH_4 led to the incorporation of Si in the film transforming it to TiSiN. It was also found that the plasma treatment of MOCVD TiN films improved its resistance to Cu diffusion to 450 to 500°C and SiH_4 treatment improved the barrier property of the plasma-treated film only slightly. Suwwan de Felipe et al. (2001) studied MOCVD TiN(Si) deposited using TDEAT and NH_3; the film had a resistivity of 600 $\mu\Omega$ cm. By using BTS, electromigration, and via chain resistance measurements, they concluded that the barrier was equal to or better than PVD Ta; however, below 75 Å, the TiSiN film on Cu was discontinuous, lowering the via chain resistance (based on lower contact resistance).

5.4.1.7.3 Other Liners

TiN and WN films were deposited into high-AR structures using ALD (Elers, 2002). The TiN film had low Cl^- and low organic residues and had a resistivity less than 200 $\mu\Omega$ cm. However, WN films deposited from WF_6 and NH_3 had high resistivity in spite of low residues. The films were difficult to

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form on Cu surfaces. In follow-on work (Elers, 2003) the nucleation problem on the Cu surface was solved by introducing triethylboron, a reducing agent for W, thereby forming WN_xC_y films. The C-containing films adhered well to Cu and can be used as a base for subsequent TiN deposition. Lipsanen et al. (2003) prepared Cu/WN_x/Si structures by magnetron sputtering and subjected them to rapid thermal annealing (RTA). A 15 nm WN film was effective in preventing the Cu–Si reaction up to 700°C and a 12 sec RTA stress. Lu et al. (2003) found that even 6 nm of W–Si–N was effective in preventing the Cu–Si reaction when subjected to RTA at 800°C. Lu further found, however, that ALD deposited WN_xC_y films failed when subjected to 700°C for 30 minutes. A similar observation was made by Kim et al. (2003), who reported that ALD deposited WN_xC_y failed as a barrier layer between Cu and Si on annealing at 700°C for 30 minutes. Ecke (2002) reported a promising diffusion barrier, a WN_x amorphous film deposited using a mixture of WF_6, N_2, and H_2 in a PECVD process. The electrical resistance of the film was about 200 μΩ cm and its fluorine content was very low.

Deng (2002) reported on the use of amorphous WSi_2 as a barrier to Cu diffusion. The films were effective up to 600°C and can be further improved by using an *in situ* N_2 plasma treatment at 300°C for 5 minutes. Takeyama (2003) deposited ternary nitride films, TiZrN, and found them as a good barrier between Cu and Si up to 600°C. The films had fine grains, 2 to 10 nm in size, and had a resistivity of 90 μΩ cm. Kim et al. (2003) showed that a multilayer diffusion barrier of the structure TiN/M/TiN where M can be Ru, Cr, and Zr, and found that Zr provides the best barrier performance.

5.4.1.7.4 Electroless Plated Barrier

Kohn (2003) used a selective electroless process to deposit a 10 nm film of Co–W–P conformally and found that the barrier was effective in preventing Cu diffusion up to 450°C The as-deposited film consisted of nanocrystalline Co (h.c.p.) and an amorphous CoWP phase. At about 290°C, the amorphous part crystallized to h.c.p. phase. At about 420°C an orthorhombic CoP phase was starting to form, while the major parts of the film remained h.c.p.

5.4.1.8 Encapsulation

It is clear that, due to the need for encapsulating/passivating layers, the low RC delay expected from the use of low-resistance Cu wiring is not realized. This is illustrated in Figure 5.1. It must be pointed out again that, with respect to delay, the choice of dielectric, i.e., ε, is as important as the ρ of the metal. Gardner et al. (1995) stated that encapsulated Cu performed better than AlCu but, as seen in Figure 5.1, this may not be always true.

Attempts to reduce the effects of encapsulation appear to introduce other problems. The barrier layer thickness may be reduced, but at the possible expense of unreliable performance. The increased line resistance arising from the use of a barrier layer may be ameliorated by increasing the width of the conductor but reducing the spaces between conductors increases cross talk. To avoid this problem, the wiring pitch must be increased but this comes at the expense of reduced packing density. An alternative might be the use of a nitride-based dielectric or, better yet, the lower ε SiCH film as the barrier, but only immediately adjacent to the Cu (to avoid a huge increase in cross talk of the higher ε material), with a lower ε material forming the bulk of the insulator. However, any significant increase in ε is to be avoided as is any increase in line resistance.

In addition to its effect on delay time, encapsulation increases process complexity and therefore process cost.

5.4.2 Physical Vapor Deposition of Cu

Both evaporation and sputtering are feasible methods and were used extensively, particularly in earlier days when hole filling was not of paramount importance.

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Park et al. (1991) compared dc planar magnetron sputtering of Cu and Al. They reported that the thickness of metal at the bottom of a hole was greater for Cu and that the sidewall coverage of Cu was continuous. They attributed this to the near normal cosine distribution of the sputtered Cu (Figure 5.5a) which enhances the forward throw of sputtered particles. Sputtered Al showed a preferential emission distribution directed at about 40° from the target normal (Figure 5.5b) which would promote lateral growth at the top, resulting in void formation within the hole as well as thinner deposits on the bottom of the hole.

A so-called low-energy ion bombardment process (using an RF–DC coupled mode of bias sputtering) was used to deposit Cu films on oxide or nitride substrates (Takewaki et al., 1995). The grains in films which were bombarded, during growth, by ions of energy ≥50 V and then annealed at 450°C for 30 min, grew to sizes as large as several hundred micrometers; this probably accounted for the excellent electromigration resistance of the films. In addition, the crystal orientation of the film was converted from Cu(111) to Cu (200). The ρ of the films was 1.76 μΩ cm (bulk = 1.72 μΩ cm). The drawback for device fabrication was the need to remove part of the dielectric film to couple the DC bias to the substrate surface.

5.4.3 CVD of Copper

5.4.3.1 Introduction

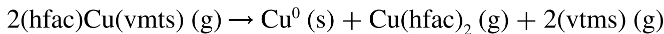
There are two classes of precursors for CVD Cu, Cu(I) or Cu^{+} and Cu(II) or Cu^{2+}.

5.4.3.2 Cu(I) Precursors

The general formula of the Cu(I) precursor is $XCuL_n$, where X = univalent negative ligand, L = neutral Lewis base ligand, and $n = 1$ or 2.

A widely used compound is (hfac)Cu(vmts), sold as Cupra Select (Norman et al., 1991); in this compound X = hfac (hexafluoroacetylactonate) and L = vmts (vinyltrimethysilane) (Jain et al., 1991; Awaya and Arita, 1993a; Han and Jensen, 1994). The compound is shown in Figure 5.6.

The deposition reaction is disproportionation:



$$2(\text{hfac})\text{Cu}(\text{vmts})\ (\text{g}) \rightarrow \text{Cu}^0\ (\text{s}) + \text{Cu}(\text{hfac})_2\ (\text{g}) + 2(\text{vtms})\ (\text{g})$$

The reverse reaction is a selective, noncorrosive, isotropic dry etch for Cu (Norman et al., 1991).

There are other precursors, with different X and/or L groups, e.g., X may be other β-diketonates, e.g., acetylacetonate (acac), fluoroacetylacetonate (tfac) (Shin et al., 1992), alkyltrimethylsilane

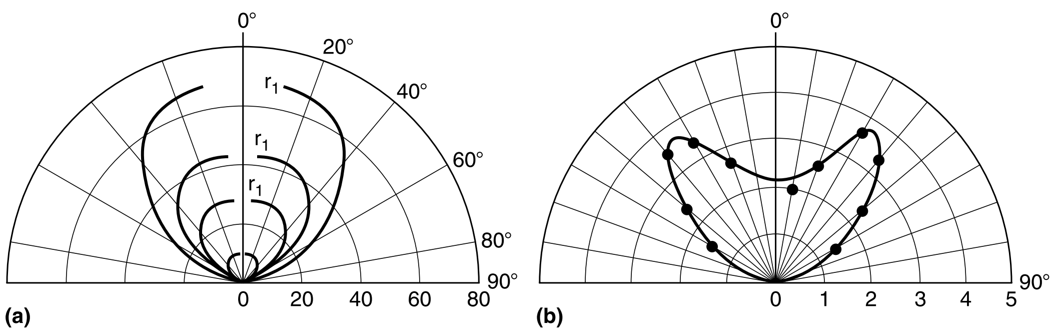


Figure 5.5 Angular distribution of (a) sputtered Cu and (b) sputtered Al. (Reprinted from Park, Y.H., A.H. Chung, and M.A. Ward, VMIC, 1991, p. 295. With permission.)

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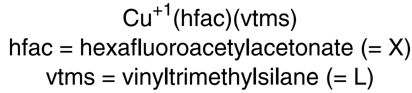


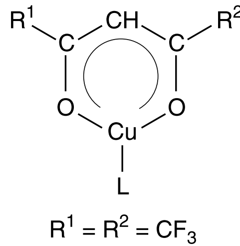


Figure 5.6 Structure of Cu(I) precursor.

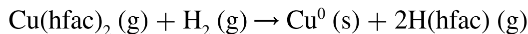
(ATMS) (Park et al., 1998), 3,3-dimethyl-1-butene (DMB) (Rhee et al., 2000), and L may be 1,5-cyclooctadiene (COD) (Jain et al., 1991; Cohen et al., 1992) or 2-butyne (Jain et al., 1991), trimethylphosphine (PMe_3) (Dubois and Zagarski, 1992), and vinyltrimethoxysilane (VTMOS) (Choi et al., 1996), 1,5-dimethylcyclooctadiene (1,5-DMCOD) (Lee et al., 2001).

Lin et al. (2003), using Cu(hfac)vmts, showed that using He as a carrier gas instead of H_2, increased the capability of void-free filling of small, high-AR vias. The use of He would avoid the H_2 reduction reaction which enhances the deposition of Cu, and so decreases the probability of re-emission (increases the sticking coefficient) which inhibits void-free filling.

5.4.3.3 Cu(II) Precursors

The most widely used Cu(II) precursor is $Cu(hfac)_2$. A cold-wall reactor was often used. Cu can be deposited by heating the precursor in Ar (Temple and Reisman, 1989), reduction in H_2 or in an Ar/H_2 mixture (e.g., Awaya and Arita, 1989; Kaloyeros et al., 1990; Lai et al., 1991; Lecohier et al., 1992a), or in an H_2O/He mixture. The growth rate for Cu on Pt-seeded oxide surfaces was the same in a chemically inert carrier gas (He) or a reducing gas (H_2) (Lecohier et al., 1992a).

The reaction with H_2 is



$$Cu(hfac)_2\ (g) + H_2\ (g) \rightarrow Cu^0\ (s) + 2H(hfac)\ (g)$$

Water vapor, added to both Cu(I) (Gelatos et al., 1993) and Cu(II) precursors, increased the deposition rate of Cu (Away and Arita, 1991a,b; Lecohier et al., 1992a) and improved the surface morphology and resistivity of the deposited film. Addition of water vapor to Cu(hfac)(vtms) at the optimum concentration more than doubled the deposition rate and reduced the nucleation time without affecting the resistivity of the film, although too high a concentration increased the resistivity significantly, perhaps by forming copper oxide (Gelatos et al., 1993). For $Cu(hfac)_2$, the improvement in rate of a factor of about 9 was attributed to the formation of a dihydrate of $Cu(hfac)_2$ which has higher vapor pressure and lower decomposition temperature than the anhydrous compound (Awaya and Arita, 1993b). However, this was refuted by Lecohier et al (1992b), who observed a dependence of the growth rate on the water vapor content of the reaction mixture when the amount of precursor arriving at the substrate was independent of that of the water vapor. They stated that the concentration of water vapor appeared to be rate determining. Awaya and Arita, 1993b) proposed that the CVD mechanism changed when H_2O was used.

Other Cu(II) precursors include Cu acetylacetonate ($Cu(acac)_2$), Cu dipivoylmetanato ($Cu(DPM)_2$) (Pelletier et al., 1991; Zama et al., 1992).

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5.4.3.4 Deposition

Deposition of Cu using any of the precursors and thermally activated reactions most often has been carried out in LPCVD reactors but APCVD has also been used (Temple and Reisman, 1989; Lai et al., 1991). The systems have been hot wall (e.g., Lai et al., 1991; Kaloyeros et al., 1990; Shin, et al., 1992; Jain et al., 1993b), warm wall (Jain et al., 1993b; Gelatos et al., 1993), and cold wall (Away and Arita, 1989; Cho et al., 1992; Kim et al., 1994). Thermally driven deposition using an Ar laser resulted in very high-purity Cu deposits (Han and Jensen, 1994). Photoassisted CVD, using Hg-vapor UV light, has also been reported (Zama et al., 1992). PECVD in an RF glow discharge (Oehr and Suhr, 1988; Awaya and Arita, 1991b) and using microwave plasma excitation have also been used. In all these reactors, the precursor was vaporized and flowed into the deposition chamber. An aerosol-assisted, liquid delivery system was used to attain very high deposition rates in a warm-wall reactor. The liquid was a solution of Cu(Hfac)(COD) in toluene (Roger et al., 1994). This method does not rely on the delivery of the precursor at the equilibrium vapor pressure at the bubbler temperature. Thus higher precursor feed rates, leading to higher deposition rates, can be obtained.

The resistivity of CVD Cu films deposited using all the methods described above ranged from about 1.7 to 7 μΩ cm; the bulk resistivity is ~1.7 μΩ cm. Both blanket and selective deposition can occur. Growth rates as high as ~5000Å/min have been reported using (hfac)Cu(vtms) (Jain et al., 1993a) and 900 Å/min with $(Cu(hfac)_2$ in $H_2 + H_2O$ (Awaya and Arita, 1993b).

5.4.3.4.1 Blanket Deposition Using (hfac)Cu(vtms)

5.4.3.4.1.1 On Blanket Metal Underlays In one instance a cold-wall reactor was used with a carrier gas (Ar) and a barrier metal, TiW, was the underlay. The wafers were placed face down and heated at the back. Excellent step coverage was obtained; high-AR trenches and vias were filled without keyholes. After annealing at 400°C, the resistivity of the films was 2.0 μΩ cm. (Cho et al., 1992). In another, a H_2 carrier gas was used in a cold-wall reactor and the underlay a Ta seed layer. The step coverage and hole fill were temperature dependent. At 260°C, the Cu film was thinner on the edge of a step than at the top and bottom; there was separate island growth and voids were formed at the bottom of a via. Below 210°C, the shape was more fluid-like; below 200°C the vias were filled completely, the films were continuous, and the upper surface over the via was planarized, as shown in Figure 5.7 (Awaya and Arita, 1993, 1995).

5.4.3.4.1.2 No Metal Underlay There was no substrate-dependent nucleation; both Si and SiO_2 surfaces were coated when the Cu was deposited in a warm-wall reactor, using (hfac)Cu(vtms) without a carrier gas. Excellent step coverage was observed; the film deposited into the deepest corners of an overhang structure, which was consistent with a very low sticking coefficient. Films had very low stress, as indicated by the fact that a thin cantilever (used in the step coverage experiments) was not bent (Jain et al., 1993b).

The evolution of the Cu profile in small features was modeled for low-pressure, low-temperature CVD. A single rate-limiting precursor model was used; the model was verified by SEM images of the features (Burke et al., 1997). Surface diffusion was unimportant. Species remission within the features plays a critical role in achieving conformal step coverage and complete filling, thus the sticking coefficient (S_c) is required to be $\ll 1$. The probability of re-emission was directly proportional to the precursor flux and inversely proportional to substrate temperature. With a value 0.003 for S_c, and a trench width of 0.35 μm, the model predicted complete fill for an AR of 4 but a key hole for AR = 5; increasing S_c to 0.01 led to a large void. Since both the deposition rate (Nguyen et al., 1997) and S_c (Burke et al., 1997) increase with temperature, balancing the need for a reasonable growth rate and good fill will require a careful choice of deposition conditions. Kobayashi et al.

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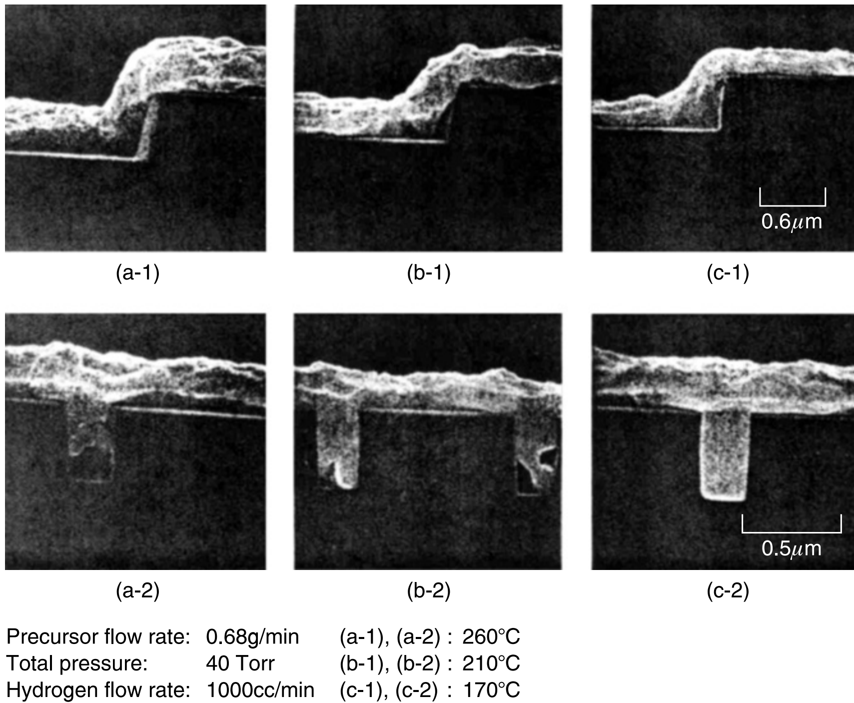

Figure 5.7 SEM images showing temperature dependence of step coverage and via filling by CVD Cu. (Reprinted from Awaya, N. and Y. Arita, *Jpn. J. Appl. Phys.*, 32, 3915, 1993; Awaya, N. and Y. Arita, *Thin Solid Films*, 262, 12, 1995. With permission.)

(1999) reported good filling of 0.25 μm holes and trenches (AR = 3) at a high temperature (215°C) and high rate (200 nm/min) by ensuring that the partial pressure of the source gas was high.

5.4.3.4.2 Selective Deposition

5.4.3.4.2.1 Cu (I) Precursors Some precursors always result in selective growth, e.g., (hfac (Cu)$(PMe)_3$, and some never do, e.g., (hfac)Cu(2-butyne). Other precursors, e.g., (hfac)Cu(vtms) and (hfac)Cu(COD), may or may not, depending on the experimental conditions; Jain et al. (1992) and Dubois and Zegarski (1992) have summarized some of the different results reported in the literature. This indicates the need for careful surface preparation, but there may be other reasons for variability in results, e.g., the reactor configuration, wall temperature, use of a carrier gas, etc.

Selectivity might be explained by catalysis of the deposition reaction by conductors so that no Cu could be formed on dielectric surfaces; this is related to the need for electron transfer (Norman et al., 1991).

In a study using (COD)Cu(hfac), the precursor adsorbed on a metal surface, forming a Cu(I)–hfac surface intermediate which then reacted to form Cu. On SiO_2, the precursor adsorbed as a very different surface complex. This suggested that the basis for selectivity was the differences in surface reactions and not a lack of precursor adsorption on oxide (Cohen et al., 1992).

In the case of (hfac)Cu(vtms) it was demonstrated that adsorbed H-bonded OH groups on SiO_2 surfaces are nucleation sites for film growth, but that isolated OH and strained Si–O–Si groups are not (Dubois and Zegarski, 1992; Farkas et al., 1994). Selectivity depends on passivation of the OH surface groups. This was done most effectively by *in situ* introduction (before or during CVD) of

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gaseous $(CH_3)_2SiCl_2$; the Si bonds to the O group after the H is removed by the Cl, so that the surface is O–$Si(CH_3)_2$ and not OH (Jain et al., 1993b).

The bond strength of Cu–L, and thus the nature of the precursor ligand, was shown to affect selectivity. A weak bond (e.g., L = 2-butyne) is readily dissociated on most surfaces with little thermal activation and no electron transfer from the substrate resulting in easy deposition on oxide (Jain et al., 1991; Dubois and Zegarski, 1992). Although (hfac)Cu(vtms) (a high vapor pressure liquid) is stable, it appears to have a very narrow process window. The most stable precursor is (hfac)Cu(PMe_3) which should guarantee selectivity; however, it is a solid and difficult to pump. Thus there appears to be no completely satisfactory precursor as yet.

5.4.3.4.2.2 Cu (II) Precursors

Selective deposition appears to be the rule. The same difference in the surface reactions on oxide vs. metal was found to hold for the $Cu(hfac)_2$ as well for (COD)Cu(hfac) (Cohen et al., 1992). Thus selective deposition of Cu can be used to fill via holes etched down to the underlying conductor which can be Al, Cu, Al, silicides (Awaya and Arita, 1989). It can also be used for area-selective deposition on oxide surfaces by forming a thin patterned seeding layer upon which Cu can then grow The underlay must adhere well to the substrate and must not degrade the morphology, purity, or conductivity of the CVD Cu film (Lecohier et al., 1992a). The deposition temperature was found to be the most important parameter in ensuring selectivity. Under the deposition conditions investigated, substrate temperatures between 310 and 360°C ensured selectivity. When the temperature became too high, Cu was always deposited on oxide, sometimes as a localized deposit or else as a continuous film (Kim et al., 1994). When water vapor was added to increase the growth rate, the selectivity was improved when He was used instead of H_2 (Lecohier et al., 1992b,c).

H_2 reduction of $Cu(hfac)_2$, for filling small features with Cu, was recently carried out in supercritical CO_2 (SC-CO_2); this was named supercritical fluid chemical deposition (SFCD). High diffusivity and low viscosity are responsible for the penetration into small, high-AR features. The deposition rates were 30 to 50 nm/min and the yield of Cu was very high, almost 100% under certain (unstated) conditions (Kondoh and Kato, 2002).

5.4.3.4.3 Selectivity Loss

Loss of selectivity occurs if there is an electrically conducting path through the dielectric (poor-quality film, pinholes) or there are metallic residues on its surface (Cohen et al., 1992). A high total pressure and a hot-wall system often result in nonselective deposition (Kim et al., 1994). Other factors that can lead to loss of selectivity are heating the precursor or the substrate to too high a temperature, the presence of contaminant hydrocarbons, and residual precursors contaminating the chamber walls when opening the system. Once a film is nucleated, subsequent growth is rapid.

5.4.3.5 Film Growth and Morphology

Nucleation and growth of CVD Cu films, deposited using (hfac)Cu(vtms), depended on the underlying barrier films. Nucleation was more difficult on both Ta and TaN_x ($x < 0.5$) than on a Ta layer with a thin overlying sputtered Cu film.

Films grown directly on the barriers first coalesce into islands and only form a continuous film after the deposition of > 200Å, whereas a continuous film is formed immediately on the Cu-coated barrier. Films grown directly on Ta or TaN_x are randomly oriented. There is an amorphous layer between the CVD film and the barrier. When the barrier was coated with the sputtered Cu layer there was no amorphous layer and the CVD Cu film had a highly preferred (111) orientation (Kroger et al., 1999).

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Copper films deposited on DC-sputtered TiN films had lower resistivity and impurity contamination, and a higher (111) orientation and better adhesion than those deposited on Ta and TaN sputtered substrates (Lin et al., 2002a). The properties of TaN became similar to those of TiN when the TaN film was exposed to an Ar (Lin et al., 2002b) or a H_2 (Lin et al., 2002c) plasma before being transferred (via a load-lock to the Cu CVD chamber) and annealed in N_2 after deposition.

Kang et al. (2002) found that the (111)/(200) ratio of a CVD Cu film on a CVD TaN barrier increased as the (111)/(200) ratio of the barrier decreased. Depositing the TaN at 250°C resulted in a CVD Cu film with the stronger (111) preferred orientation.

The grain size of the as-deposited films was small but increased and the level of contamination decreased when the films were annealed. After annealing and chemical mechanical polishing (CMP, see Chapter 6) the Cu grains in the features were larger than the feature width (0.25 μm) (Kobayashi et al., 1999).

5.4.3.6 New Developments

The high cost of CVD has largely restricted its use in IC manufacturing to the deposition of very thin films used as seed layers. The appeal of using existing vacuum deposition apparatus to deposit CVD films for seamless fill as well has revived some interest in CVD and led to the development of catalyst-enhanced CVD (CECVD). Iodoethane (C_2H_5I) was the source of iodine used as a catalytic surfactant and (hfac)Cu(vmts) was the Cu source. In this system, film growth is bottom-up; the features are superfilled without voids or seams (Shim et al., 2002).

The growth rate was shown to be proportional to the surface concentration of I on the Cu seed layer (Shim et al., 2002; Kwon et al., 2002). The action of the adsorbed I in enhancing the growth rate is postulated to be due to its weakening of the Cu^+–(β-diketonate)$^-$ ionic bond. The process required a thin Cu seed layer sputtered over a barrier layer. Iodothane was injected into the reactor at 150°C, and allowed to adsorb on the Cu seed upon which it dissociates into I atoms. The Cu precursor was then admitted and Cu deposited. The initial deposition was conformal but then abnormal thickening occurred on the bottom and eventually the feature was filled completely; the growth rate then decreased abruptly. If deposition was continued, the film became almost level with a small bump over the top of the feature. Holes superfilled faster than trenches of the same width.

The growth was described in terms of the growth rate of the film and the diffusive transport rate of I on the surface of Cu. During the initial conformal growth, the bottom area shrinks faster than the area along the sidewall. Thus the initially uniformly distributed I atoms migrate from the sidewall to the bottom (a snowplow effect), increasing the deposition rate there. As the film reaches the top of the feature, the I migrates across the surface and the growth proceeds evenly along the surface. The dependence of the growth rate on the I adatom concentration supports the proposed mechanism.

Holes are filled, in a bottom-up fashion, more rapidly than trenches of the same geometric dimensions (Shim et al., 2002). The adsorbed I also suppressed development of surface roughness. The resistivity of the films was 2 μΩ cm; they were polycrystaline but predominantly (111) oriented (Hwang and Lee, 2000).

The mechanism of curvature-enhanced accelerated coverage (CEAC) by CECDV (Josell et al., 2002a) is the same as that used to predict superfilling of damascene features by electroplating (see Section 5.4.4), i.e., the increasing coverage of a rate-accelerating catalyst due to a decrease in surface area.

5.4.3.7 Atomic Layer Deposition (ALD)

ALD resembles CVD. It is "a monolayer stepwise growth process that exploits the binding energy difference between chemisorption and physical adsorption" (Solanski and Pathangey, 2000).

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The technique is used for forming Cu seed layers. The substrate is exposed alternately to the Cu precursor and the reducing agent with a pulse N_2 gas between. The pulses are timed so that the reaction to form Cu goes to completion. After each reaction excess reactants and byproducts are removed with a N_2 pulse. Conditions are adjusted so that all surfaces are saturated, making it a self-controlled growth process. It is capable of depositing conformal films with an accurate control of thickness. High-quality films can be deposited at temperatures lower than those used in other methods. The Cu source was $Cu(hfac)_2\ xH_2O$ and the best films were grown using formalin as the reducing agent. The resistivity of a 20 nm thick film, deposited on 6 nm TiN was 4.25 $\mu\Omega$ cm, and the conformality over high-AR features was excellent.

Another process involves (1) deposition of a monolayer of a precursor (e.g., Cu(hfac)(tmvs), Cu(hfac)(2-butyne), etc.), (2) exposure of the layer to an O_2 or O_2-containing plasma, liberating the ligand, and forming an oxidized Cu surface, (3) reduction of the Cu oxide by exposure to a H_2 or H_2-containing plasma leaving a monolayer of Cu on the surface, (4) repetition of steps (1) (3) to form the desired thickness. An alternative is the use of water vapor to liberate the ligand; this oxidizes the ligand but not the metal (Powell and Fair, 2002).

5.4.4 Electrochemical Deposition of Cu

5.4.4.1 Introduction

The replacement of RIE of Cu (see Section 5.7.2) by deposition of the metal into features etched into the ILD (embedment/damascene processing, see Chapter 6) requires a process which can fill the gaps without voids/seams. Although CVD was adequate (better than sputtering), deposition of thick films is an expensive process (consumption of precursors). By now, electrochemical deposition, which is more cost-effective and uses simpler equipment, has largely replaced it. This is a two-step process; a Cu seed layer is usually deposited first, although the feasibility of electroplating directly onto a barrier at the exchange current density (c.d.) using a low concentration of Cu^{2+} has been discussed by Takahashi (2000).

5.4.4.2 Seed Layer Deposition

To ensure that electrochemical deposition is successful, the seed layer must provide complete and smooth coverage of the features without an overhang profile and must not be heavily oxidized so that the oxide layer can be dissolved readily in the plating bath. Dubin et al. (1997) proposed the *in situ* deposition of a sacrificial protective Al layer on the Cu seed to avoid its oxidation during air exposure. The Al film is etched when immersed in the plating bath.

Seed layers have been deposited by directional sputtering (IMP or long target-to-substrate, with or without substrate bias) or by CVD. Sidewall coverage is sometimes difficult to achieve with sputtered films whereas thin films of a CVD deposit are conformal. For electroplating, the resistance of the seed layer is important in the initial stages (Broadbent et al., 1999). They modeled the effective resistivity of CVD and IMP films in terms of step coverage and mass deposited within the feature. The resistivity of the CVD films was significantly lower due to the improved coverage. They also emphasized that the resistivity (thickness) of the seed layer within the features is significantly higher (thinner) than that measured on planar monitor wafers. Initial thin deposits can be plated uniformly on high-resistivity seed layers using the method mentioned above for plating on the barrier layer directly.

The resistivity of blanket Cu films (500 to 700 Å), deposited on a CVD TiN barrier layer using (hfac)Cu(1,5-DMCOD) with He + H(hfac) carrier gases, at the transition temperature (i.e., the temperature at which the mechanism changes from a surface activated to a mass-transport-limited regime) was similar to that of annealed sputtered Cu. The cost of this precursor is lower than that

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of the (hfac)Cu(vmts), the one used frequently, and thus lowers the cost of seed layer deposition (Lee et al., 2001).

The new approach is ALD (described above), which, according to the International Technology Roadmap for Semiconductors (2001), will emerge as the dominant solution because of its ability to deposit conformal films with an accurately controlled thickness.

5.4.4.3 Electroless Plating

Electroless Cu deposition is an autocatalytic process, i.e., once an initial layer of Cu is formed, the reaction continues unabated. The process requires a catalytic surface, on which both reduction of the Cu ions and oxidation of a reducing agent take place. The catalytic or activated surface (seed layer) is usually Cu.

The overall deposition reaction (with formaldehyde (HCHO)) as the reducing agent) is

$$Cu^{2+} + 2HCHO + OH^{-} \rightarrow Cu^{0} + H_2 + 2CHOO^{-} + 2H_2O$$

The deposition rate of Cu increases with increasing temperature and pH; the rate reaches a plateau above pH ~ 12.5. No deposition is observed at a pH < 11; a pH > 12 is needed for stable deposition but too high a rate can degrade the film quality. Jagannathan and Krishnan (1989) showed that replacing formaldehyde by triethanolamine extends the operating range to a pH < 9. Ethylenediaminetetracetic acid (EDTA) is a complexing agent often used in these baths.

Typical formaldehyde-based solutions, with and without Na^+ and K^+ (to minimize incorporation of these ions in the film), were given in a review by Cho et al. (1993) and Shacham-Diamand et al. (1995) who also discussed the mechanisms of electroless plating. The baths include not only the ingredients essential for the reaction shown above, but additives to stabilize the solution, reduce surface tension, retard H_2 incorporation, and otherwise regulate the film properties. Resistivity values of $< 2\ \mu\Omega$ cm have been reported (Dubin et al., 1997). One of the drawbacks to the use of electroless Cu is the incorporation of the reaction products H_2 and H_2O into the film since they degrade the quality of the film.

Dubin et al. (1997) demonstrated filling high-AR features. High deposition rates (~120 nm/min) resulted in seams; lowering the rate to 75 nm/min eliminated them. They proposed that seams are due to "a balance of diffusion-limited reaction of electroless Cu plating in subhalf micron features with a kinetically (or electron-transfer) limited reaction on the field of the wafer and close to the top of vias/trenches." A simulation of the deposition of electroless Cu into deep features predicted that a seam or void would form if the diffusivity was too small or the deposition rate too high (Smy et al., 1997).

Electroless Cu films, as deposited, are fine-grained. Mak et al. (1993) deposited films from baths containing different (but unfortunately unidentified) additives. They were comparable as-deposited but one film recrystallized at low (< 300°C) temperature whereas the other resisted it. According to them the films that resisted recrystallization had a high density of organic inclusions and trapped H_2. The inclusions were effective in pinning grain boundary movement. They also showed that "H_2-containing voids can be an internal source of structural defects and can cause internal fatigue degradation during thermal cycling."

5.4.4.4 Electroplating (Electrodeposition) of Cu (ECD)

5.4.4.4.1 Introduction

An introduction to the principles of electroplating can be found in Chapter 2.

Electroplating avoids incorporation of H_2. For many years it was used on circuit boards, ceramics, and flexible plastic substrates. Poris (1993) patented a process for replacing RIE of Cu by plating Cu into resist which had been patterned to expose the via and interconnection regions. After removing

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the mask the metal features are etched electrochemically to round the corners. The plating cell included a virtual anode for improved thickness uniformity and a cathode gasket to protect the back surface. In 1994 Contolini et al. suggested electroplating, followed by electropolishing, for forming embedded planar Cu interconnections on chips but it was several years before plating was used in commercial chip production. Plating is now used extensively, followed by CMP. The use of electropolishing was mentioned in the International Technology Roadmap (2001) as a possible replacement for CMP to prevent damage to soft low-ε dielectric films. The thrust of the development work with respect to ECD is achieving and understanding void-/seam-free fill of small features.

5.4.4.4.2 Processes

The basic plating bath almost always contains $CuSO_4$ with H_2SO_4 to decrease solution resistance and dissolve the oxide on the surface of the seed layer; excessive oxidation can inhibit wetting (Reid, 2001). Commercial plating baths have always contained proprietary additives and are well stirred. Single-wafer plating stations are the general rule in chip production. The wafer is held, face down, in a relatively small volume of the electrolyte. The stress in plated Cu films was reduced significantly when Cu hexafluorosilicate replaced $CuSO_4$ and used as the sole ingredient in a plating solution. The reduction in stress was said to improve the adhesion between the Cu film and the barrier layer. After annealing at 300°C the Cu film was essentially stress-free (Hara et al., 2002).

Nothing of substance can be said about process specifications since they are usually tailored to a given application and are often proprietary. An example of a possible sequence of steps was described by Reid et al. (2001) and shown in Figure 5.8. During the induction time (as illustrated) no current is applied when the wafer is exposed to the plating bath; the wafer is then at the floating potential (as illustrated). An alternative is to apply a very small current or a small cathodic potential immediately for cathodic protection. During the next step a relatively small current (the initiation current) is applied; the deposition rate is slow and the deposit is conformal, thickening, and perhaps repairing the seed layer. The final step is the fill step.

The way in which electrical contact is made to the wafer is very important to (1) ensure uniform potentials across the wafer and (2) to avoid the terminal or bipolar effect in which dissolution instead of plating occurs adjacent to a very resistive contact (Broadbent et al. 1999; Dordi et al., 2000). To ensure uniformity, one scheme provided a 128-point contact peripheral array under a lipseal (clamshell) (Broadbent et al., 1999; Patton and Fetters, 2000); another used a continuous peripheral contact together with nonconductive field shaping shields to reduce the thickness of Cu plated along the edges (Deligianni et al., 1999; Contolini et al., 2000). Dordi et al. (2000) advised using knife-edge platinum contacts to keep the contact resistance low and consistent to avoid bipolar behavior. An electrolytic cell containing a barrier (porous only to ions) to separate the anolyte and catholyte was designed to reduce the breakdown of additives, thereby minimizing power

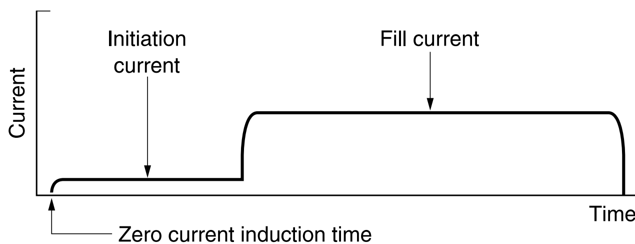

Figure 5.8 Two-step DC plating process. (Reprinted from Reid, J., *Jpn. J. Appl. Phys.* 40, 2650, 2001. With permission.)

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consumption and waste generation and improving bath stability and longevity. It also prevented particles generated at the anode from reaching the cathode causing defects in the plated film (Mayer et al., 2003). The cell is shown in Figure 1.48a (Chapter 1).

Voids/seams are almost always formed in films plated into high-AR features using additive-free electrolytes. They may be formed due to a potential drop in either the solution or the metal film or depletion of Cu^{2+} in the solution inside the feature. Depletion of Cu^{2+} generates an appreciable concentration overpotential and depresses plating inside the feature relative to the rate near the mouth. Thus the walls grow together near the top, closing the feature, leaving a void or seam. Potential variations in solution or in the metal film as well as convection are not important in submicrometer features (Takahashi and Gross, 1999). Increasing the bulk concentration of Cu^{2+} or decreasing the current density (c.d.) relieves the concentration overpotential as does stirring the bath more vigorously (Takahashi and Gross, 1999; Deligianni, 2002).

Vias are harder to fill completely than are trenches (West, 2000). “The main reason is the restricted nature of the via geometry. The shape of the evolving profile promotes depletion of the Cu^{2+}.” (Deligianni, 2003).

West et al. (1998) proposed pulse reverse plating as a way of completely filling features without the use of additives. Reverse current (dissolution) diminishes the void size. Chen et al. (1999) also used pulse plating and achieved void-free fill without additives. They reported that the waveform and its frequency had no significant effect for filling gaps 0.5 μm wide (AR ~ 2) as long as the c.d. was low. Pulse reverse plating is a slow process and does not appear to be extendable to much higher AR features.

The more efficient plating baths containing additives are now used routinely. Additives can be classified as suppressors (inhibitors), accelerators, and levelers (brighteners); it has been found that all or some of the additives are necessary to achieve void/seam-free fill, i.e., to produce bottom-up filling (also called superfilling, or superconformal filling) at reasonable rates. The net result of their action is increased deposition in interior corners and on the bottom of the feature and decreased deposition along the sides and at the top corners to prevent pinch-off. As the feature width decreases, it becomes more difficult to achieve void-free fill. The mechanism of superfilling depends on which additives are present and how they act and interact. Additives affect not only how well the features are filled but also grain size, resistivity, and surface smoothness, i.e., reflectivity. Unfortunately, in a number of reports the additives are not identified, making assessment of the results and comparison with other work difficult.

Suppressors inhibit the deposition of Cu. They are long-chain polymers, most often polyethylene glycol (PEG), usually used as a glycol–Cl^- mixture. Healy et al. (1992) proposed that a PEG film can be adsorbed on the Cu surface in two forms. Close to open circuit potential, it is as a CuCl/PEG complex; at more negative potentials where plating occurs, it is likely to be neutral PEG. Kelly and West (1998a,b) noted that addition of Cl^- alone promotes deposition and PEG alone has a relatively small effect. They proposed that Cl^- is necessary to maintain an adsorbed layer of PEG, and stated that the primary effect of PEG adsorption is blocking of available sites for charge transfer. Chang et al. (2002a), using pulsed plating, reported defect-free filling of 100 nm features (AR not specified) in an electrolyte containing $CuSO_4$, H_2SO_4, Cl^-, and PEG. A lower frequency was required for filling higher AR features. They suggested that the longer off-time “alleviated the concentration of Cu^{2+} in the gap.”

Cl^- also affects the plating process by complexing Cu^+ and Cu^{2+} (Gross et al., 1999). Cl^- also has an influence on grain structure; it inhibits growth of existing grains and favors formation of new nuclei so that small grains are formed (Gross et al., 1999). According to them “this inhibitory effect is critical to achieving void-free filling of sub-micron features” in baths with inhibiting (proprietary) additives and correlate the inhibition with the nucleation of the recrystallization process at these sites.

Accelerators are small S-containing organic molecules. Some of the ones used are bis(3)sulfopropyl disulfide (SPS), 3-mercapto-1-propanesulfonate (MPSA), and 4,5-dithiaoctane-1,8 disulfonic acid (DDDS).

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Levelers (often called brighteners) were used originally to smooth rough surfaces by causing metal to be deposited preferentially into a depression. They are organic compounds usually containing N or S groups. A nitrogen-containing dye, safrananne azo dimethyl aniline (Janus Green B, JGB), is one that has been used in feature-filling experiments together with the additives discussed above. Kelly et al. (1999), Madore et al (1996), and Madore and Landolt (1996) developed a model of cathodic leveling by blocking inhibitors based on a diffusion-adsorption mechanism. It included (1) transport of the leveling agent from the bulk to the cathode surface, (2) adsorption on the cathode surface, and (3) removal of by reduction. Although they verified their model by depositing Ni in the presence of coumarin, they claimed that the results were applicable to other systems.

Andricacos et al. (1998) developed a model of superfilling similar to that of Madore et al. (1996). It was based on "differential inhibition by diffusion-controlled additives" adsorbed on the surface. They stated that "because the additive is diffusion-controlled, shape-induced concentration-field effects drive a very wide rage of additive fluxes over the microprofile." Diffusion is sustained because the adsorbate is consumed, either by reaction or incorporation into the deposit. The inhibitor flux will be very low in bottom corners, low at the bottom of the feature, moderate on the sidewalls, and high at the top shoulders, ensuring differential deposition rates in the various parts of the feature so that there are no voids/seams in the deposit. The additives used in the experimental verification of the model were not described.

Kelly et al. (1999a,b) studied leveling of a grooved electrode. They found that leveling occurred only when four additives, PEG, Cl^-, SPS, and JGB, were present. This suggested that additive–additive interactions were operative. They were, however, unable to achieve 100% filling of trenches with an AR ~ 4, although they adjusted the c.d. and JGB concentration for optimal results. In later work it was found that if the concentration of JGB was too high (which depends on the SPS concentration) the leveling capacity of the bath disappeared (Taephaisitphongse et al., 2001). This was explained by assuming that, if a concentration gradient of leveling agent is required to produce the spatial variation in additive surface coverage, leading to preferential deposition at the bottom of the feature, then JGB coverage appears to saturate at high concentrations. Thus the concentration gradient can no longer affect the surface coverage of additive. Good (but not complete) filling was also obtained in the complete absence of JGB.

A phenomenon called overfill (Moffat et al., 2000) or bump formation (West et al., 2001) above the feature opening has more recently been observed during superfilling, using the additives PEG/Cl^- and SPS or MPSA. As the feature fills, the original concave surface profile becomes convex due to sustained acceleration of the growth within the feature. Under these conditions, the model of diffusion-adsorption of inhibitors does not apply. Both Moffat et al. and West et al. have proposed mechanisms for an accelerator-dominated process resulting in overfill as well.

Moffat et al. (2000, 2001) and Josell et al. (2001a,b) concluded that when the three additives are present, inhibition is provided by the interaction between PEG and Cl^- and the Cu surface, while acceleration is associated with competitive adsorption of MPSA (or a derivative) displacing the film derived from PEG–Cl^-. This conclusion was based on the current vs. overpotential characteristics that showed that PEG–Cl^- in the electrolyte inhibits growth and MPSA–Cl^- accelerates it. In their model of superfilling the kinetics and mechanism of the metal deposition reaction depends on the fractional surface coverage θ of a catalytic accelerating species. On patterned surfaces, local θ changes inversely to changes in the local surface area. During conformal growth, coverage increases on a concave surface, so that there is an increase in the local deposition rate. The opposite is true for a convex surface. When the catalytic surface species become sufficiently concentrated at the bottom, superconformal deposition occurs. As the deposit nears the top of the feature, the shape of the growth front changes and a bump is formed. Trench filling depends on the concentration of MPSA. If it is too low, θ is too low for enhanced deposition at the bottom; if it is too high, the surface is saturated and there is not enough spatial variation in deposition rate. At an optimum concentration, below saturation, all features were filled. Their simulation (which correctly predicted the experimental

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results) showed that the process has an incubation period of conformal growth as the concentration of the catalyst on the concave corners of the feature increases. It also predicted that a seam will be formed when the AR is too high. Josell et al. (2001a,b, 2002a,b) coined the acronym CEAC (curvature-enhanced accelerated coverage) for the mechanism of superconformal fill.

If the electrolyte was either additive-free, contained binary combinations of the additives (Cl-PEG, Cl-MPSA), or the corrosion inhibitor benzotriozole (BTAH), which is also an inhibitor of Cu deposition, voids were formed in vertical features. (As mentioned above (Chang et al., 2002), successful filling with a binary additive (Cl-PEG) was accomplished using pulse plating.) As in the case of other deposition techniques, features with sloping sidewalls were filled more completely. In ECD, reduction in void formation was attributed to geometric leveling associated with conformal deposition on the slanted walls. The slanted walls neutralize the influence of depletion of Cu^{2+} within the trench. In addition the opening is wider at the mouth compensating for the higher deposition rate there (Moffat et al., 2000).

The model of West et al. (1998) for superfilling in an electrolyte containing PEG, Cl^-, and SPS emphasized an interaction between PEG and SPS. It assumes that "superfilling is caused by an accumulation of the adsorbed accelerator (SPS) on the feature bottom as surface area available for deposition within a feature shrinks." They hypothesized a "transition from an inhibited to a noninhibited state at the feature bottom" due, probably, to an accumulation of SPS which lowers the surface coverage of PEG but does not block the charge transfer reaction. The local surface area for deposition changes as the shape changes, especially in the interior corners. The stages of the fill process are shown for several feature sizes in Figure 5.9a (West et al., 1998). The smallest features filled first. The highest bump height occurred over the smallest feature. There is an influence of the pitch as well; as the spaces became smaller, the bumps merged.

The difference in the height of a Cu film on a flat region and over a group of closely spaced trenches is shown in Figure 5.9b (Im et al., 2003). Ritzdorf et al. (2000) reported that the height of plated film increased as the pitch deceased; this can also be discerned in Figure 5.9b where the spacing increases toward the right. These differences have adverse affects on the CMP process. Ritzdorf et al. showed that inclusion of a leveler did reduce the bump height, but since seams were formed this was an unacceptable solution. The alternative approach, which accomplished a noticeable reduction in the height of the bump, was to modify the deposition parameters, c.d., waveform, fluid flow, and wafer rotation velocity after the smallest features were filled. The modified parameters were optimized to minimize the differences in height, but no details of this new process were given. They postulated that the effect of pitch is due to the fact that the additives incorporated in the Cu film remain at the surface as the feature is filled and continues to enhance deposition in areas where its concentration it greatest, i.e., in the narrow regions between the filled gaps.

Using the leveler 2-aminobenzothiazole (2-ABT) with Cl^- and PEG in plating resulted in a highly selective concentration gradient between the opening and the bottom of the feature because of its lower diffusion and consumption. Via holes 0.1 μm wide (AR = 10) were filled completely (no voids) (Lin et al., 2000d).

Another ternary electrolyte used to fill 100 nm wide AR = 10 features without voids is PEG-Cl-BTAH (Lin et al., 2002e). Using electrochemical analysis, Lin et al. found that a high concentration of BTAH inhibited the rate of Cu deposition whereas a low concentration accelerated it. Thus they termed BTAH a "hybrid-mode additive," enhancing deposition within the gap (low concentration) and inhibiting it at the opening of the gap (high concentration).

Chang et al. (2002b) used an acid–Cu electrolyte without levelers or brighteners for superfilling; the only additives were Cl^- and PEG with two different molecular weights (MW). They proposed that the lower-MW PEG (PEG200) with higher diffusivity transported Cu ions into deep features for bottom-up filling and the higher-MW one (PEG2000) reduced the interfacial energy between the electrolyte and feature openings to enhance filling capability. They showed filling of 0.13 μm vias (AR = 8), achieved only with *both* PEGs in the electrolyte.

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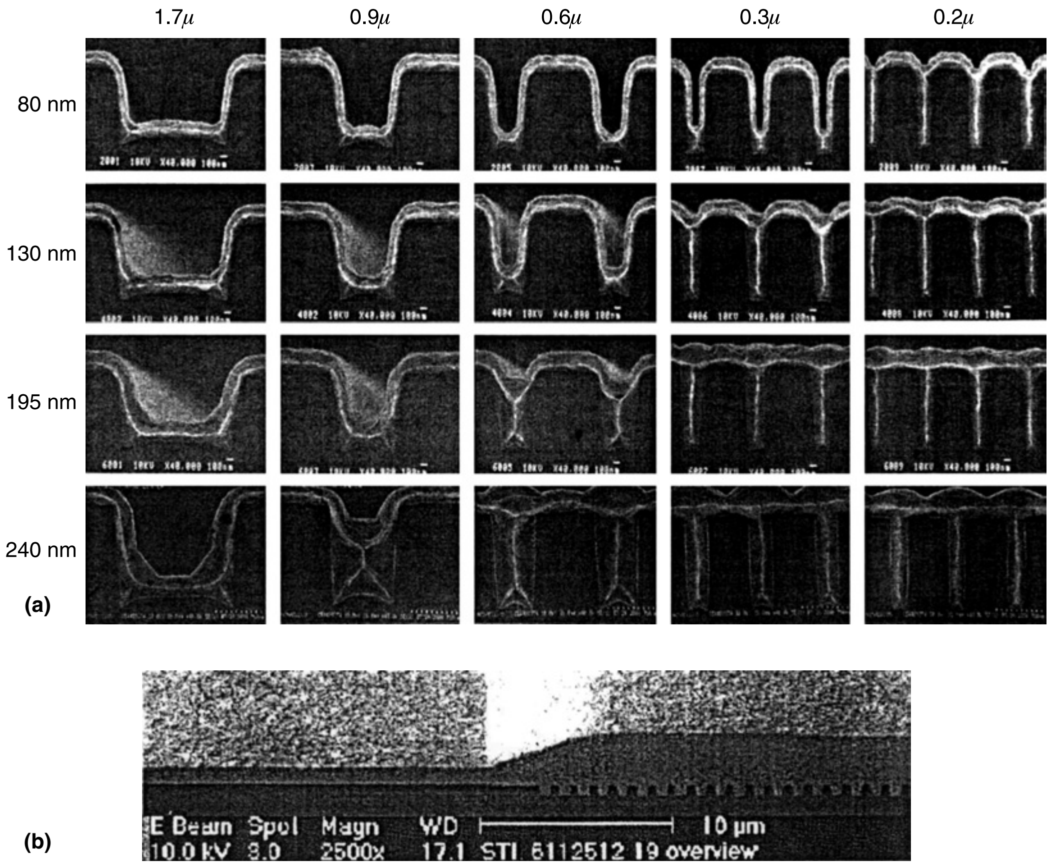

Figure 5.9 (a) SEM images illustrating, for various trench widths, the progression of trench filling by electroplated Cu at various stages (various thicknesses). (Reproduced from West, A.C., S. Mayer, and J. Reid, *Electrochem. Solid State Lett.*, 4, C50, 2001. With permission of the Electrochemical Society, Inc.) (b) SEM image showing height differences: flat region vs. group of closely spaced trenches. (Reproduced from Im, Y.H., M.O. Bloomfield, S. Sen, and T.S. Cale, *Electrochem. Solid State Lett.*, 6, C42, 2003. With permission of the Electrochemical Society, Inc.)

Moffat et al. (2000) studied the voltammetric behavior of various electrolytes and observed hysteresis in the case of a Cl-PEG-MPSA but not for binary combinations of Cl-PEG, Cl-MPSA, or additive-free electrolytes. They concluded that interactions among the constituents "led to an irreversible change in the reaction dynamics" and that "hysteresis reflects the competition between the rate of metal deposition and the accumulation and consumption of inhibiting additives, i.e., is a direct result of the alteration in the surface chemistry." They suggested that slow-scan voltammetry may be able to screen and/or optimize electrolytes for their filling potential and be a less ambiguous monitor than CVS.

5.4.4.4.3 Film Properties

In addition to filling high-AR features, the ECD process must produce films with a low resistivity (decrease RC delay), a suitable microstructure (improved electromigration resistance), and acceptable mechanical properties.

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The properties of a plated Cu film depend on the constituents of the plating bath, extent of contamination, temperature, and c.d. during plating, thickness, seed layer, and dimensions of the feature into which the Cu is deposited. The grain size of films deposited in an additive-free bath is large and stable and the resistivity is close to the bulk value. As-plated films deposited from baths containing the additives required for superfilling are fine-grained, shiny, and have a higher resistivity (~2.2 μΩ cm). The grain size and structure, resistivity, and mechanical properties of the films undergo a spontaneous transformation which is discussed in Section 5.9.2.5.

5.4.4.4.4 Jet Electrochemical Deposition (JECD) (Jet Plating)

This technique has been described as a superior and cheaper method of Cu plating for fabricating damascene structures. The essential component of the jet plating cell is the rotating anodes/jets assembly (shown in Figure 5.10). The wafer and anode, facing each other, are immersed in an electrolyte containing an inhibitor. The jets impinge on the surface of the wafer creating turbulence, reducing the diffusion layer significantly, and increasing the plating rate (and thus throughput) substantially. With the appropriate seed layer, the films are also brighter. The model proposed for filling is that while there is vigorous agitation on the flat surface, inhibiting deposition, the solution is essentially stagnant inside the openings. This results in a depletion of inhibitor so that plating is accelerated in the holes. Due to the enhanced supply of inhibitors to the wafer surface, a concentration gradient is established along the sidewalls of the opening. The lowest concentration of inhibitor is at the bottom which results in void-/seam-free superfilling of features with an exceptionally high AR (e.g., trenches 0.16 μm wide, 1.4 μm deep) (Cohen, and Tzanavaras, 2000, 2001).

5.5 TUNGSTEN

5.5.1 Introduction

Tungsten is a refractory material (m.p. 3370°C) with a bulk resistivity of 5.28 μΩ cm at 20°C. The possible forms of W are an amorphous phase, α-W, the equilibrium low-resistivity phase, and β-W, the high resistivity metastable phase.

Films can be evaporated but a high substrate temperature is required for low resistivity. Low-resistivity films can be deposited by sputtering, in all types of systems; a high sputtering pressure minimizes stress (Dori et al., 1990). However, CVD is the method of choice for most applications in IC fabrication.

5.5.2 CVD Tungsten

5.5.2.1 Introduction

CVD W has been used in the production of ICs chiefly as a contact plug and a vertical interconnection between successive wiring levels of multilevel devices. A contact plug connects the active and passive devices in the substrate to the first layer of metallization and to planarize the surface before that film is deposited. It also acts as a barrier, inhibiting interdiffusion and reaction between Si and the metal; this is discussed in Chapter 3. Its usefulness for vertical interconnects may be ending as new hole-filling deposition techniques for lower resistivity metals are developed and dual damascene processing takes hold. CVD W has also been used for gate electrodes and local interconnections (i.e., very short wires), replacing higher resistivity polysilicon.

CVD W can be deposited selectively, i.e., only on reactive surfaces, or as blanket films, i.e., non-selectively. Although it is toxic, corrosive, and highly reactive and readily hydolyzed in moist air to

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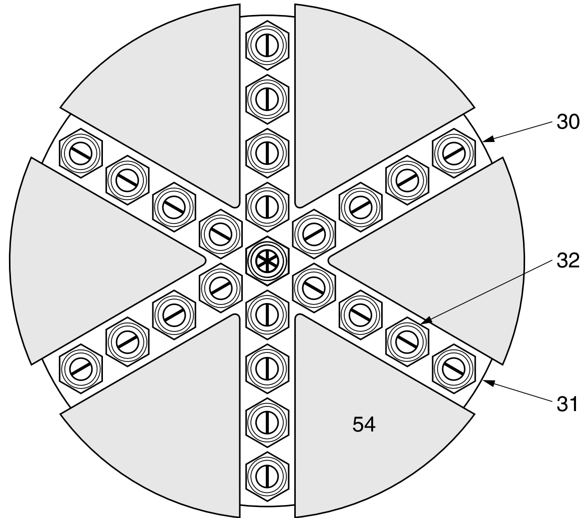


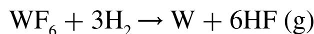
Figure 5.10 Schematic of the rotating anodes/jet assembly. (Reprinted from Cohen, U. and G. Tzanavaras, VMIC, 2000, p. 21. With permission.)

form HF, WF_6 is the most common source gas. LPCVD is the usual method of deposition although high-pressure CVD has also been studied. Both hot- and cold-wall reactors have been used.

PECVD has also been used, with various reactants, to deposit blanket W films, both in RF reactors (Tang and Hess, 1984; Greene et al., 1988a; Wong and Saraswat, 1988; Kim et al., 1991) and in an ECR system (Akohori et al., 1990). Other methods include laser-induced CVD (e.g., Mogyorosi and Carlsson, 1992), ion-enhanced evaporation (Joshi et al., 1987), and electron beam-induced deposition (e.g., Bell et al., 1994).

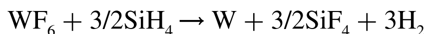
5.5.2.2 Blanket Deposition

The reaction used most frequently is the reduction of WF_6 by H_2:



$$WF_6 + 3H_2 \rightarrow W + 6HF\ (g)$$

SiH_4 reduction of WF_6 has also been used to deposit a seed layer before H_2 reduction, as described in a patent by Schmitz et al. (1990). The reaction is



$$WF_6 + 3/2SiH_4 \rightarrow W + 3/2SiF_4 + 3H_2$$

5.5.2.2.1 Reduction by H_2

This reaction may be preceded by the reduction of WF_6 by SiH_4, as shown above, or else by coating the surface first with a thin conducting layer, e.g., a sputtered metal film such as TiN, TiW as a seed or a barrier layer. These steps are taken to prevent a reaction with the underlying Si or Al since the reaction between WF_6 and these substrates is favored over reduction by H_2. The seed layer also acts as an adhesion layer. The deposition rate is increased by adding SiH_4 to the reaction mixture (Park et al., 1989). Under optimal deposition conditions, a conformal film can be deposited and holes filled without voids; this subject is discussed at greater length in Chapter 6. The film can be deposited at high temperatures and at high rates, since there are no selectivity restraints, but

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capping with WSi_x is required to prevent oxidation of the hot W surface as it emerges from the reactor, since *in situ* cooling reduces throughput unacceptably.

Joshi et al. (1993) patented a process for depositing W on nitride, using SiH_4 and reduction by H_2. Schmitz and Kang (1993) patented a two-step process in which the first W layer was deposited under conditions (temperature < 440°C, pressure = 20 to 100 torr, flow of $WF_6 \geq 0.15$ sccm/cm^2 of wafer surface) for forming void-free hole-fill and then by reducing the flow of WF_6 to no more than 0.05, produced a layer with low stress.

Reduction of WF_6 by B_2H_6 (+H_2) formed α-W with a low resistivity that was attributed to the lower F-content of the film (Hara et al., 1994), although Smith et al. (1994) reported that the films deposited from WF_6/B_2H_6 were high-resistivity W_xB_{1-x}.

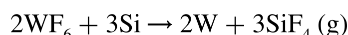
5.5.2.2.1.1 Mechanism: $WF_6 + H_2$ The deposition rate of W by the H_2 reduction of WF_6, under the conditions used for practical deposition, varies as the square root of the partial pressure (pp) of H_2 (i.e., rate ~ $P_{H2}{}^{1/2}$), and is independent of the pp of WF_6 (i.e., rate ~ P^0_{WF6}). The activation energy was found to be 0.71 eV, in the range of 250 to 500°C and pressure range of 0.1 to 5 torr. The agreement between this value of the activation energy and that reported for the H_2 surface diffusion on W led to the suggestion that the rate-limiting step was H_2 dissociation (Broadbent and Ramiller, 1984). An activation energy of 0.75 eV, reported by McConica and Krishnamanihi (1986) for a smaller temperature range, is in good agreement. Pauleau and Lami (1985) found that a rate-limiting step of dissociative adsorption of H_2 on W could not account for the large decrease in the rate of selective deposition of W when the deposition area increased but was, instead, the surface reaction between fluorine and hydrogen atoms in the adsorbed phase. McConica and Krishnamani (1986) also rejected adsorption of H_2 as the rate-limiting step.. The mechanism they felt was more in keeping with the way the reaction of H_2 actually occurs, was "addition of adsorbed monatomic hydrogen to adsorbed partially fluorinated W." They also pointed out that agreement with rate data does not prove a mechanism and that eliciting the true mechanism would require surface analyses. They re-stated the obvious that "since the reaction is a heterogeneous one, surface cleanliness is critical to film growth and purity." Desorption of HF from the W surface was another suggestion for the possible rate-limiting step for the $WF_6 + H_2$ reaction (Broadbent and Ramiller, 1984; McConica and Krishnamanihi, 1986). However, Bryant (1978) has shown that the reaction orders for this limiting reaction are 1/2 with respect to H_2 but 1/6 with respect to WF_6. At low temperatures and very low pp of WF_6, van der Putte (1987) did find that the rate was no longer independent of the pp of WF_6, and that the rate equation was $R = K(P^{1/2}_{H2})(P^{1/6}_{WF6})$, suggesting the rate-limiting step as desorption of HF.

5.5.2.3 Selective Deposition

This is essentially a hole-filling process. In a selective process, nucleation (initiation) occurs only on reactive surfaces; for hole filling, only the bottom of the hole must be reactive. It is more difficult to control than blanket deposition, but has the great advantage of requiring less WF_6 (an expensive reagent) and fewer processing steps since an adhesion layer is not required. Etchback of overfilled holes is less demanding. Since the film grows from the bottom of the hole, there are no seams or key holes in it. WF_6 can be reduced by Si, Ti, Al, SiH_4, and H_2.

5.5.2.3.1 Reducing Agents

5.5.2.3.1.1 Silicon The selective deposition of W on Si



$$2WF_6 + 3Si \rightarrow 2W + 3SiF_4\,(g)$$

is a self-limiting reaction. A thin film (~100 to 200 Å) is formed very rapidly; the limiting thickness is independent of time, temperature (270 to 450°C), and pressure (Broadbent and Ramiller, 1984; Saraswat et al., 1984; Broadbent and Stacy, 1985; Green and Levy, 1985). The thickness and

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physical structure depended on the surface preparation, i.e., the W/Si interface. Two models have been proposed to explain the existence of a limited thickness. Once a continuous film of W is formed, WF_6 cannot reach the Si surface to react. However, Si reduced W films deposited between 210 and 700°C were found to be porous and discontinuous. The porosity was said to be due to the evolution of the gaseous product, SiF_4; the pores might be remnants of these bubbles (Green et al., 1987). Amorphization of the Si surface by ion implantation decreased the nucleation barrier and allowed the formation of thicker films at lower temperatures (Green et al., 1986). Another proposal was that the presence of a nonvolatile lower fluoride of W was the inhibitor of further reaction between WF_6 and Si. This hypothesis was supported by the presence of F in the W film (Lifshitz, 1987; Park et al., 1988). A pinhole theory was proposed by Broadbent and Ramiller (1984) but was refuted by Green et al. (1987).

Although all the Si-reduced W films are self-limiting, the thickness reached is not always the same. A limiting thickness of 60 Å (equivalent of full-density W) was reported to be formed at < 310°C. The thickness reached a maximum value at 340°C and decreased with increasing temperature, leveling off at about 200 Å. The temperature dependence and the self-limiting behavior were believed to disprove that the reaction is diffusion limited. The reaction might be controlled by factors such as the temperature dependence of nucleation, sticking coefficient and desorption of intermediates, an atomistic reduction mechanism, and other (unstated) mechanisms; this could also explain the surface sensitivity (Green et al., 1987).

A dependence of the limiting thickness (> 400 Å) on both the doping condition of Si and the surface preparation has also been reported (Tsao and Busta, 1984). An advantage of the use of W as a barrier layer between the Si and the interconnections metallization (usually Al-based) is the low and tightly distributed contact resistances, particularly in small contacts (Shibata et al., 1984).

However, what have been called wormholes and tunnels, empty channels with a W particle at the end, are formed at the W/Si interface at the rim of a contact window (Green and Levy, 1985; Stacy et al., 1985; Yang, et al. 1987). Tunnels are shown Figure 5.11.

Three atoms of Si are for every two atoms of W formed; the thickness of W deposited has been observed to be about half the thickness of Si consumed (Tsao and Busta, 1984). Since this is an isotropic reaction, there is lateral encroachment at the Si/SiO_2 interface (Moriya et al., 1983;

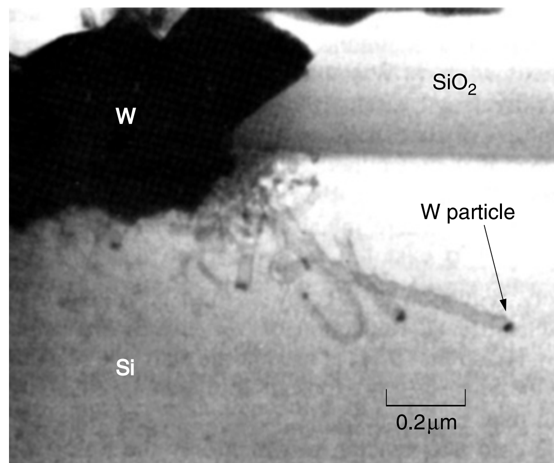

Figure 5.11 SEM image showing tunnels into Si after selective CVD of W. (Reproduced from Stacy, W.T., E.K. Broadbent, and M.H. Norcott, *J. Electrochem. Soc.*, 132, 444, 1985. With permission of the Electrochemical Society, Inc.)

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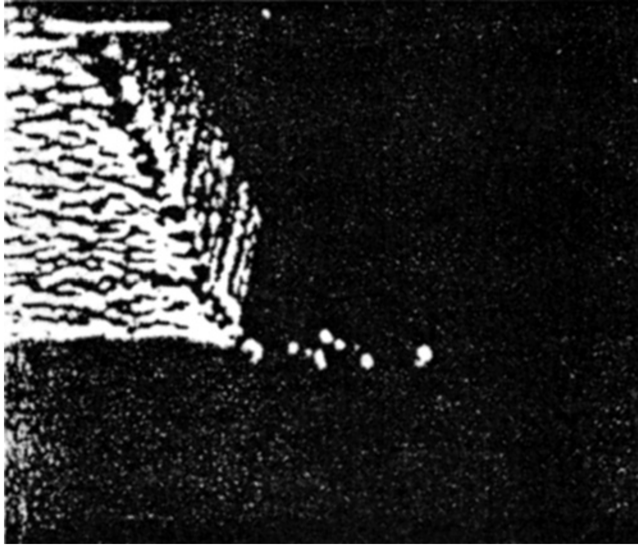

Figure 5.12 SEM image showing encroachment due to selective CVD of W. (Reproduced from Moriya, T., K. Yamada, T. Shibata, H. Iizuka, and M. Kashiwagu, Symposium on VLSI Technology, 1983, p. 96. With permission of IEEE. Copyright 2004.)

Stacy et al., 1985), as seen in Figure 5.12. The lateral encroachment distance increases with increasing partial pressure of WF_6 and temperature. Encroachment can be minimized by the use of the proper pressure and substrate temperature, which at the same time, improves selectivity (Moriya et al., 1983). Wormholes and encroachment are particularly serious when thick films are deposited. They lead to junction degradation, i.e., high leakage currents.

Several process modifications have been proposed to limit consumption of Si. Addition of SiF_4 to WF_6, by shifting the equilibrium of the $WF_6 + Si \leftrightarrow W + SiF_4$ reaction, inhibited erosion and encroachment of the Si contacts and resulted in improved performance (Levy et al., 1986). An interlayer, blanket WSi_x, followed by W deposition under selective conditions, prevented excess Si loss and filled contacts without keyhole formation (Hieber and Stolz, 1987). Coating the contact holes with amorphous Si by sputtering at room temperature replaced the Si substrate which would have been consumed from the contact holes during the $WF_6 + Si$ reaction. Therefore, consumption of the diffused layer and encroachment was reduced (Kakiuchi et al., 1987). Selective deposition could be maintained and thick films formed while suppressing Si consumption, tunneling, and encroachment by using SiH_4 as the reducing agent in a range of $SiH_4/WF_6 < 1.5$ (Kusomoto et al., 1988; Gorczyca et al., 1989). The SiH_4 reduction reaction has the potential for higher deposition rates (e.g., 0.6 μm/min) than other reduction reactions, but when the SiH_4/WF_6 ratio exceeded ~1.6, although the rate was higher, blanket deposition occurred. There is the potential for forming a damage-free surface because there is no interaction with the Si substrate and no HF production. In this case, a cold-wall reactor was used (Tsutumi et al., 1990). Feinerman (1990) found that surface treatment in a dilute HF/HNO_3 mixture minimized encroachment, whereas exposure to a CF_4/O_2 plasma maximized it. GeH_4 reduction of WF_6 was proposed as an alternative reaction. β-W containing ~10 a/o Ge was deposited selectively without harmful consumption of Si, tunnels, or encroachment. Contact resistivity to both n^+ and p^+ Si was low, the β-W stable to 600°C, and the adhesion of the W to Si was excellent (van der Jeugd et al., 1990, 1992).

Another phenomenon, creep-up in contact holes, has been observed. After W has been formed on the Si surface in a contact hole, the growth continues along the SiO_2 sidewalls, forming a

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collar (Itoh et al., 1985). The collar affords extra protection at the edges of a contact hole where metal coverage by an overlying metal may be thinned.

5.5.2.3.1.2 Hydrogen To grow thick films selectively, reduction of WF_6 by Si must be followed by reduction by H_2 (Blewer and Wells, 1984). Reduction of WF_6 by Si is favored energetically over the reduction by H_2, so that if H_2 is used at the start, the reaction with Si will still occur so long as the Si surface is exposed. To maintain selectivity, low temperatures, i.e., low growth rates, are used.

The introduction of a LPCVD cold-wall reactor, in which only the wafer was heated by a lamp or hot plate, allowed rapid selective growth of W (by the reduction of WF_6 by H_2) in interlevel vias on Mo interconnection metallization. Mo does not react with WF_6 and so is an excellent substrate for the $WF_6 + H_2$ reaction (Stoll and Wilson, 1987). The high rate implied a high deposition temperature. Any metallic impurities were scrupulously removed from the surrounding oxide surface to prevent nucleation (loss of selectivity). This process allowed complete filling of deep vias. If vias of different depths were present, the excess W in the shallow vias could be etched off using a sacrificial resist process (Saia et al., 1987). Such a process would be useful only where resistivity requirements are not stringent since the resistivity of bulk Mo is 5.34 $\mu\Omega$ cm at 20°C. A highly selective deposition of W on Si used alternating cyclic hydrogen reduction of WF_6. Hydrogen reduction was interrupted periodically to vaporize incipient precursor nuclei formed on the oxide surfaces via the disproportionation reaction forming WF_5 from W and WF_6 (Rieseman et al., 1990). Selective deposition of W in a polymeric matrix was accomplished using rapid thermal LPCVD and a mixture of $WF_6/H_2/SiH_4$. α-W was always obtained and had a resistivity of ~20 $\mu\Omega$ cm (Bouteville et al., 1991).

5.5.2.3.1.3 Titanium Ti can reduce WF_6 but the resulting structure consisted of clusters of W on a layer of TiF_3 (Broadbent et al., 1986).

5.5.2.3.1.4 Aluminum There have been two problems associated with depositing W on an Al surface. One is high interface resistance, due to a surface film of AlF_3; the other the inability to nucleate W rapidly, reproducibly, uniformly, and then to grow a smooth thick film without loss of selectivity.

The reaction byproduct is involatile AlF_3, trapped at the interface, increasing interfacial resistance (Broadbent and Ramiller, 1984; Broadbent and Stacy, 1985). However, Hey et al. (1986) reported that although the via resistance was higher than for an Al–Al contact, it was acceptable. They postulated that the larger contact area of the interface alleviated the problem caused by the AlF_3 insulating film. The W was deposited at a temperature below that used to deposit the Al so that hillock growth was suppressed.

Low via resistance was achieved by controlling two parallel reactions, the reduction of WF_6 by H_2 and Al, in a single step in a cold-wall reactor described above, in which the deposition temperature was high, while selectivity was maintained. Several explanations have been proposed to explain the effect of the higher deposition temperature on the via resistance. One is that at the higher temperature, AlF_3 was more volatile. Another is that the shortened reaction time allowed less AlF_3 to be formed before the surface was covered with W, i.e., W would cover the Al surface before it could react extensively with WF_6. An additional reason is that at high deposition rates, less or no F is expected to stay at the interface (although the fluorination of Al surfaces occurs readily) (Chow et al., 1987; Wilson et al., 1987; Kang et al., 1988).

W deposition did not take place on the plasma-oxidized Al surface formed during resist ashing and no F was detected after exposure to WF_6. In the absence of ashing (just native oxide on the Al surface), W layers could be formed reproducibly after cleaning the Al surface by brief etch in hot concentrated HCl. Low levels of F were found at the interface. Since a wet pretreatment was

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thought to be unacceptable, deposition of a thin (but not too thin) layer of W was sputtered directly on the uncleaned Al surface before exposure to WF_6. These authors reported that accumulation of F was correlated with aluminum oxide, not bare Al. They concluded this because when both W and uncleaned Al surfaces were exposed to WF_6 (the surface condition when the W film was too thin), high concentrations of F were detected at the interface (Ng et al., 1987). Immersion of the Al surface in a dilute HCl solution before CVD W deposition was reported to improve the via resistance, although it was still substantially higher than that of an Al/Al interface (Oshima et al., 1993).

Other processes have been developed to improve the nucleation of W on Al; they involve pretreatment of the Al surface and successive reduction by H_2 and then SiH_4. One consisted of a brief etch in a very dilute HF solution, followed by a dry pretreatment. The most satisfactory was a short exposure to a BCl_3 and then a H_2 plasma or to H_2 gas at an elevated temperature; this resulted in a uniform W film at the bottom. SiH_4 was used for the final W growth step, ensuring minimal selectivity loss (Hintze et al., 1994; Schulz et al., 1994). Preparing sputtered W and TiN capped Al surfaces for CVD W deposition required the HF dip and exposure to an NF_3 plasma. In the case of TiN, etching was stopped before the Al surface was exposed. Then the H_2/SiH_4 reduction was carried out (Schulz et al., 1994).

Another process started by removing polymeric residues using an HF/ashing/HNO_3 sequence followed, without further pretreatment, by a two-step W CVD process: H_2 reduction at 350°C, then SiH_4 reduction at 280°C. This sequence resulted in a very low F level at the W/Al interface, with an acceptable via resistance, smooth films, and favorable selectivity (Bae et al., 1994).

5.5.2.3.1.5 Reduction by SiH_4 The growth rate of selective W was proportional to the partial pressure of SiH_4 and decreased slightly with increasing partial pressure of WF_6. The activation energy was slightly negative, indicating competition between adsorption/desorption processes and surface reactions, i.e., adsorption of SiH_4 and competition between film formation on the surface and byproduct desorption. The growth rate was inversely proportional to the exposed area indicating a reactant supply limited reaction. The resistivity of the film increased with higher deposition rates and lower deposition temperatures (Colgan and Chapple-Sokol, 1992).

A two-step process is described in a patent by Joshi et al. (1993), using a flow ratio of $SiH_4/WF_6 < 1$ for the deposition of an initial layer of W selectively on Si, at temperatures about 500°C (430 to 480°C preferred) followed by reduction of WF_6 by H_2 at temperatures ≥ 500°C for the rest of the film.

5.5.2.3.2 Mechanisms

5.5.2.3.2.1 $WF_6 + SiH_4$ The apparent activation energy for this reaction varied with both temperature and pressure, suggesting multiple kinetic regimes. The kinetics were modeled to include three competitive reactions of surface-adsorbed WF_6: (1) reduction by SiH_4, (2) dissociation of SiH_4 and reduction by Si, and (3) reduction by H_2 (formed in (1) and (2)). Since the relative importance of each reaction pathway is highly dependent on process and system conditions, it was difficult to establish a universal rule for the process trends. Reactions (1) and (2) have near zero activation energies and for (3), as stated above, $E_{act} \sim 0.7$ eV. A deposition regime controlled by (2) occurs when the ratio SiH_4/WF_6 is too high and loose β-W films and gas phase nucleation can result (Hsieh, 1993).

An alternative reaction mechanism in which a fluorinated W surface is reduced by both surface-absorbed SiH_x and impinging SiH_4 molecules was proposed by Bolnedi et al. (1994). The model predicted the effect of a varying SiH_4/WF_6 pp ratio (R) on (1) the observed shift in the apparent SiH_4 and WF_6 reaction order and on (2) the conformality of the deposit. For values of $R < 0.3$ there is a first-order dependence on SiH_4 pressure ($m = 1$) and zeroth-order dependence on WF_6 pressure ($n = 0$). At higher ratios ($0.5 < R \leq 1.0$) the orders are shifted to $m = 2$, $n = -1$. It was concluded that “the unique reaction order shifts observed can only be explained by parallel reaction pathways,

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both of which contribute to the overall deposition rate. Although one or the other may be the dominant pathway under given conditions." "For low values of R, when $m = 1$, the sticking factors are flux independent and the deposit is conformal. For higher values of R, $m > 1$, the sticking coefficients increase with increased SiH_4 flux and the conformality degrades."

5.5.2.3.3 Prediction of Selectivity; Loss of Selectivity

Selective deposition is difficult to control. The important factors are pressure, flow rate, and surface preparation/area. According to Carlsson and Bowman (1985) "selective CVD (of W from the WF_6/H_2 reaction) is based on a difference in thermochemical stability between different substrate regions; the higher the difference, the higher the selectivity." Selective W deposition on Si is favored by low temperature and total pressure and a high concentration of WF_6 in the initial stages of deposition. Low temperatures means slow growth and long deposition times but long deposition times, whether due to the rate or the final thickness required, compromise selectivity. As W is formed and growth now occurs on the W surface, the selectivity is less but increases with decreasing WF_6 concentration and increasing temperature. This suggests a two-stage operation should be used. A high temperature increases the probability of reaction with SiO_2 and etching of the oxide may occur. They concluded that temperature was the most important parameter for maximum selectivity and minimum attack of oxide.

Loss of selectivity has been linked to an increase in the HF concentration in the reactor; a high flow rate, reducing the residence time of HF on SiO_2, will, therefore, improve selectivity (Pauleau and Lami, 1985; Korner, 1989). Nuclei were formed more readily on nitride than on oxide surfaces and the presence of P (as a surface treatment or as PSG) inhibits nucleation (Bradbury and Kamins, 1986). Metallic contaminants (residues) on the insulator are sites for H_2 reduction of W (Blewer, 1986). Increased numbers of wafers or exposed area degrade selectivity as do improper cleaning, ion implantation, or exposure of the surrounding regions to a plasma (Saraswat et al., 1984). Selectivity loss was found to be caused by the transport of W from the W surfaces to the surrounding oxide. The mechanism was desorption of tungsten subfluorides from the W surface and transport to the other surfaces where they are condensed and disproportionated, leaving on the oxide a reactive state of W which catalyze the reaction between H_2 and WF_6 (Creighton, 1989). A similar model was developed by Desatnik and Thompson (1994), who found that the amount of nucleation on SiO_2 decreased with increasing distance from the metallic surfaces. The model developed was that a short-lived reactive gaseous intermediate diffuses from the metal to the SiO_2 where it reacts to form nuclei in clusters. Nucleation was favored at higher temperatures and increased as the process progressed. McConica et al. (1988), however, developed a model that predicted that *high* temperature, low pp of WF_6, minimal hot-metal area, and deep narrow vias enhance selectivity.

Loss of selectivity in the WF_6/SiH_4 process can occur when $[SiH_4]/[WF_6] < 0.3$ was found to be due to an autocatalytic reaction on the SiO_2 surface, the formation of Si_2H_{2n} from two adjacent SiH_4 molecules on a nucleation site (impurity or adjacent metal area). Formation of this intermediate is retarded by WF_6 chemisorption on the site but, once formed, reacts rapidly to a W-containing species (perhaps W_2F_2, W_2F_6). At monolayer coverage, further reaction with Si_2H_{2n}, forms W which acts as nucleation sites. At relatively high SiH_4 densities in the reactor, the Si_2H_{2n} species react with each other to form Si clusters which react with WF_6 to form W, at a reactant ratio >1. If it were possible to remove the W-containing species selectivity would be maintained (Groenen et al., 1994).

5.5.2.4 Preferred Method of Deposition

The problems discussed above have led to the use of a liner of Ti/TiN, formed by sequential CVD or directional sputtering, and then CVD W by reduction of WF_6 by H_2 or SiH_4 or mixtures of

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them. The excess W can be removed by RIE, but more commonly now, by CMP. The metal–silicon reactions are covered in greater detail in Chapter 3.

5.5.2.5 Properties of CVD W

The films formed by the WF_6/H_2 reaction are polycrystalline, with a grain size of ~2000 Å, a tensile stress of 7×10^9 dyne/cm^2, and a resistivity of 13 $\mu\Omega$ cm for a film ~1000 Å thick, decreasing with increasing thickness, tending toward the bulk resistivity of 5.3 $\mu\Omega$ cm. The contact resistance to both n^+ and p^+ contacts is low and it is a good diffusion barrier between Al and Si up to 450°C. The oxygen content of the film increased with increased deposition temperature or decreased thickness; it was concentrated at grain boundaries. The F content decreased with increasing temperature but was independent of thickness (Green and Levy, 1985; Learn and Foster, 1985).

5.6 PATTERNING OF ALUMINUM AND ALUMINUM ALLOYS

5.6.1 Wet Etching

A widely used etchant for Al and its alloys is a mixture of phosphoric, nitric, and acetic acids in water. Others can be found in a listing by Kern and Deckert (1978). Because of the fine dimensions required for VLSI and ULSI interconnections, wet etching for pattern definition has long been discarded.

5.6.2 Sputter Etching; Ion Milling

These techniques can be used to pattern any metal and is compatible with the small dimensions, but they are not used widely because of the superior results obtained by using reactive plasmas in manufacturing environments.

5.6.3 Anodic Oxidation of Al

One of the early attempts to improve dimensional control was the use of anodic conversion of Al (in pure Al or AlCu alloy) to Al_2O_3, i.e., conversion of the unwanted metal to its oxide instead of etching it and depositing a dielectric in the spaces thus formed (Platter and Schwartz, 1974a). This process had some advantages. The line width was increased, as compared with wet etching using the same mask (the taper angle was ~60°). The surface was planarized. Monolithic vertical interconnects were easily fabricated (Platter and Schwartz, 1974b). However, the value of ε for the oxide is high and the manufacturability of the process was doubtful. A better replacement for wet etching was the lift-off process and eventually RIE. The technique was revived by Surganov and Mozalev (1997); they stated the advantages as reduced production time/costs, simpler processes, and increased reliability but ignored the high ε of Al_2O_3.

5.6.4 Additive Processes

5.6.4.1 Lift-Off

In this process the appropriate patterns (interconnects, vias) are formed in a disposable matrix which is dissolved (lifted-off) after deposition of the metal. It was used widely for Al and Al alloy patterning as an improvement over wet etching for dimensional control and over anodic oxidation for process simplicity.

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Among the first of these processes to be used extensively employed a trilayer structure. It consisted of a thick base layer of a hard-baked resist (which accommodated topography differences and withstood elevated metal deposition temperatures and *in situ* sputter cleaning), an inorganic layer, called a barrier layer (which does not etch in an O_2 plasma) and a photoresist film (used to pattern the inorganic layer). In the first version (Franco et al., 1975) the barrier layer was a metal, but transparent barrier films (for improved overlay capability) soon replaced it. Openings were formed in the barrier layer; these corresponded to the metal interconnection pattern (the inverse of a metal etch mask). This layer was used as a mask during RIE in O_2 of the underlying polymer layer. The RIE conditions were such that the inorganic layer was undercut, i.e., an overhang or ledge was formed; the edges of the overhang defined the width of the metal line. *Any* metal may be evaporated into the lift-off stencil. The undercut in the stencil and directional deposition of evaporation kept the edges of the metal from touching the polymer walls, but at times a thin layer of metal extended from the bottom of the metal line, reaching the base of the stencil, making clean lift-off more difficult (Dinklage and Hakey, 1984). The final steps were dissolution of the stencil in a hot solvent which removes the unwanted metal deposited on top of the stencil, followed by rinsing and drying the wafer. The sequence of process steps is shown in Figure 5.13.

A modification substituted a soluble polyimide for the hard-baked resist (Milgram, 1983). Several other closely related processes have been patented. In one the use of sputtered metal was allowed, but the cusps extending from the body of the metal at the bottom of the stencil had to be etched off (Sebesta, 1985). Shibata (1986) used a stencil made of a composite of resist and plasma deposited SiN.

A single-layer stencil, which did not involve RIE, was developed by Hatzakis et al (1980). It involved soaking a positive photoresist layer in chlorobenzenene to produce differential solubility during development. This resulted in an overhang and an undercut profile. A scheme that relied on the taper angle of the resist but did not need an overhang was described by Batchelder (1982). Separating the metal from the mask required that the metal be etched in resist developer which did reduce the linewidth.

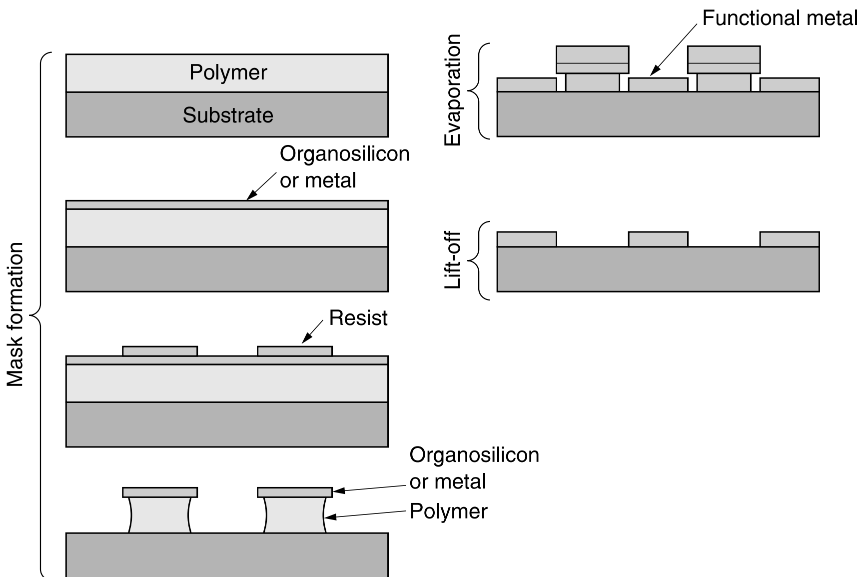

Figure 5.13 Process sequence for forming a metal pattern by lift-off. (Reproduced from Fried, L.J., J. Havas, J.S. Lechaton, J.S. Logan, G. Paal, and P.A. Totta, *IBM J. Res. Develop.*, 26, 363, 1982. With permission.)

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An image reversal process was the next development. Reversed images have negatively sloped undercut profiles that are ideally suited for lift-off processing. The process steps are: exposing a positive resist, baking it at 100°C, exposing it to blanket illumination, and finally developing it. The top of the mask defined the metal width (Moritz, 1985).

Another single-layer stencil was formed by exposing and developing a resist layer, using no profile-shaping procedures. Either evaporated or sputtered metal could be used. After deposition, a second layer of resist applied; since it is thinnest at sharp edges, a controlled etchback broke through in that region, exposing the metal which was etched just to clear the sidewalls of the stencil which could then be removed (Pai et al., 1986). In addition to flexibility with respect to the choice of metallization, there was a great improvement in cross-sectional area compared with both wet etching and anodization; the metal taper angle usually varied between 80° and 85° in most of the lift-off processes. Another advantage of a lift-off process is the ability to expose underlying conductors in a via hole without subsequent attack when patterning the upper metal layer. Highly stressed metals may be used since only limited areas are formed (Fried et al., 1982). One disadvantage of many of the processes is the requirement of line-of-sight evaporation which limits step coverage. The lines are tapered which limits the packing density. The real limit lies in the minimum pitch obtainable. In lift-off patterning, it is not the width of the conductor that limits its usefulness (as it is in subtractive processes) but the space between the lines. The minimum space is determined by the mechanical and adhesive strength of the stencil which defines it. If the stencil is too narrow, it may fall over or collapse or be easily undermined during the premetal processes (Homma et al., 1981). Another problem occurred when using a trilevel stencil (with an evaporated or PECVD oxide barrier layer) to form the vertical interlevel interconnects (studs). Although the process had been used successfully in forming the conductors on a single level, the studs, in the outer regions of an array, or in an isolated position appeared to be corroded; when viewed in the optical microscope, they appeared black. SEM examination, however, showed that this was an optical illusion; the studs were severely tapered and taller than those in the center of an array. The distortion did not depend on the organic material used for the stencil, could not be eliminated by any processing changes, e.g., improved solvent removal, prolonged baking or elimination of sputter cleaning prior to metal deposition, etc. Since this distortion was not observed when an SiO_2 stencil was used (an impractical solution), outgassing during metal deposition was an obvious culprit. Only along the openings made for conductors or for studs in the middle of an array were there sufficient pathways for removal of the products. The solution was providing a permeable barrier layer, a large area through which the volatile product could escape. The problem was solved when PECVD HMDS was substituted for the usual, but impermeable, barrier materials (Schwartz, 1991).

Although many other versions of lift-off processes have appeared in the literature, both the limitations of the process and the advent of commercially available reactive plasma-etching reactors designed to etch metals eventually led to the abandonment of lift-off for metal patterning.

5.6.4.2 Embedment

In this case, the Al or an alloy is deposited into patterns formed in a permanent dielectric. This is discussed more fully in Chapter 6.

5.6.5 Reactive Plasma-Assisted Etching of Al and Its Alloys

5.6.5.1 Introduction

Among the earliest reports of plasma-assisted etching of Al was one by Hosokawa et al. (1974), using fluorochlorohydrocarbon gases as etchants. RIE in halogenated gases, such as Cl_2, Br_2, I_2, HCl, HBr, CCl_4, was patented by Harvilchuck et al. (1976) and later described by Schaible et al.

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(1978). Fluorine-based gases were excluded as etchants since AlF_3 is involatile. Compared with Br-based etchants, the Cl-containing compounds were easier to handle and not as destructive of the existing pump oils and other components of the vacuum systems. Although the vapor pressure of $AlCl_3$ is slightly lower than that of $AlBr_3$ below ~125°C, its vapor pressure is adequate at the use temperatures. Thus, Cl-containing etchants have been used more widely than Br-based ones, despite corrosion and resist-interaction problems. I-based plasmas have not been used in any practical process. The toxicity of many of the reactants and products/byproducts makes operator safety an important consideration in RIE of Al.

5.6.5.2 Mechanism of Etching Al in Halogen-Based Etchants

5.6.5.2.1 Al + Cl_2 or Br_2: Spontaneous Etching

The native oxide on the Al surface protects it from attack by corrosive species. Once the oxide is removed, Cl_2 and Br_2 etch Al spontaneously, i.e., isotropically. The spontaneous nature of the etch by Cl_2 was demonstrated by Poulsen et al. (1976) who showed that once the etch process has been started (i.e., the protective oxide removed) the plasma could be extinguished and Al would continue to be etched as long as Cl_2 was kept flowing though the reactor. Plasma beam/mass spectroscopic studies in an ultrahigh vacuum were carried out by Smith and Bruce (1982). They found that after the native oxide was removed, the Al etch rate in Cl_x^+ was unaffected by beam bias or plasma power and the rate remained the same even when the plasma was extinguished. They concluded that the etch product was $AlCl_3$ since the appearance potentials in the mass spectrometer of all the $AlCl_x$ fragments were the same as those obtained for sublimed anhydrous $AlCl_3$ crystals. Although at low temperature (33°C) the primary product is the dimer (Al_2Cl_6) and $AlCl_3$ forms at higher temperatures (Winters, 1985), the product is almost universally referred to as $AlCl_3$ when discussing RIE of Al in chlorinated plasmas. Park et al. (1985) observed that clean Al films etched spontaneously in both Cl_2 and Br_2 beams at room temperature without ion bombardment and that the rates were approximately proportional to the halogen molecule pressure and were not enhanced significantly by Ar^+ bombardment. Under bombardment, the rate was approximately the sum of the spontaneous and physical etch rates. Ion bombardment did not change the chemical states of the halogenated Al species significantly. Dissociative chemisorption of the halogen on a clean Al surface seems to be the rate-limiting step and the sticking coefficient was not changed by ion bombardment. The rates of surface diffusion and reactant desorption were high; the surface coverage of the etch product was very low (~0.1 monolayer). Molecular Cl_2 etches Al four times faster than do Cl atoms, probably due to the enhanced sticking coefficient between the molecule and chlorine bound to the surface. Below 25°C, etching was quenched; this was postulated to be due to the inability of the products and/or contaminants to desorb (Danner and Hess, 1986b).

Despite the insensitivity of the Al + Cl_2 reaction to ion bombardment, increased ion energy does increase the etch rate in practical etch systems (e.g., Purdes, 1983). This apparent contradiction is due to the fact that ion bombardment is required to remove surface contaminants (which exist in a RIE system as opposed to an ultrahigh-vacuum system) and expose the Al surface to the reactants. At pressures as low as 2 mtorr, etching of Al in a helicon reactor was via a chemical reaction (Jiwari et al., 1993). Steinbruchel (1986) concluded that in reactive ion beam etching, direct reactive ion etching, i.e., the chemical reaction between the substrate and a reactive ion to form a volatile species, was a component of the etch mechanism.

5.6.5.2.2 Native Oxide Removal: Initiation or Induction Period

It is clear that the native oxide must be removed before the bulk of the film can be etched. The etch rate of the oxide, in a CCl_4 plasma for example, is about two orders of magnitude slower than

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that of the unoxidized Al (Tokunaga et al., 1981); the etch rate of the oxide is always significantly less than that of Al in any plasma, be it reactive or inert. The oxide film can be sputter-etched by inert ions or by those produced in the etching plasma, but since reoxidation is energetically favored, it can be reformed readily by the residual gases (largely water vapor and air). A hypothesis to account for the improved performance of CCl_4 over Ar in initiating etching was that CCl_3^+ is heavier than Ar^+ and therefore more efficient in sputtering the native oxide (Schaible et al., 1978). But this explanation is untenable since it has been shown that molecular ions are completely dissociated upon impact with the substrate (Steinbruchel, 1984). The improvement is due, in part, to the chemical reduction of Al_2O_3 by radicals formed in the plasma from the parent molecule: CCl_x (fromCCl_4) (Poulsen et al., 1976), BCl_x (from BCl_3) (Poulsen et al., 1976; Ingrey et al., 1977), $SiCl_x$ (from $SiCl_4$) (Danner et al., 1987), and BBr_x (from BBr_3) (Keaton and Hess, 1985). Ion bombardment assists the reaction. Initiation time was longer in BBr_3 than in BCl_3, most likely because the etch rate of the oxide was lower. However, another property of the radicals is, perhaps, more important; it is the ability of the radicals to scavenge oxygen and water vapor and so prevent reoxidation. The scavenging efficiency is $BCl_3 > SiCl_4 > CCl_4$ which may be explained by thermodynamic considerations and steric effects (Danner et al., 1987); the scavenging effect of BCl_3 and BBr_3 should be similar (Keaton and Hess, 1985). The initiation period, i.e., the time required to remove the native oxide and start etching the bulk Al, is thus a combination of sputter- and chemical-etching the oxide while preventing reoxidation of the Al. It is generally agreed that the initiation period is shortest in BCl_3 plasmas but that precautions must be taken to reduce moisture contamination in the reactor to minimize the occurrence of nonreproducible total etch times. Vossen (1983) suggested pretreatment by a hydrogen glow discharge for improving variable induction times, but this does not appear to have been used widely. Other means of reducing the moisture in the reactor are keeping the chamber walls warm at all times, extending the pump-down times, using a cryogenic trap, and installing entrance and exit load locks; this last is now an integral part of modern metal etchers.

Anodization is a method of forming surface oxide films of known thickness (e.g., Young, 1961). Thus a direct correlation between the oxide thickness and initiation time and its influence on total etch time was demonstrated by etching-to-completion Al films which had been anodized to form different thicknesses of oxide (Schwartz et al., 1986).

If there are nonuniformities in the surface oxide, the differential between the etch rates of the oxide and bulk Al can produce random surface roughness and, at times, distinct residues (Chapman and Nowak, 1980).

Slow etching of the oxide layer increases the difficulty of RIE of a metal film deposited over a step because oxide etching is directional and the vertical oxide thickness on a curved surface is not uniform; the steeper the step, the greater the vertical oxide thickness. Thus, even after an extensive overetch, a wall of oxide may still remain adjacent to the metal sidewall (Maa and Hanlon, 1986).

Since grain boundaries contain a higher concentration of oxygen than do the grains, grains etch preferentially to the boundaries.

5.6.5.2.3 Anisotropic Etching

In other systems (e.g., RIE of Si), it has been shown that directional etching is a result of radiation-enhanced gas–surface chemical reactions where the radiation is energetic directional positive ions (Coburn and Winters, 1979). In the case of Al etching in a Cl- or Br-based plasma, one might postulate that the vertical etch rate is enhanced relative to the lateral rate, to achieve directionality, because the reaction product is $AlCl_x$ or $AlBr_x$ which is further reacted, sputtered, or desorbed by energetic ion bombardment. However, the beam work discussed above disproved this hypothesis, since complete reaction of Al in the halogen gas did not require ion bombardment. The dominance

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of etching by neutral species is also illustrated by the significant loading effect observed in RIE of Al in CCl_4 (Schaible et al., 1978; Lin et al., 1989; Tsukada, 1991).

It is now accepted that anisotropy is a result of sidewall passivation. Schaible and Schwartz (1979) demonstrated the existence of polymeric films on the sidewall of an Al structure etched in CCl_4/Ar using an oxide mask. Any polymer formation on the horizontal surface would be removed by the bombarding ions and is one of the reasons for the increase in etch rate with increasing RF power. Smith and Saviano (1982), in mass spectral analyses of Cl_2 plasmas containing various chlorocarbons, concluded that the C_xCl_y plasma products were responsible for sidewall passivation. In BCl_3-based plasmas, a surface-recombinant mechanism, i.e., the removal of Cl_2 at the sidewall by BCl_x, was suggested by Flamm and Donnelly (1981). This was refuted by Schwarzl and Beinvogel (1983) who proposed instead that the protective layer originated in the photoresist mask as suggested earlier by Smith and Saviano (1982).

Etch rates of Al by ion bombardment were reduced in the presence of CCl_4 and CBr_4. These molecules are chemisorbed on a clean Al surface and form a carbide-like layer. Exposure to an ion beam and CCl_4 resulted in the production of chlorinated Al species of lower oxidation states which were easily removed by ion bombardment although the carbide-like species were not. This is consistent with the protective action of the etched sidewall by C-containing species produced in the plasma (Park et al., 1985). The need for sidewall protection has led to the inclusion of polymerizing species in BCl_3/Cl_2-based etchants, such as a fluorocarbon (Iida et al., 1981; Wang et al., 1983), $CHCl_3$ (Bruce and Malafsky, 1982, 1983), and CH_4 (Lutze et al., 1990). In addition to including $CHCl_3$ in the etching gas, Dohmae et al. (1990) used a CHF_3-based encapsulating step before the final overetch step. Fujino and Oku (1992) claimed that in HBr/BCl_3/Cl_2 or HBr/BCl_3 plasmas, the sidewall film derived from the photoresist, consisting of C, Br, and Al, was a better passivant than those derived from Cl. Improved profile control was achieved in a TCP reactor when BCl_3/Cl_2 was replaced by HCl/Cl_2 (Yang et al., 1994).

After etching, the sidewall films are usually removed during resist ashing.

There are examples of inorganic sidewall protective films as well. Bollinger et al. (1984) suggested that F-based additives might protect the sidewalls by forming AlF_3 on them. According to Sato et al. (1987) lateral etching is inhibited in $SiCl_4$ RIE of Al by silicon deposition. Sidewall protection was provided by sulfur deposition when etching Al in S_2Cl_2 in an ECR reactor at 20°C; the protective film was removed by sublimation at ~100°C (Tatsumi et al., 1992). Al was etched in Cl_2/N_2 in an ECR reactor, at 60°C with an SiO_2 mask; sidewall protection was provided by a film which consisted of two layers, an outer one Al–O, Al–N, Si–O, Si–N and the inner containing Al with added Cl. The sidewall film was removed in a BCl_3 plasma (Kawamoto et al., 1994). Fu et al. (1991) claim that intrinsically anisotropic etching can be obtained using $SiCl_4$ to etch an Al alloy in MERIE reactor because of the high degree of ionization and low pressure (4 mtorr). Although the low pressure reduces gas scattering so that the etchants impinge in a more normal direction, the high degree of ionization can be useful only in clearing the surface, as discussed above. This suggests that Si species, from the gas and the oxide mask, may contribute to sidewall passivation, as postulated by Sato (1987). Although biased ECR etching in Cl_2 resulted in vertical profile and the same argument of high ion density and low pressure were invoked to explain the result (Samukawa et al., 1991), it would appear the resist mask provided the species for sidewall protection.

5.6.5.3 Practical Etchants

BCl_3 etches Al slowly. This appears to be due to limited dissociation (production of Cl) in the plasma. This view is bolstered by the relative insensitivity of the etch rate to temperature, indicating a gas-phase reaction as the rate-limiting step. CCl_4 etches Al at a faster rate but the rate is temperature sensitive (Schaible et al., 1978; Tokunaga et al., 1981), a characteristic of a surface-reaction rate

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limit. As expected, addition of Cl_2 accelerated the etch rate (Kurisaki et al., 1982; Horiike et al., 1982); the increase was faster for BCl_3 than for CCl_4 (Danner and Hess, 1986a). Using a mixture of PCl_3 and BCl_3 in a RIE system increased the etch rate over BCl_3 alone; there was no undercut or residue formation and the selectivity to SiO_2 was improved (Nakamura et al., 1981). But this mixture has not been used by others.

N_2 was said to be the key to improving the passivation of sidewalls, e.g., using BCl_3 and Cl_2 in a single-wafer RIE (Clayton and Besson, 1993) and in a HDP reactor using Cl_2 (Liao et al., 1995). CCl_4 is no longer used as an etchant because it is a carcinogen. This narrows the choices to BCl_3-, $SiCl_4$-, and BBr_3-based etchants, with Cl_2, Br_2, and HBr to increase rates, and polymer-forming gases for sidewall protection, where needed. The combination, $BCl_3 + Cl_2$ is used most frequently. The choice of passivants has become narrower, since $CHCl_3$ is a carcinogen, and the PFCs are now classified as environmental hazards.

5.6.5.4 Reactors

Although some of the early work was done in the plasma mode of reduced ion bombardment (i.e., in a symmetrical reactor), RIE has been the method of choice for many years. Magnetic enhancement of RIE and biased high-density plasma reactors, in which high rates can be obtained at lower pressures, have largely replaced the lower density systems. Low pressure decreases gas scattering and thus the tendency toward lateral attack and increases the ease of desorption of reaction products, as pointed out by Puttock et al. (1994).

5.6.5.5 Practical Etching Processes

The issues of etch rates, etch rate ratios with respect to mask and substrate, profile, and uniformity are determined by the film itself, e.g., whether Al or an alloy, composition of the alloy, deposition temperature or any heat treatment before etching, oxygen contamination (Eldridge et al., 1987), choice of reactants, their proportions, process parameters such as power, pressure, flow rate (residence time), frequency, masking material, and reactor configuration, which cannot be summarized to any useful extent. The individual papers must be consulted and analyzed. The equipment manufacturers now provide a useful start-up process which they have developed for their own reactors.

5.6.5.6 Al Alloy Etching

As mentioned earlier, Al has been alloyed with Si and with Cu and AlCu is used in a stack with Ti and TiN in which some of the Al and Ti may have interacted, forming $AlTi_3$, depending on the deposition temperature.

Al/Si alloys might be expected to behave like pure Al since Si routinely etched in a RIE system in chlorinated plasmas. Maa and O'Neill (1983), however, found that, in RIE of Al/Si films in $CCl_4/N_2/BCl_3$, the etch rate of Si was much less than that of Al, perhaps due to inadequate substrate bias: Si requires ion bombardment in order to etch in a Cl-based plasma whereas Al does not. If the Si is oxidized by residual gases it will etch slowly.

Cu, on the other hand, is expected to pose a problem since the vapor pressures of the copper halides are low. This is covered in the next section.

Ti, TiAl intermetallics, and TiN are readily etched in the plasmas used for Al. A problem arises when etching the Ti compounds beneath the AlCu because this is equivalent to an appreciable overetch of the AlCu with an attendant undercut. Reducing the Cl_2 content and increasing the passivating gas (e.g., $CHCl_3$) solves this problem (Dang, 1994).

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5.6.5.6.1 Cu-Containing Residues

As indicated above, the Cu-content of Al alloys complicates etching because Cu-rich residues may be left on the surface after etching. As discussed previously, Cu often concentrates at the metal/oxide interface during deposition, increasing the difficulty of etching. An underlay of Al inhibits the pile-up of Cu, making residue-free etching easier. The residues may be either non-volatile reaction product or unreacted large $CuAl_2$ (θ-phase) precipitates that had formed within the film (Abraham, 1987; Hu et al., 1989; Suzuki et al., 1992); these act as micromasks, forming conical residues.

In the early days of RIE of Al–Cu alloys, residues were sputter etched in an inert plasma. Departing from the use of simple sputter etching, two opposing procedures were used to eliminate the θ-phase particles at the conclusion of RIE. Hu et al. (1989) finished the etch process by lowering the pressure in the reactor, thereby increasing the ion bombardment and, in effect, sputter etching the particles in the reaction mixture. On the other hand, Suzuki et al. (1992) added a step in which there was significant lateral etching; the residues presumably were undercut and thus etched away.

Elevating the wafer temperature by using a heat-conducting medium between the heated substrate holder and the wafer or enhanced ion bombardment to increase sputtering and heat the wafer, prevent the formation of a Cu-rich residue. Heating the substrate holder without thermal bonding between it and the wafer may be of benefit simply because the gas surrounding the wafer is hotter so that the reaction product may be pumped away before it redeposits on the wafer. By keeping the substrate at 100°C, residue-free etching was accomplished in biased ECR etching in Cl_2 (Samukawa et al., 1991). However, raising the wafer temperature restricts the choice of masking materials and increasing the sputtering component degrades selectivity to both mask and substrate.

Tsukada (1991) reported that magnetron etching was very useful in removing residues. Yet, in $BCl_3/Cl_2/N_2/CF_4$ in a MERIE reactor, residue was observed. There was less residue at high RF powers, slower etch rates (i.e., lower Cl_2 concentration) and high cathode temperatures. There was more residue in the dense areas than in the open ones. Residue formation was minimal at very low pressures, and relatively sparse at very high pressures; residue was densest at intermediate pressures (Mak et al., 1992).

Sparse residues resulted after RIE in a single wafer etcher in HBr/BCl_3 or $HBr/BCl_3/Cl_2$ (Fujino et al., 1992).

Residue-free etching has been reported by a number of workers: RIE in $SiCl_4$ (Sato et al., 1987), ECR using Cl_2 (Samukawa et al., 1991), BCl_3/Cl_2 (Samukawa et al., 1991b; Bradley et al., 1991), $BCl_3/Cl_2/N_2$ (Marx et al., 1992). Interposing BCl_3 "sputter etch" cycles at several points during RIE in BCl_3/Cl_2 in a MERIE reactor resulted in residue-free etching at 45°C and 8 Pa (Hattori et al., 1994).

A patent by Webb (1994) disclosed a low-temperature (low-pressure, high-power) process for RIE of AlCu alloys with a Cu content $>0.5\%$ Cu. The process was carried out in a single wafer magnetically enhanced capacitively coupled reactor. Elimination of the etch residue depended on controlling the N_2 content of a BCl_3/Cl_2-based etchant mixture; the higher the Cu-content, the lower the N_2-concentration. However, higher Cu-content alloys required higher temperatures, e.g., for a 2% alloy, the temperature was ~100°C, but whether the temperature referred to that of the wafer or the wafer holder was not specified.

Reacting $AlCl_3$, produced in the chamber in large quantities from a source of Al external to the wafer, with the copper chloride as it was formed on the surface of the film during RIE, prevented the formation of residue by volatilizing Cu during etching. The volatile compound is a copper–aluminum chloride complex (Bausmith et al., 1990). This process was also used by Narasimhan et al. (1992) in a MERIE reactor and Sato (1994) in a static magnetron triode RIE system (SMTRIE).

Addition of N_2 to a BCl_3/Cl_2/mixture in an ECR reactor suppressed residues (and postetch corrosion), but in a MERIE reactor addition promoted residue formation (and corrosion). It was postulated that BCl_x^+ ($x = 0$ to 3) in the plasma produced the benefit by enhancing an ion-assisted

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reaction and/or by physical sputtering; these species were elevated in the ECR and suppressed in the MERIE reactor (Kusumi et al., 1995).

It can be seen that many methods have been proposed for removing or preventing the formation of Cu-rich residues; there are some conflicting reports as to the success of the methods. In order to have a successful process, no residue may remain on the surface at the end of the process. For each user/reactor/etchant system, some method has been evolved which produces a satisfactory product although the experience of others may lead them to disagree with the theory or practice.

It is also possible to remove the residues, post-RIE, by rinsing the wafer in HNO_3, (Herndon and Burke, 1977; Nakamura et al., 1981). This treatment also helps passivate the surface, but is rarely done now.

5.6.5.7 Loading and Feature Size-Dependent Etching

The bulls-eye etch pattern, discussed in Chapter 1, is one of the problems characteristic of etching Al and its alloys. A pattern-sensitive clearing effect is seen even when etching pure Al films; it is, perhaps, exaggerated by the formation of Cu-rich residue during AlCu RIE. Overetching to clear the residual metal in narrow spaces may result in drastic overetch of large features and may produce substrate damage. The definition of the various terms used to describe the phenomenon, the distinctions among the terms, and the basic mechanisms proposed are covered in Chapter 1. In many of the reports on etching Al or its alloys, the terms were used somewhat loosely if the guidelines relating to definitions and measurement techniques stated by Gottscho et al. (1992) are taken as definitive. For example, the term ARDE has been used when only a single thickness of metal and mask were etched (space width was translated into aspect ratio) and the etch rate dependence on etch time (for various size spaces) was not measured.

In the case of Al alloy etching, an inhibitor (identified in some cases as redeposited sputtered mask fragments) has been identified as the cause of slow etching in narrow spaces.

In one instance of etching an Al alloy film in $Cl_2/BCl_3/N_2$ in a MERIE reactor, by controlling the process so that it was in a transport rate-limited regime, the etch rate difference between tight spaces and open areas could be reversed by changing the BCl_3/N_2 flow rate ratio. The normal lag was observed at a high flow rate ratio. In this case, there was a large sputtering component which was attributed to the BCl_3; a large amount of sputtered material was available to deposit in small spaces. At the same time there was a good supply of reactants to the open areas in which redeposition was minimal. By reducing the flow rate ratio, the sputtering component was decreased so that there was less deposition in the small spaces to inhibit etching. At the same time the residence time was increased, reactant supply to the large areas was reduced. Thus the lag was reversed. Other factors that reduced the normal lag were increasing magnetic field strength, increasing pressure, and decreasing the Cl_2 flow rate. Thus there should be some optimal conditions at which loading is minimized, or perhaps eliminated entirely (Huang and Siegel, 1994).

Webb et al. (1996) examined ARDE in a high-density, high etch-rate reactor, the decoupled plasma source (DPS) metal etch system. They also found that high etchant concentration enhanced the etch rate in open areas and deposition of resist byproducts reduced the etch rate in dense areas. The optimized process conditions (e.g., source power, choice of etchants, and etchant ratios) which balance etch and deposition can minimize microloading at both high and low pressures. They also reported that the breakthrough step played a major role in microloading and could cause poor performance despite good microloading in the main etch.

In an ECR reactor, RIE lag was shown to depend on the substrate RF bias and the mask material, i.e., etching in small spaces was inhibited by the deposition of sputtered mask fragments. The amount of material deposited depended on the distance from the mask, so that narrow spaces receive more of this material. There was less lag when SiO_2 was used as a mask. The angular distribution of ions impinging on the etching surface had no effect. The concept of a limited flow

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of neutral species into the narrow spaces appeared to be valid only in the case of etching with an SiO_2 mask or etching with a resist mask with zero applied bias. Thus the proposal for reducing RIE lag: lower the RF bias and use an inorganic mask. However, profile control will be exceedingly difficult (Sato et al., 1995). Xie and Kava (1996) and Xie et al. (1996) reported that RDE in metal etching was more severe in high-density plasmas operating at low pressures. They found that ARDE in a MERIE reactor was controlled by the effective ion to neutral flux ratio and the ion to inhibitor flux ratio. A high ion to inhibitor ratio resulted in a higher etch rate but greater RIE lag; a lower one reduced both the etch rate and lag. At the lowest ratio, reverse lag and a low etch rate may result. They concluded that absolute AR-independent etching may not be realized but may be minimized while keeping a high etch rate. The nature of the inhibitor was not identified.

A simulation program was developed (Aoki and Sasamura, 1996) in which the flux rates (gas particles, ions, and sputtered mask fragments) are calculated as a function of trench AR and then the etch rate is calculated with these flux rates at each AR. The surface reaction parameters are determined by fitting the calculated results to the experimental etch rates. It was confirmed that microloading was affected by the sputtered resist fragments. It was concluded that there might be less microloading in a RIE system, where the resist sputtering rates are lower, than in the high-density plasma systems.

Microloading was reduced significantly when HCl/Cl_2 was used instead of BCl_3/Cl_2 in a TCP system. The improvements were said to be due to the change from a more chemical process to a more physical one. The importance of polymer deposition in RIE lag was again emphasized. They had some preliminary results that indicated that replacing photoresist with a carbon mask reduced microloading effects (Yang et al., 1994). Microloading was eliminated, for features with a 0.4 mm space and AR > 4, by using a N_2/Cl_2 plasma in an independently biased high-density reactor. The role of N_2 was to enhance sidewall passivation and raise the etch rate by increasing the Cl radical concentration. (Liao et al., 1995). Gabriel et al. (1997) reported that, in an ICP reactor, addition of $CHF_3 + Ar$ to a BCl_3Cl_2 mixture could reduce the lag in narrow spaces significantly. They proposed that the improvement was due to the presence of sidewall passivants, e.g., CHF_3 which reduced the sticking coefficient of Cl on Al, increasing the reactant flux to the bottom of high-AR spaces. Abdollahi-Alibeik et al. (2001) confirmed this conclusion using a combination of experiment and the Stanford etching and deposition profile simulator SPEEDIE. They added another condition: the inhibitor (passivant) does not recombine with the etchant to form a volatile product.

5.6.5.8 Profile Control

Prevention of undercutting, i.e., producing features with vertical walls and replicating the dimensions printed in the mask, has been the aim of most processes, as discussed above under anisotropic etching. This has involved, for the most part, controlling the concentration of Cl_2 and ensuring adequate sidewall passivation.

Some processes designed to produce positive sidewall tapering (as opposed to undercut) have been developed in order to improve the step coverage by an overlying insulator. The earliest attempts depended on resist erosion: Booth and Heslop (1980) using resist tapered by baking, and Nakamura (1981) using a CCl_4/H_2 mixture, in which the resist and Al were etched at almost equal rates. They were unsuccessful; control of the resist profile and etch nonuniformity were cited as reasons. A later attempt at using the same principle of controlled resist erosion was more successful. Abraham (1986) used a hexode reactor with BCl_3-based etchants and an etch process based on high DC bias/pressure ratios. The faceting of the resist angle in this case resulted in the tapering of independent of feature size.

Another approach has been balancing deposition and etching of a polymeric film on the sidewall. In one instance, the taper angle was determined by the ratio of $CHCl_3$ to Cl_2 in the etch mixture using a MERIE system (Arikado et al., 1986). A similar process used $CHF_3/Cl_2/BCl_3$ in a

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hexode reactor; the taper angle was determined by the CHF_3 and Cl_2 flow rates, bias, and resist thickness. By a suitable choice of parameters, angles ranging from 60° to 90° could be obtained (Selamoglu et al., 1991). However, the taper angle decreased with increasing spacing of the aluminum lines.

A process resulting in tapered sidewalls was based on sidewall passivation due to resist consumption rather than resist erosion. It was carried out in a biased TCP reactor using $BCl_3/Cl_2/N_2$ and the inclusion of N_2 was the key to forming sloped profiles. Substrate bias, TCP power, and gas flows were determining factors. The dimension of the top of the line was the same as that of the initial mask dimension. In this process, also, the slope angles depended on the space between the lines, decreasing with increasing spacing with the maximum slope for isolated lines. The deposited polymer was readily removed when the resist was removed (Allen and Rickard, 1994).

5.6.5.9 Corrosion Control

Prevention and control of post-RIE corrosion of Al and its alloys has presented a major challenge. The presence of Cu in the film and in the residue (if formed) enhances the susceptibility to corrosion because of the galvanic action of dissimilar metals and because the involatility of the CuCl leaves a higher concentration of Cl on the etched surfaces. The higher the content of Cu in the AlCu film, the greater the corrosion susceptibility (Lee et al., 1981; Rotel et al., 1991). The surface oxide, which plays a role in corrosion protection, is thought to contain discontinuities in the case of AlCu films (Zahavi et al., 1984).

The reaction product $AlCl_3$ hydrolyzes in moist air forming HCl. The HCl is a source of Cl^- which destroys the passivating native oxide, reacts with Al to form a soluble compound which hydrolyzes in moist air, forming HCl, which, in turn reacts further. It is the regeneration of HCl that is responsible for the massive corrosion even when the surface concentration is relatively low. Cl has been found to be bonded both to the metal lines and to the C in the sidewall layer as well as the resist. The corrosion product observed on the metal surface or extruding from the sidewalls is hydrated aluminum oxide or aluminum hydroxide. Corrosion results in increased resistance of metal lines and may even cause cracking of the overlying dielectric films (Wada et al., 1987). The use of caps or underlayers of other metals (e.g., Ti, TiW) increase the susceptibility to corrosion (Maa et al., 1990).

Prompt plasma stripping of a resist mask is thought to be helpful in inhibiting post-RIE corrosion, although there is some disagreement as to when this should be done in the post-RIE process cycle, due to the possible acceleration of corrosion by heating the wafer in the presence of Cl. A wide variety of passivation treatments have been proposed, but there is disagreement about the effectiveness of each; the results published in one paper may be contradicted in another. A sample of the proposed post-RIE treatments are (1) low-temperature thermal oxidation of the surface (Lee et al., 1981), (2) rinsing in deionized water immediately or keeping the wafers in an inert ambient (e.g., dry N_2) if rinsing must be postponed, (3) rinsing in phosphochromic acid solution (Eldridge et al., 1983), (4) post-RIE exposure to a F-containing plasma, e.g., CHF_3 (Tsukada et al., 1983), CF_4, $CF_4 + O_2$, substituting F for the Cl on the walls while depositing a passivating polymer film; Fok (1980) suggested following the plasma exposure step, with rinsing in fuming HNO_3 to remove the fluoride and oxidize the surface and Iida et al. (1982) by using an NH_3-containing plasma and water rinse, (5) microwave downstream resist strip in O_2/NH_3 (Hwang and Mak, 1992), (6) rinsing in an aqueous alkaline solution and then in water (Iida et al., 1981), and (7) a combination of heat treatment and an organic solvent rinse (Samukawa et al., 1989). Evaluation of corrosion has usually been by visual inspection. However, Brusic et al. (1991, 1993) carried out electrochemical measurements and concluded, on the basis of those experiments, that the most effective post-RIE treatment (of AlCu) was an immediate water rinse, followed by resist strip, immersion in phosphochromic acid, then rinsing and drying. CF_4/O_2 treatment prior to the water rinse had a slight but

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negative influence of corrosion resistance. Brusic and Yang (1996) compared the corrosion susceptibility of AlCu films etched in a RIE system using HCl/Cl_2 and BCl_3/Cl_2 as etchants. They again used electrochemical methods and examined the wafers minutes after being removed from the etcher, which included an ashing station. The wafers exposed to HCl/Cl_2 dissolved more slowly at all potentials. This was explained by the nature of the polymeric films; HCl-treated wafers were more wettable, more cleanable in a O_2 plasma and thus more readily formed a passivating oxide. Immediate water rinsing and phosphochromic acid etching were again found to be very effective in further reduction of the corrosion rate. Wafers etched in BCl_3/Cl_2 were more sensitive to any delays before water rinsing. Addition of N_2 and an extended anneal before resist stripping had a beneficial but small effect. Here, too, the effects of CF_4 on AlCu corrosion were well pronounced and negative. These two electrochemical studies appear at variance with many other studies, in which visual inspection was the criterion, in rejecting the benefits of F-containing plasma treatment.

By reducing the substrate temperature during etching in Cl_2 in an ECR reactor, corrosion of AlSiCu was reduced (Aoki et al., 1991). It was found that after water rinsing, the Cl concentration was much smaller on wafers etched at –60°C than on wafers etched at +30°C. It was postulated that the smaller number of Al–Cl bonds left on the surface was due to reduced chemical reaction and diffusion rates at the lower temperature. Adding N_2 to the BCl_3/Cl_2 etch mixture in an ECR reactor also reduced post-RIE corrosion (Kusumi et al., 1995). Corrosion across a wafer was not uniform but was related to the pattern density Corrosion was heaviest and the concentration of Cl highest in regions of intermediate spacing. They proposed that there was a limit to the supply of the product $AlCl_3$ in narrow spaces and a depletion of reactant Cl in wide spaces, i.e., a microloading effect (Gabriel and Wallach, 1992). Levy (1992) patented a process for etching Al without forming corrosive Cl-containing residues by using a mixture of one or more Br-containing compounds and SF_6. Gebara et al. (1994) pointed out that different types of photoresist absorb Cl differently, so that the choice of resist also has an influence on corrosion.

Polymer buildup in a RIE system when $CHCl_3$ was added to the reaction mixture for better sidewall protection was the cause of increased corrosion susceptibility. The sidewall polymer was contaminated with Cl, either by reaction or absorption. The polymer eventually deposited on the wafers, masking the metal, leaving cluster defects. In addition, it was difficult to remove the deposited polymer which then reacted with moisture and corroded the metal. Reducing the $CHCl_3$, and increasing the Cl_2 concentration, raising the chamber pressure and lowering the pressure, reduced the buildup of polymer (Dang, 1996).

Corrosion pits (voids), in the absence of visible corrosion product, have been observed on the sidewalls of the etched features after RIE in both a batch (hexode) and a single-wafer etcher (Daubenspeck and Lee, 1992) and in a TCP reactor (Hill, 1996). Daubenspeck and Lee (1992) stated that the reaction was thermally driven and did not require the presence of moisture. The voids were most numerous at the interface between AlCuSi films and Ti or TiN layers, but existed in the bulk of the film as well. Void formation appears to be due a reaction of the Cl-containing etchants or residues on the sidewalls with the alloy at imperfections in the sidewall passivation either during etching or the stripping process. Daubenspeck and Lee (1992) opt for their occurrence during the stripping operation. Thus to eliminate the voids, the wafers must be heated gradually to remove the residual Cl-contaminant and to reduce the probability of a thermally driven reaction, before the resist is stripped. Hill explained that void formation was a case of galvanic corrosion in the neighborhood of θ particles at grain boundaries; the corrosion was caused by rinsing in hot deionized water after stripping the resist. Using room temperature water eliminated the problem. Baek et al. (1998) reported that post-RIE exposure to an SF_6 plasma inhibited corrosion of AlCu films. Although the Cl atoms incorporated during etching were not replaced by F atoms, the SF_6 formed a passivation layer which prevented moisture penetration.

Thus, it is evident that there are many different and sometimes contradictory recipes for corrosion inhibition. Each laboratory or fabrication line most probably has a favorite post-RIE treatment, which satisfies the product requirements.

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No mention of corrosion was made in the paper in which HBr was the sole etchant (Aoki et al., 1992). There is essentially nothing in the literature to indicate what might be expected (e.g., is there regeneration of Br^- in a hydrolysis reaction?) apart from the fact that HBr, like HCl, corrodes Al.

5.6.5.10 Masking

Both inorganic and organic masks are used in RIE of Al and its alloys. In addition to the usual concerns about the etch rate of a mask, and in the case of an organic masks, its thermal stability, is the chemical interaction of the etch product ($AlCl_3$) with photoresist. The result is excessive global degradation and localized pitting (Spencer, 1983, 1984). This has been explained by the fact that $AlCl_3$ is a Lewis acid which reacts readily with organic materials (Hess, 1982). Another problem is incorporation of $AlCl_3$ into the resist mask; during resist ashing the chloride is converted to the oxide which remains on the surface.

Thus an additional step, such as immersion in phosphochromic acid or a mild alkaline solution, is required. Resist stabilization in a plasma or by UV exposure and hard-bake before RIE was reported to minimize or eliminate the problem (ter Beek, 1985).

The use of a trilevel resist has several advantages; the lithographic resolution is independent of its thickness; loss of masking due to an inadequate etch rate ratio is no longer an issue. In addition, the walls of the mask are vertical and not distorted by heat. However, during RIE transfer of the pattern in a O_2 plasma into the thick underlay, the Al surface beneath the mask is sputtered and a thick layer of oxidized Al is deposited on the walls of the mask, changing its dimensions and interfering with mask removal (Kinsbron et al., 1982a). There is another residue which is deposited from the hard mask during RIE in O_2; it looks like stalks of grass in the SEM and has, therefore, been named "RIE grass." Both kinds of residue can be removed, before etching, without attack of the Al by immersion in a mixture of ethylene glycol and buffered HF (Kinsbron et al., 1982b). However, this puts an additional burden on the adhesion of the mask to the substrate, and when the lines are very narrow, the mask may not survive.

5.6.5.11 Temperature Effects

Elevated wafer-holder temperatures had been reported to be necessary for etching Al–Cu films without leaving residues (Schaible et al., 1978) but this was disputed, for example, by Chambers (1982) who used a low-frequency (380 kHz) plasma for etching. Subsequently, it was realized that merely using a heated wafer holder in a low-pressure reactor does not heat the wafer (Schwartz and Schaible, 1981) but probably prevents redeposition. However, the low-frequency ion bombardment, more energetic than 13.56 MHz bombardment, probably did heat the wafer to assist in volatilization of CuCl and sputtering would also be more efficient.

The differences between the temperature sensitivity of CCl_4 and BCl_3 etching was discussed earlier.

High wafer temperatures are usually avoided, where possible, to prevent enhancement of the thermally driven isotropic reaction and to prevent thermal distortion of the resist mask, i.e., flowing and reticulation. When necessary, resists can be stabilized to withstand elevated temperature by either plasma (Ma, 1980) or UV (Haroka and Pacansky, 1981) hardening, followed by a hard-bake.

Cooling the wafer during RIE in a $BCl_3/SiCl_4/Cl_2$ plasma suppressed undercutting; the resulting taper of the profile could be adjusted by changing the temperature (using He between the wafer and the holder for temperature control) (Nakamura et al., 1987).

Thin AlCuSi films were etched in Cl_2 in a biased ECR reactor at low temperatures (down to −50°C). Only relative etch rates were given; there were none for the metal itself. SiO_2 was a better mask than resist; the selectivity to SiO_2 was higher and improved as the temperature was reduced. The decrease in etch rate as the spacing decreased (microloading) was smaller as the temperature

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was reduced from +40 to –50°C. This was explained by postulating that a low vapor pressure precursor was formed on the surface, its thickness independent of the supply of Cl (which is larger in the wider spaces) and its removal dependent on ion bombardment which is also independent of spacing. There was less dependence on line spacing if an SiO_2 mask was used instead of resist and more dependence when HBr was substituted for Cl_2. The change in line dimension, compared with the dimensions of the SiO_2 mask (critical dimension shift) could be controlled by adjusting the temperature. In Cl_2, the line width was decreased at higher temperatures due to lateral etching. At all temperatures there was a positive shift when HBr was used; for Cl_2, zero shift was obtained at –30°C. There was no mention of any residues (Aoki et al., 1992).

The etch rate (in Cl_2, in a biased ECR rector) was constant as the wafer temperature was reduced from +50 to about –10°C; below this temperature the etch rate increased rapidly with decreasing temperature; the rate appears to saturate, at almost double the high-temperature rate, at about –50°C. The explanation for this phenomenon was based on the model of Bermudez and Glass (1989) which postulated that there are two kinds of adsorption sites for Cl on Al, namely surface and subsurface sites. Physical adsorption occurs at the surface sites, but the chlorine evaporates before reacting. Chemical reaction occurs at subsurface sites and the product is desorbed thermally. Thermal desorption decreases as the temperature is decreased, but desorption may be induced by ion bombardment. In addition, there is increased adsorption at surface sites; a cluster model was proposed, i.e., at low temperatures, there are attractive interactions between chlorine molecules on the surface (cluster formation) which decreases the probability of evaporation. Under the influence of ion bombardment two events occur at the surface sites chemical reaction and desorption. The conclusion is that the increase in etch rate at low temperature is due chiefly to the processes at the surface sites (Uchida et al., 1993).

5.6.5.12 Extendibility of RIE

RIE of Al alloys is an established manufacturing process. To what dimensions is it extendable? Ning et al. (1999) claimed that reliable 0.15 μm, high-AR line/space wiring patterns can be manufactured with good yield using RIE of a Ti/TiN/A/Ti/TiN stack in Cl_2/BCl_3. A PVD W cap hard mask appeared to be the most suitable, although it added complexity to the process. Oxide gap-filling process limitations restrict the AR to ≤ 3. If the gap-filling capability of some of the low-ε dielectric films is greater, the extension of RIE to the smaller dimensions could be worthwhile, but removing any overfill (e.g., by CMP) presents a new problem (see Chapter 6). Hansen (2000), however, argued that below 0.25 μm, RIE is not the method of choice, due to incomplete removal, leaving "stringers" causing shorting between adjacent lines and to poor uniformity, and that the damascene process, despite its problems, must be pursued. The case for changing from RIE to dual damascene processing was also made by Schnabel et al. (2000). They cited as reasons for abandoning RIE: poor etch selectivity to masks, difficulty in filling gaps with insulators, and corrosion. Discussion of the advantages and problems associated with this newer technology is found in Chapter 6.

It should be noted, however, that in real products, AlCu is used for 0.18 μm line/space wiring patterns, sometimes for 0.15 μm dimensions, and migrating to Cu at 0.13 μm.

5.7 PATTERNING OF COPPER

5.7.1 Introduction

Wet etchants for Cu have been compiled by Kern and Deckert (1978). They have not been seen as suitable for defining the small dimensions now required for VLSI and ULSI devices. However,

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a new wet etchant for Cu, used to define interconnection test patterns, was reported by Takewaki et al. (1995). It was a mixture of H_2O_2 (to oxidize the Cu), acetic acid (to etch the CuO), and H_2O.

Sputter etching and ion milling are viable techniques but are not now used extensively for patterning. Since it is essential that Cu migration into the surrounding dielectrics be prevented, after Cu is etched, it must be encapsulated in an appropriate barrier layer, increasing complexity of processing.

5.7.2 Reactive Ion Etching of Copper

Many processes have been developed for RIE of Cu in Cl-containing plasmas in many types of reactors; most required high wafer temperature ($\geq 225°C$) but in some, lower temperatures (as low as room temperature) produced acceptable results. CCl_4/Ar (Schwartz and Schaible, 1983), $SiCl_4$ with various additives (e.g., Howard and Steinbruchel, 1991, 1994; Igarashi et al., 1994, 1995; Ohno et al., 1996), as well as Cl_2, with and without irradiation, have resulted in anisotropic profiles (Miyazaki et al., 1996; Lee et al., 1998; Choi and Han, 1998). Br_2 but not I_2 was used successfully (Rogers et al., 1992).

As mentioned in the introduction, an encapsulating barrier layer is needed to prevent migration into the ILD. This complicates the processing; after the Cu features are etched and coated with the barrier metal, the extra steps of masking and removing the barrier from dielectric layer must be carried out. To avoid these extra steps, Markert et al. (2000) proposed using air gaps in place of a dielectric film to avoid the need for a barrier layer on the sidewalls of the Cu feature Thus a single step of RIE of the metal stack of barrier/Cu/barrier would be sufficient.

Thus, although anisotropic RIE of Cu has been demonstrated, currently the embedded (inlaid, damascene) process for Cu and a barrier layer has been chosen by the chip fabrication industry for both the horizontal and vertical interconnections. The damascene as well as earlier additive processes are discussed in Chapter 6.

5.7.3 Additive Processes

5.7.3.1 Introduction

The formation of encapsulated Cu interconnections by an additive process is more feasible than by a subtractive one, although RIE of the low-ε dielectrics may require substantial modification of the RIE processes usually used for SiO_2. In addition, the requirement of a barrier layer is easier to implement.

5.7.3.2 Lift-Off

Rogers et al. (1991) described the use of lift-off for forming Cr-encapsulated Cu interconnects. The evaporated metals were a Cr base, then Cu, and then a capping layer of Cr. The stencil was a soluble polyimide. The metals were clad in PECVD SiON before the permanent polyimide dielectric layer was spun-on. The via plugs were Ti/AlCu/Ti, also formed by lift-off. Cho et al. (1991) illustrated a similar process using CVD W encapsulation of Cu, by depositing selectively on a W seed layer.

5.7.3.3 Embedment

In this technique, the metal is deposited into patterns formed in the permanent dielectric, usually by CVD (Section 5.4.3) or by electrochemical plating (Section 5.4.4.4) although Lakshminarayanan et al. (1994) sputtered Cu into Ti-lined trenches etched into the PECVD oxide.

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These additive processes may be combined with blanket removal by CMP, sputter etching, or ion milling in the case of nonselective deposition or overfill with a selective process. Embedment is discussed more fully in Chapter 6.

5.7.4 Dry Etching

Hampden-Smith and Kodas (1993) have reviewed chemical approaches to dry etching of Cu, but with the possible exception of laser-assisted etching which may have the potential for anisotropy, the methods are useful for blanket removal, not patterning. These include the reversal of the CVD deposition reaction (reverse CVD), oxidation, and the formation of volatile copper(I) halide Lewis base adducts.

5.8 PATTERNING OF TUNGSTEN

5.8.1 Wet Etching

There are suitable liquid etchants for W (e.g., Kern and Deckert, 1978) but dry etching, in F-, C-, and Br-containing plasmas, is now preferred.

5.8.2 Lift-Off

The high substrate temperatures required for evaporation of low-resistivity W are not compatible with the organic stencils usually used in these processes.

5.8.3 Reactive Ion Etching

When W is deposited into holes, the excess must be removed, usually using a sacrificial organic overcoat, as discussed in Chapter 6. When etched to form patterns, for gate electrodes or interconnections, dimensional control, i.e., anisotropy, is essential. Etch rate ratios, to both the mask and substrate, are also important factors when choosing a patterning process.

W is etched spontaneously by F only very slowly at room temperature but the rate is enhanced significantly when the surface is bombarded with Ar ions. WF_6 is the only product (Winters, 1985). Mechanisms to explain the ion enhancement of the W + F reaction are (1) chemical sputtering (Winters) and (2) lattice damage-induced chemical reactions (Greene et al., 1988b).

WF_6 is less volatile than the oxychloride; therefore O_2 is often added to Cl-based plasmas. Cl_2/O_2 mixtures etched W and a conductive underlayer (e.g., TiN) anisotropically and selectively to an oxide underlay and photoresist mask (Cote et al., 1988). However, W could be etched in a Cl_2 discharge with the addition of a small amount of BCl_3 (Fischl and Hess, 1987). In the absence of ion bombardment, W could be etched by Cl atoms, but not Cl_2 molecules (Fischl et al., 1988).

Anisotropy and selectivity to underlying insulators are inadequate in CF4 and SF_6 plasmas. Addition of CH_3 to SF_6 eliminated undercut (Chen et al., 1987). Low-temperature (– 10 to – 50°C) etching in a triode reactor using SF_6 was anisotropic and exhibited a reasonably good selectivity to resist. However, when the W film was deposited over a TiN or Ti glue layer, residues were formed. The mechanism proposed for residue formation was formation of nonvolatile but water-soluble TiF_xO_y, which covered the entire surface or acted as micromasks during W etching, resulting in spikes of unetched W. Following the main etch by RIE in SF_6 at +55°C in a diode and finally in Cl_2 at 5°C resulted in clean surfaces (Sridharan et al., 1992).

$CBrF_3/O_2/He$ was found to be more suitable, possibly because a more substantial polymer deposit protects the W sidewalls. The selectivity to both oxide and resist were acceptable (Burba et al., 1986).

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Another suitable etchant is $CF_2Cl_2 + CHF_3/O_2$ (Daubenspeck et al., 1989; Daubenspeck and Sukanek, 1990). In a low-pressure batch reactor, etch rate and anisotropy depended on the energy of ion bombardment and reactor loading, as well as on power, pressure, and gas composition. In single-wafer reactors, in which pressure and power density are higher, multistep processing was required to balance etching and deposition of polymer (Daubenspeck and Sukanek, 1990).

Addition of C_4F_8 to SF_6 in an ECR reactor eliminated the undercut, through sidewall protection; it also decreased RIE lag with the decrease greater as for higher C_4F_8 concentrations. At AR = 2.5, the normalized etch depth was increased from 0.72 in the absence of C_4F_8 to 0.82 with $C_4H_8/SF_6 \sim 0.4$. No change in RIE lag with RF power was observed up to 60 W. Application of RF bias increased the etch rate of W but degraded the selectivity to resist significantly. However, anisotropy was achievable in the absence of RF bias and thus unbiased etching was the process of choice (Maruyama et al., 1995).

5.9 STRUCTURE OF METAL FILMS

5.9.1 Hillocks

"Hillocks" is the name given to protrusions on the surface of metal films; they can be formed during deposition but those studied most intensively are a result of postdeposition heat treatments. They can create problems both in processing (interlevel shorts) and in reliability (breakdown during use). It may be necessary to increase the thickness of a dielectric overcoat to insure adequate coverage to prevent these failures. CVD dielectrics conform to the hillocks but sputtered insulators probably afford less protection. Resist may be thinned when applied over hillocks and thus erode prematurely during RIE.

Hillock formation during deposition depends on the deposition rate and the substrate temperature. When the temperature was increased, at a constant deposition rate, the density of the hillocks decreased but their average size increased. As the deposition rate was increased, the hillock density and average sizes decreased. In general, hillocks formed when films were deposited at low temperatures and low rates (Chang and Vook, 1991).

During postdeposition heat treatments, many hillocks are formed on small-grained films; as the grain size is increased, both the number and size decrease (Philofsky et al., 1971). Hillocks formed during heat treatment after deposition may grow to substantial heights (e.g., >2 μm) although whiskers have also been observed. The thickest films had the highest density of hillocks and the biggest ones (Ericson et al., 1991). Some observers reported that hillocks had a well-defined, crystalline appearance. Several classes of hillock were characterized by Santoro (1969); the type depended on the grain structure from which they arose. Edge hillocks grew along grain boundary segments, flat-topped structures arose from small grains, and spire-like ones originated in triple points. Ericson et al. (1991), however, found that annealing hillocks were usually softly rounded, with the well-defined ones arising in very thin films. Hillocks formed on AlCu films were Cu-rich (Philofsky et al., 1971). The hillock density decreased but the size increased as a function of time during isothermal annealing (Chang and Vook, 1989). Ericson et al. (1991) found that initially hillocks are separated from the film by a grain boundary-like interface along the original film surface, but during prolonged annealing, grain growth of adjacent grains eventually result in integration of the hillock in the film.

One mechanism proposed for hillock formation is stress relief (Paddock and Black, 1968). A high compressive stress is induced, during thermal cycling, due to the thermal mismatch between Al (which has a high coefficient of thermal expansion, CTE) and the substrates (e.g., Si, SiO_2) which have significantly lower coefficients. The low yield strength of Al causes the film to yield. Transport along grain boundaries and possibly along the surface and interface provides the material for hillock

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growth. To supply material for hillock growth, the film will be thinned elsewhere. The mechanism for surface reconstruction, the mass transport phenomenon responsible for hillock growth, was said to be compression fatigue, and methods of hillock suppression are those that increase fatigue resistance (Philofsky et al., 1971). An alternative mechanism is a creep phenomenon, a lattice diffusion process; the surface is deformed due to atomic motion in the bulk (Santoro, 1969).

Suppression of hillock growth has often been accomplished in two general ways: by overcoating the films before heat treatment and by doping the Al. Among the specific suggestions are: (1) coating with Al_2O_3, grown by anodization (Dell'Oca and Learn, 1971), grown in hot water after immersion of the Al in fuming nitric acid (McMillan and Shipley, 1976), or after sputter etching the Al surface (Harada et al., 1986); (2) periodically introducing O_2 during Al deposition, i.e., Al/AlO layering (Faith, 1981) or using an Al/Al_2O_3 alloy (Bhatt, 1971); (3) addition of alloying elements, Si (Paddock and Black, 1968), Cu (Learn, 1974), Ti *and* Si (Gardner et al., 1984), Sn (Sato et al., 1971); and (4) overcoating, e.g., with N-doped TiW (Lim, 1982), TiW (Townsend and Vander Plas, 1985; Mak, 1986), TiN (Rocke and Schneegans, 1988), sputtered SiO_2 deposited at low power, i.e., low temperature (Barson and Schwartz, 1970), low-temperature CVD (Learn, 1986), refractory metals or silicides (Ho et al., 1987). Alternating layers of Al and $TaSi_x$ remained hillock-free after annealing (Draper et al., 1985). Ar^+ ion implantation, an effect not related to damage (Holland and Alvis, 1987), and interposing a layer of WSi_2 between the Al film and the underlying SiO_2 were also reported to be effective in hillock elimination (Cadien and Losee, 1984).

The similarity between thermally induced hillock formation and electromigration failures is emphasized by the similarity of some of the measures used to minimize both effects (Berenbaum, 1972).

5.9.2 Microstructure of Metal Films

5.9.2.1 Evaporated Films

The microstructure of films deposited by vacuum processes is particularly sensitive to the substrate temperature (T) and the melting point of the material (T_m). The basic model is the structure zone model of Movchan and Demchishin (1969), shown in Figure 5.14.

Below T_1, i.e., $< 0.3T_m$ (for metals), this first zone consists of tapered grains; the surface has a domed structure; and the diameter of the domes increases with temperature. For Al, whose melting point is 659.7°C (932.7 K), $T_1 \sim 7$°C. Levenson (1989) described the structure as column-like bundles separated by voids. A smooth transition to a second zone occurs at about $T1$. In this second zone there is a clearly defined columnar structure with a smooth matt surface. There are

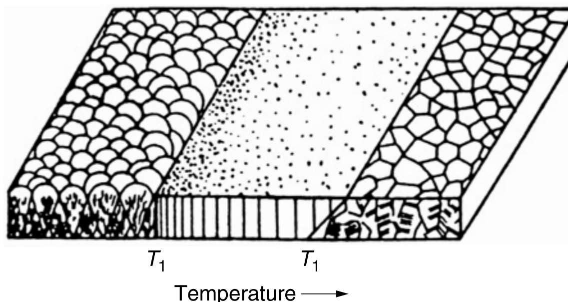

Figure 5.14 Temperature dependence of structural zones in a metal film. (From Movchan, B.A. and A.V. Demchishin, *Fiz. Metal. Mettaloved*, 28, 83, 1969.)

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well-defined grain boundaries (width ~ 5 Å) (Srolovitz et al., 1988) in this structure; the width of the columnar crystallite increases with increasing *T*. There is no porosity. The slope of the columns is related to the angle of incidence of the incoming vapor. Zone 3 is formed at $0.5T_m$ at which temperature the columnar grains gradually change to relatively large equiaxed (same size in all directions) grains. The surface is rough, with roughness increasing with increasing temperature. The activation energy for grain growth in Al films corresponds to that for grain boundary diffusion in bulk Al (Levenson, 1989). Microhardness, strength, and ductility of the films are determined by the structure features of the zone in which they were formed (Movchan and Demchishin, 1969).

Although the formation of columns depends on the deposition conditions as well as on the material itself, these structures are observed only when the mobility of the atoms is limited (Dirks and Leamy, 1977). Tait et al. (1992) state that their ballistic model confirms that the structure is due to self-shadowing and limited diffusion.

5.9.2.2 Sputtered Films

A fourth zone (termed T) lying between zones 1 and 2 was identified in sputtered films deposited at low Ar pressures. It consisted of a dense array of poorly defined fibrous grains. Its existence is largely a consequence of the bombarding effect of the ions. Intense energetic ion bombardment during deposition can largely suppress the development of the open structures in zone 1. The formation of voided structures at high Ar pressures was much less at low deposition rates. Also, at high Ar pressures, the columnar grains of zone 2 tended to be faceted. Suppression of open boundaries required an ion flux adequate to resputter 30 to 60% of the incident flux of incoming species; the required resputtering flux increased with the size of surface irregularities. However, resputtering itself is not the major effect; that is postulated to be drive-in of knock-on atoms into the bulk (Thornton, 1986).

5.9.2.3 CVD Films

Columnar microstructure is seen in refractory metal, nitride, and silicide films, but there have been no reports on structural analysis of CVD films of Al, AlCu, or Cu. The successful application of the zone model to evaporated and sputtered metal films whose melting points cover a wide range makes it likely that the structure these CVD films can also be described by the zone model.

5.9.2.4 Effect of Oblique Incidence

Column formation is more prominent in films produced by oblique incidence angle. The orientation of columns in films deposited at oblique incidence is always more nearly perpendicular to the substrate than the vapor beam direction (Dirks and Leamy, 1977). This is often expressed by the tangent rule: $2\tan\beta = \tan\alpha$, where β is the angle between the columns and the substrate normal and α is the angle between the source direction and the substrate normal. However, it has been reported that the inclination angle of the columns depends on the deposition parameters, such as temperature, deposition rate, pressure, and vapor density, so that the range of parameters where the tangent rule is obeyed are narrow and very limited (Fujiwara et al., 1988). Nonzero tilting angles are a consequence of atomic shadowing (Mazor et al., 1989). A three-dimensional ballistic deposition model for thin-film growth incorporates the mechanisms of shadowing and relaxation. The simulation produces columns which become elliptic as the angle of the vapor flux is increased. A vapor stream normal to the surface of a film is oblique at edges (Tait et al., 1992, 1993).

In thin films, the grain size and growth depend on substrate temperature, rate of deposition, film thickness, alloy content, and postdeposition annealing temperature. After annealing evaporated films, the θ particles in AlCu films tended to be localized at grain boundaries and triple points.

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During device processing, films are annealed after patterning; the ultimate grain size was believed to be determined by the film thickness and line width. Columnar and bamboo grain structures were enhanced in annealed submicrometer lines (Kwok et al., 1985). In a study of sputtered AlCuSi blanket films, it was proposed that the preferred orientation of the grains was affected by the Cu concentration, the mobility of the grain boundary, and the location of Cu precipitates. If the θ-phase is precipitated, the as-deposited film will have a less preferred orientation, and smaller grain growth rate both before and after annealing than a film without θ-phase precipitates. This was thought to be due to the prevention of coalescence of grains. Excessive heating in the early stages of film growth degrades preferred orientation (Shimamura et al., 1991).

5.9.2.5 Grain Structure of Electroplated Cu Films

As stated in Section 5.4.4.4, Cu films deposited from baths formulated for superfilling undergo a spontaneous transformation (self-annealing at room temperature (RTSA)) of grain size and structure, resistivity, and mechanical properties. In addition to the factors discussed below, the rate of transformation depends on various plating parameters, e.g., plating rate (current density), composition of the bath (particularly the additives), and age/temperature of the bath. Variations in plating procedures probably account for disagreements among the reported results.

The as-deposited films are fine-grained and shiny and have a high resistivity (~2.2 $\mu\Omega$ cm). STEM cross-sections showed numerous small grains throughout the film as well as twins and dislocations; the PVD seed layer was not distinguishable from the plated film (Gignac et al., 1999).

Neither IMP nor DC magnetron-sputtered Cu undergo such a transformation (Chen et al., 1999). When a sputtered Cu film underlies a plated Cu film, however, RTSA of the plated Cu drives a similar crystal growth in the PVD film even as thick as 1 μm. The additives used in plating appeared to have diffused into the PVD layer (Gross et al., 2000).

The smaller the grain size of the seed layer (the lower its deposition temperature), the smaller the grain size of the as-plated film and the faster its rate of self-annealing. Reducing the temperature of the plating bath resulted in films having a higher resistivity but a more rapid RTSA rate (Jiang et al., 1999a; Grunow et al., 1999). The grain size of the PVD barrier and CVD Cu seed had little influence on the grain size of the plated film but the as-plated film had a texture similar to the seed layer upon which it was deposited (Grunow et al., 1999; Ueno et al., 1999). This was confirmed by Hara et al. (2002) who showed that the intensity ratio of (111)/(200) in the electroplated Cu was closely correlated with that in the sputtered seed layers, which, in turn, depended principally on the barrier layer. Highly oriented seed layers were formed on $TaSi_{0.1}N_{0.57}$ barriers. They found that the (111) orientation in plated Cu cannot be controlled by plating conditions. Ueno et al. (1999) compared films plated on textured and nontextured seed layers; films plated on a nontextured seed layer transformed more quickly. This was explained by Rosenberg et al. (2000): the grain boundary energy is lower in the textured film and thus there is less of a driving force for grain growth. The higher the c.d., the smaller the grain size in the as-deposited film (Grunow et al., 1999).

Reduction in the resistivity of the films to near-bulk value of 1.7 $\mu\Omega$ cm is one of the striking manifestations of RTSA. An incubation period has been noted (e.g., Cabral et al., 1999; Walther et al., 2000; Jiang and Thomas, 2001) for blanket films. A correlation between the rates of fractional change in sheet resistance and the area fraction recrystallized, as measured by focused ion beam (FIB) secondary electron imaging, is shown in Figure 5.15 (Gignac et al., 1999). In contrast to this, Walther et al. (2000) (using the same measurement techniques) reported that the rates of recrystallization from FIB analysis were consistently faster than those from resistivity measurements. They explained their results as follows: the plan view, which gives direct evidence of crystal growth, is a two-dimensional view of the film surface whereas resistivity measurements, while indirect, provide three-dimensional information. They pointed out that differences between the two kinds of measurements support the view that nucleation of recrystallization occurs near the surface and extends

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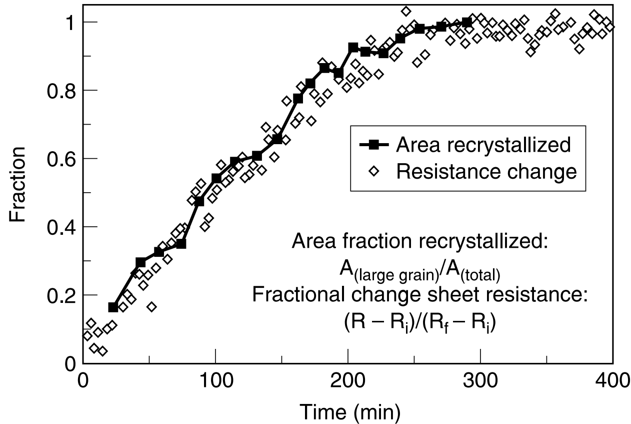

Figure 5.15 RTSA: correlation of time dependence of the area fraction recrystallized and the fractional change in sheet resistance. (From Gignac, L.M., K.P. Rodbell, C. Cabral, Jr., P.C. Andricacos, P.M. Rice, R.D. Beyers, P.S. Locke, and S.J. Klepeis, *Mater. Res. Soc. Symp. Proc.*, 564, 373, 1999.)

laterally more rapidly than vertically. They noted the importance of differences in the plating process and the location on the wafer where measurements are made; perhaps by inference, that explains the disparity between the results of Gignac et al. and Walthers et al.

The thicker the film, the faster and greater the decrease in resistivity; the final resistivity was lowest for the thickest film (e.g., Walther et al., 2000; Jiang and Thomas, 2001). The lower resistivity of the thicker films was attributed to the formation of larger grains throughout the film. (Gignac et al., 1999). Brongersma et al. (1999) explained the dependence of the rate of self-annealing on film thickness in terms of a two-step grain growth process: a very rapid initial crystallization from the top surface down then a slower lateral recrystallization producing larger secondary grains. The slower transformation of the thinner films was postulated to be due to the physical restriction as the thickness and grain size of the recrystallized approach the same value, forcing grain growth laterally (Lagrange et al., 2000).

Jiang and Thomas compared a blanket Cu film with a damascene line of the same thickness and found that the resistivity of the blanket film decreased at a much faster rate than did that of the line (~5 days vs. 36 days); the final reduction in resistivity was 20% for the blanket film but only 11% for the line.

Jiang and Thomas (2001) also measured the effect of the anneal temperature (17 to 80°C) on the rate of resistivity decrease for blanket films 0.8, 1.2, and 1.6 μm thick. From the time at which the resistivity fell by 10%, they arrived at an activation energy (E_a) of ~0.8 eV for all the films, although the transformation times were longer for the thinner films. This indicated that the mechanism was not a function of thickness. The rate of resistance decrease with temperature for lines of different widths (0.25 to 1.06 μm) was also measured to determine E_a. Although the spread of the data was large, the average activation energy for the resistance transformation for the lines was also ~0.8 eV. Thus, although the rates depended on the physical constraints of the system, the mechanism responsible for the change in resistivity is the same. A different value for the activation energy (1.1 eV) was calculated on the basis of the time to complete half the resistivity decrease (Ritzdorf et al., 1998). A value of 0.92 eV was reported by Cabral et al. (1999); they stated that this value was consistent with grain boundary diffusion as the dominant mechanism.

The decrease in resistivity is due to recrystallization, i.e., to the abnormal growth in grain size from an initial value of 0.05 to 0.1 μm to >1 μm (depending on the thickness of the film). Abnormal growth refers to growth by coalescence of small grains. "The driving force is the grain boundary

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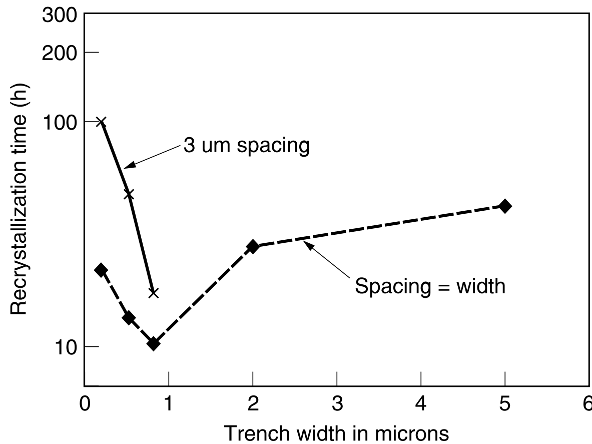

Figure 5.16 Recrystllization time (t_R) vs. trench width. (Adapted from Lingt, C. and M.E. Gross, *J. Appl. Phys.*, 84, 5547, 1998.)

energy density in the fine-grained as-deposited film" initially pinned by impurity incorporation during the plating process (Harper et al., 1999). The elimination of electron scattering at grain boundaries and defect elimination (fewer electron scattering centers) during grain growth are probably responsible for the reduction in resistivity (Rosenberg et al., 2000).

The recrystallized grains were columnar and highly twined and the large grains spanned the full thickness of the film. Jiang and Thomas (2001) examined a 0.25 μm wide damascene line after annealing and found that the final microstructure was bamboo-like. They stated that "microstructural images of damascene structures clearly indicated that wider Cu lines transform much faster than narrower ones." The data derived from resistance rate vs. temperature measurements, however, do not support this broad conclusion. Those data indicate a maximum rate of resistivity decrease for the 0.35 μm lines, a slight decrease in rate as the line widths increased to 1.06 μm and a drastic decrease in rate for the 0.25 μm line.

Lingk and Gross (1998) also studied the recrystallization rates of plated Cu using FIB secondary electron images. They reported that when Cu was plated into small trenches (0.3 to 5 μm wide), recrystallization was initiated at the upper corners of the trenches. The grains then grew laterally across the trenches, and finally between them, until the entire film was transformed. In superfilling, deposition is strongly suppressed at these corner sites. Gross et al. (1999a) suggested that there is "an indirect influence of the additives on recrystallization through formation of more defects, dislocations, and/or stresses at these sites, rather than more directly through higher impurity incorporation." Lingk and Gross (1998) measured the rate of recrystallization for both line width and the space between lines. For line widths of 0.3, 0.5, 0.8, 2, and 5 μm, the minimum time for recrystallization (t_R) was for the 0.8 μm line, as shown in Figure 5.16 (in qualitative agreement with the thermal data of Jiang and Thomas (2001)). As the space between the trenches increased, t_R increased. The explanation for the general shape of the t_R vs. width curve is as follows: (1) wide trenches/spaces separate the corners so that the structure resembles a flat surface with few nucleation sites and (2) for very narrow spaces the corners are too close and dislocation densities around the corners even out and the structure resembles a blanket film with an increase in t_R, so that a minimum value of t_R for intermediate-size trenches might be expected. Another explanation (Gross et al., 1999a) for a minimum value of t_R is in terms of the relative density of high-defect regions. At the smallest widths, there may be a uniform distribution of defects; at the largest, the upper corners are sufficiently separated to appear as discrete steps; at intermediate widths there is the highest net variation in defects. Grunow et al. (1999) observed no RTSA-induced grain growth in very fine

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trenches (0.15 to 0.25 μm). The self-annealing behavior seemed to be stopped at the entrance of the trenches, leaving the ECD Cu in the actual device features in a polycrystalline form. Gross et al. (2000), however, did not entirely agree; they stated that the very narrowest trenches did not recrystallize fully.

Lingk and Gross (1998) found that if the overlying Cu was removed by CMP immediately after plating, the recrystallization of the remaining Cu was severely inhibited and there was evidence of the sidewall texture of the (111) planes of the as-plated film. The incomplete recrystallization was postulated to be due to the loss of nucleation sites. When recrystallization of the Cu grains preceded CMP, only a (111) fiber texture was observed inside the trenches.

A low-temperature anneal should therefore precede CMP to ensure stable large-grained interconnections (Lingt et al., 1999). It is not clear whether the difference in the rate for blanket films and damascene trenches of the same thickness, reported by Jiang and Thomas (2001) was due to the fact that the trenches were polished before measurements were made.

The recrystallization rate of Cu plated in an old bath (one which was used to plate many wafers and, therefore, had had its composition adjusted to replenish the additives consumed in the process) was higher than that of Cu plated in a freshly prepared bath, but there was no influence on the texture. Since the impurity levels in the two baths were comparable, the difference was attributed to a variation in the Cu/organic interactions giving rise to different defect densities. There was no discussion, however, about why or how this variation arose or produced its effect (Gross et al., 1999b).

There is disagreement about the change in texture after transformation. Some authors report that the films exhibited a higher degree of (111) texture (Ritzdorf et al., 1998; Rosenberg et al., 2000), while others did not find that the peak intensity changed. It is generally agreed, however, that the peak width (FWHM) became narrower with time indicating a better alignment of grains (e.g., Lagrange et al., 2000; Ritzdorf et al., 2000; Grunow et al., 1999; Chen et al., 1999). Chen et al. (1999) showed that the decrease in FWHM with time was similar to that of the resistivity change.

The as-deposited films have a low compressive stress. Due to grain growth, there is a loss in the volume of the grain boundaries so that the films shrink. The stress changes with time, becoming less compressive; the annealed films are nearly stress-free (Harper et al., 1999). Cabral et al. (1999) reported that the changes in resistivity and stress followed the same trend; they concluded that both may be related to the same changes in microstructure. Lagrange et al. (2000) disagreed. They found that the rates and extents of change in stress and resistivity were different. The thinner the film, the greater the stress relaxation. In addition, the resistivity change started slowly and then accelerated whereas the decrease in stress started immediately after plating and stopped after a shorter time than did the resistivity decrease. This, they postulated, indicates that the stress stabilizes before grain growth is complete and the two phenomena may not be linked or influenced by the same parameters. They found some time correlation between stress and chemical desorption from the film.

During RTSA, the hardness of a 1.6 μm film increased initially, then decreased abruptly and remained constant at a low value (Jiang and Smekalin, 1999); this is illustrated in Figure 5.17).

Because of the dependence of RTSA on the many parameters discussed above, it is standard practice in using ECD Cu to anneal the samples (perhaps using rapid thermal processing to increase throughput and reduce the thermal budget) to ensure stable large grained interconnections and to stabilize the resistivity and mechanical properties, and to eliminate feature size/distribution effects. Finally, the metal film is polished. Figure 5.18 shows a FIB cross-section showing an embedded planar structure and a top view showing the grain structure.

5.10 CHAPTER SUMMARY

From the point of view of the interconnections, most of the learning and the innovations over the last four decades have been in processing the good conductors, Al and Cu and, to a much lesser

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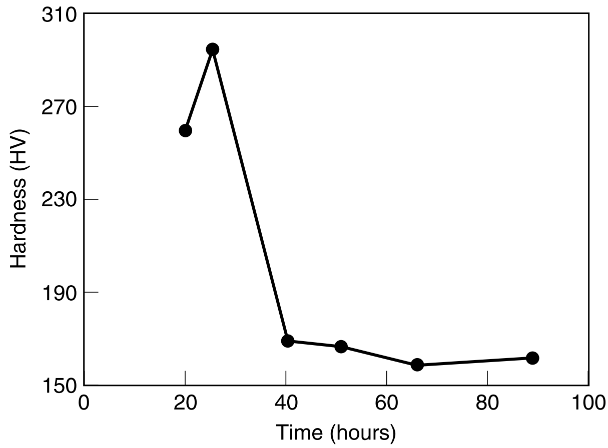

Figure 5.17 Hardness and resistivity change as a function of time of a thick (>1 μm) plated Cu film. (Adapted from Jiang, Q.-T. and K. Smekalin, *Mater. Res. Soc. Conf. Proc.*, ULSI XIV, 209, 1999.)

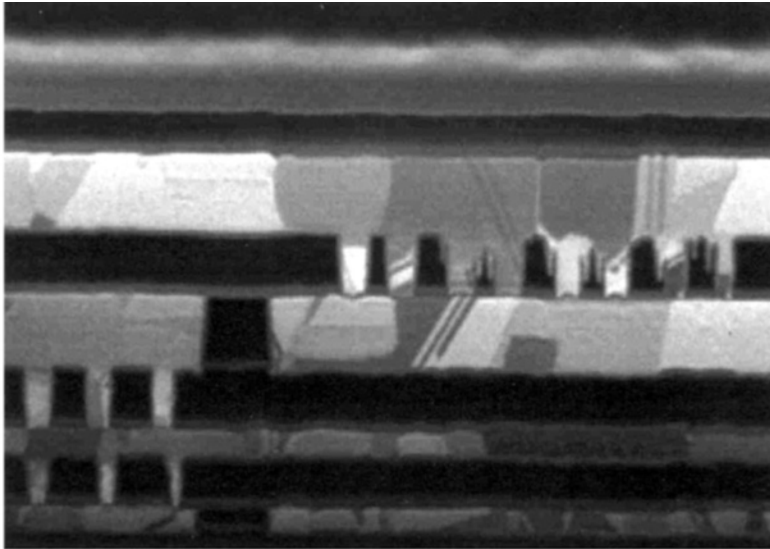

Figure 5.18 FIB cross-section and top view of a plated Cu line on a product wafer: after annealing and CMP.

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extent, Ag and Au. The learning has been in the area of reliability as dimensions have continued to shrink; the innovations have been in methods to deposit and pattern the films in very small dimensions and narrow features with a high aspect ratio. We saw significant efforts in liner materials and deposition techniques. Incorporation of liners has become routine, for one or more of the following reasons: improve electromigration lifetimes, act as a barrier to diffusion into insulators and ultimately Si, improve adhesion and promote nucleation and growth for some deposition processes. Tungsten as a contact stud seems to be well established. The invention of CMP as a way to pattern metals from prior additive or subtractive techniques drove new deposition techniques and enabled wide use of copper interconnections. It is interesting to speculate what changes are ahead for metals. If the past is any indication, it is safe to assume that the changes will be predominately in the area of processes and liner materials, changes being driven by economic and reliable processes, and continued shrinking of device features. The migration to porous conductors will present its own unique challenges and is likely to drive innovations in liners and methods for forming liners and conductors. Moving from copper as the main conductor is feasible perhaps at cryogenic use conditions, but it is hard to visualize uses of semiconductors under cryogenic conditions becoming common in any foreseeable future.

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CHAPTER 6

Chip Integration

Geraldine Cogin Schwartz and K.V. Srikrishnan

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6.1 INTRODUCTION

There are two aspects of chip integration: one is concerned with the problems created by topography (Section 6.2 through Section 6.24) and the other with the compatibility of materials and processing (Section 6.25 through Section 6.31).

The discussion of topography encompasses not only the elimination of surface irregularity, i.e., planarization processes, but also the earlier problems of step coverage and gap-fill (filling the spaces between adjacent conductors with dielectric films and filling via holes in the dielectrics with metal films), some of which have been become less demanding since the introduction of dual damascene (DD) processing (Section 6.16.3) with chemical mechanical planarization (CMP) (Section 6.17).

Compatibility issues, covered in Section 6.25 through 6.31, are (1) the interactions of the various components of the device structure with each other and their response to the processing conditions and (2) the effects of the choice of processing methods and conditions on the components and on the final device, i.e., its structure, performance, and reliability.

6.2 TOPOGRAPHY, STEP COVERAGE, AND PLANARIZATION

6.2.1 Overview

Topography is a natural result of building a device structure using multiple levels of wiring; these processes require depositing or growing films and patterning them repeatedly, thus creating steps in the different layers. Until the advent of the dual damascene process (DD) and chemical mechanical planarization (CMP), coverage of these steps by films depended on the deposition process involved and good step coverage was required to meet yield and reliability objectives.

Planarization is characterized in Figure 6.1 as partial with edge smoothing, local, or global. The ultimate aim is global planarization, but along the way, many processes with less far-reaching goals have been developed.

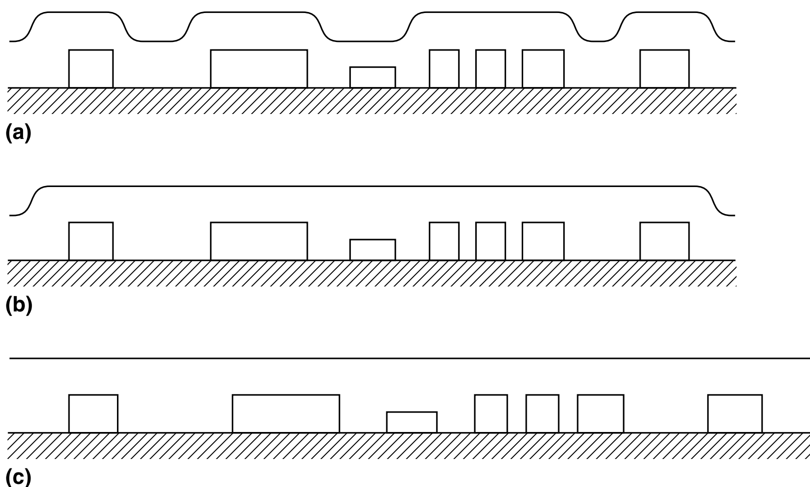

Figure 6.1 Characterization of planarization. Top: partial planarization and edge smoothing; middle: local planarization; bottom: global planarization.

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The variety of deposition methods which evolved to minimize topography and maximize gap fill will be explored since those used, particularly for metal deposition, are still of major importance.

6.2.2 Topography

6.2.2.1 Introduction

A description of building early multilevel devices follows. After the structures within the semiconductor substrate have been completed, the surface is coated by an insulator to isolate the devices from the overlying structures. In the case of silicon devices, this layer is thermally grown SiO_2. Connections must then be made to the devices at the appropriate locations; therefore, so-called contact holes must be etched through the insulator. This introduces topography, i.e., a nonplanar surface. A metal film may be deposited into this hole or, more recently, the hole may be filled by a vertical interconnect. This illustrates facets of the problems of topography, i.e., step coverage (how well does the metal layer cover the sides of the contact hole?) and gap-fill (how well does the metal fill the contact hole?).

6.2.2.2 Consequences

6.2.2.2.1 Structural

Vertical interconnects can result in a planar surface, eliminating the topography due to the contact hole. But the problem re-emerges when the first-level conductor is formed. And, as each successive level of the metal–insulator structure is built, the steps become deeper, since the successive layers are usually thicker. Metal films are thickened to decrease line resistance and increase electromigration resistance; insulator films are thickened to reduce capacitance and to cover the thicker metal layers adequately. The trend toward increased numbers of levels is accompanied by a decrease in device and interconnection dimensions as well as an increase in packing density. And as deep steps become steeper to accommodate the increased density, the difficulties of step coverage and hole-fill increase. In addition, residues formed during RIE are less tractable if the sidewalls are steep, adding to reactive ion etching (RIE) selectivity problems. Thickness variations in the interlevel dielectric result in variation of the interlevel capacitance.

6.2.2.2.2 Lithographic

Another deleterious consequence of topography is the loss of line-width control in lithography. The thickness of a photoresist film changes as the film is spun-on over a step (Widman and Binder, 1974; Lin et al., 1984; Thompson, 1994). The resist is thinnest at the top of the step. Its thickness (t_a) can be approximated as

$$t_a \sim t_n[1 - 1/2(s/t_n)^2]$$

where s = step height, t_n = nominal thickness of resist, and t_b = the thickest resist at the bottom of the step:

$$t_b = t_a + s$$

There is a corresponding change in pattern dimensions; the image is largest where the resist is thickest (Lin et al., 1984); the variation increases as the step height increases; any variation in dimension becomes more serious as the dimensions decrease. The use of an antireflection (AR) coating reduces, but does not eliminate, the variation (Lin et al., 1984; Horn, 1991).

Thick resist films are more planar than thinner ones (White, 1983; Pampalone et al., 1986). However, since Fresnel diffraction limits the resolution of the minimal pitch (resolution $= 3[\lambda(d/2)]^{1/2}$), increasing the resist thickness (d) degrades the lithographic performance.

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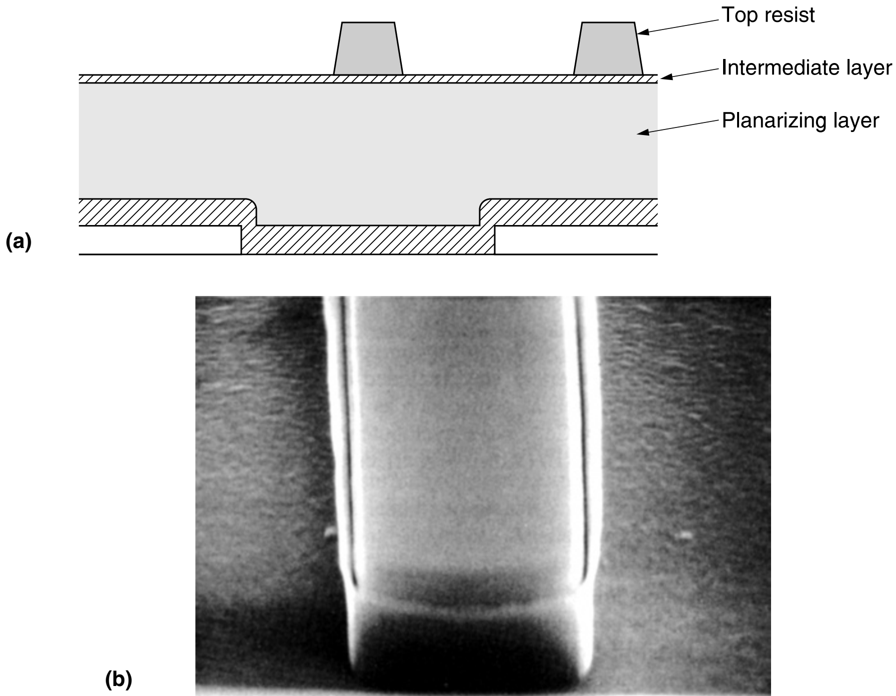

Figure 6.2 (a) Starting structure for a typical trilevel mask. (b) SEM image of the sidewall coating formed during RIE in O_2 of the thick planarizing (organic) layer.

The use of multilevel resist masks is a technique for achieving planarity and acuity. Figure 6.2a shows the starting structure in the fabrication of a trilevel mask after patterning the thin resist film. The resist pattern is used as a mask during RIE of the intermediate (barrier) layer (e.g., silicon oxide, nitride, or SOG) which does not etch in O_2. The patterned barrier layer then acts as the mask during RIE in O_2 of the organic film, forming the ultimate thick mask for etching the substrate. However, during RIE of the organic underlay in O_2, there is redeposition on the sidewall of the resist, during etching by sputtering of the inorganic barrier layer, and during the overetch period by sputtering of the substrate (Kinsbron et al., 1982). The coating on the sidewalls of a mask formed by RIE in O_2 (with an overetch of 100%) on an AlCu substrate is shown in the SEM image of Figure 6.2b, but such sidewall films have been found on many other kinds of substrates. This film must be removed before etching the underlay, without shifting or otherwise distorting the organic mask, in order to preserve the dimensions of the initial mask. Thus it is clear that the use of such masks increases both the number of layers and processing steps and requires RIE equipment in addition to the usual ones used for lithography. The patterning process becomes more complex and, therefore, more costly.

There are also line-width variations caused by reflections off topographic features within the resist layer although it may be planarized. This is due to standing waves in the resist image (Lin, 1983), as shown in Figure 6.3.

Another lithographic issue is the depth-of-focus (DOF). To improve the resolution of the resist image, the DOF must be decreased. However, variation in surface height can result in exceeding the in-focus condition for submicrometer imaging; out-of-focus images lose fidelity, especially for closely pitched features (Moreau, 1988; Bothra et al., 1995).

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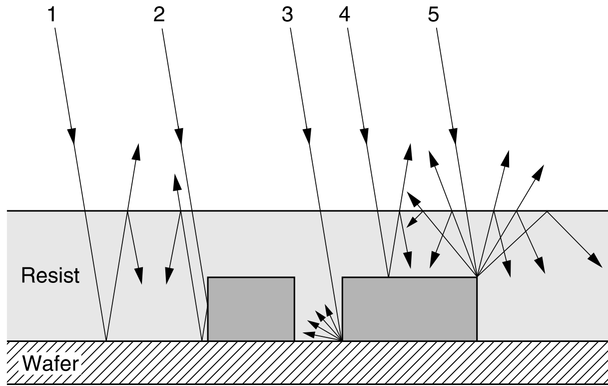

Figure 6.3 Reflection off topographical features. (Reprinted from Thompson et al., *Introduction to Microlithography*, 2nd ed., 1984. Copyright 1984, American Chemical Society. With permission.)

6.2.2.3 Organization

The sections on planarization are organized to consider, first, the traditional aspects of planarization; these include step coverage and gap-fill as well as surface leveling. In the second section, we cover CMP, which tacitly assumes that the underlying structures have been adequately protected using the methods in the earlier sections. In both sections, dielectrics are covered before metals.

6.3 SPIN-ON FILMS*

Many spin-on films were developed for their planarizing properties, but that attribute is no longer of great interest. Many of the films (e.g., PI, BCB, FOx, etc.) are now employed as low-ε interlevel dielectrics.

6.4 STEP COVERAGE BY DEPOSITED FILMS

6.4.1 Characterization

Step coverage by deposited films, such as those formed by evaporation, sputtering, and blanket CVD and PECVD processes, is very different from that of spin-on films. Whatever mechanisms dominate the processes, it is found that it is more difficult to cover vertical sidewalls than tapered ones and to fill features completely (i.e., void-/seam-free) as the aspect ratio (AR) increases, as illustrated in Figure 6.4a.

Geometric shadowing as well as the deposition conditions now play a dominant role (Levin and Evans-Lutterodt, 1983). The sides of a feature limit the acceptance angle of the incoming species so that, in most cases, the deposit along the sidewall decreases in thickness with increasing depth. Step coverage is often characterized by the ratio $\text{thickness}_{(\text{inside corner})}/\text{thickness}_{(\text{horizontal surface})}$. If the sides are closely spaced, the films deposited on the top edges may converge, creating a void within the deposit.

When the mobility of the incoming species is large, i.e., the sticking coefficient (sc) is low, so that shadowing effects become negligible and/or the mechanism of film formation insures it, equal thicknesses can be formed on all surfaces; such conformal coverage, shown in Figure 6.4b (top) is

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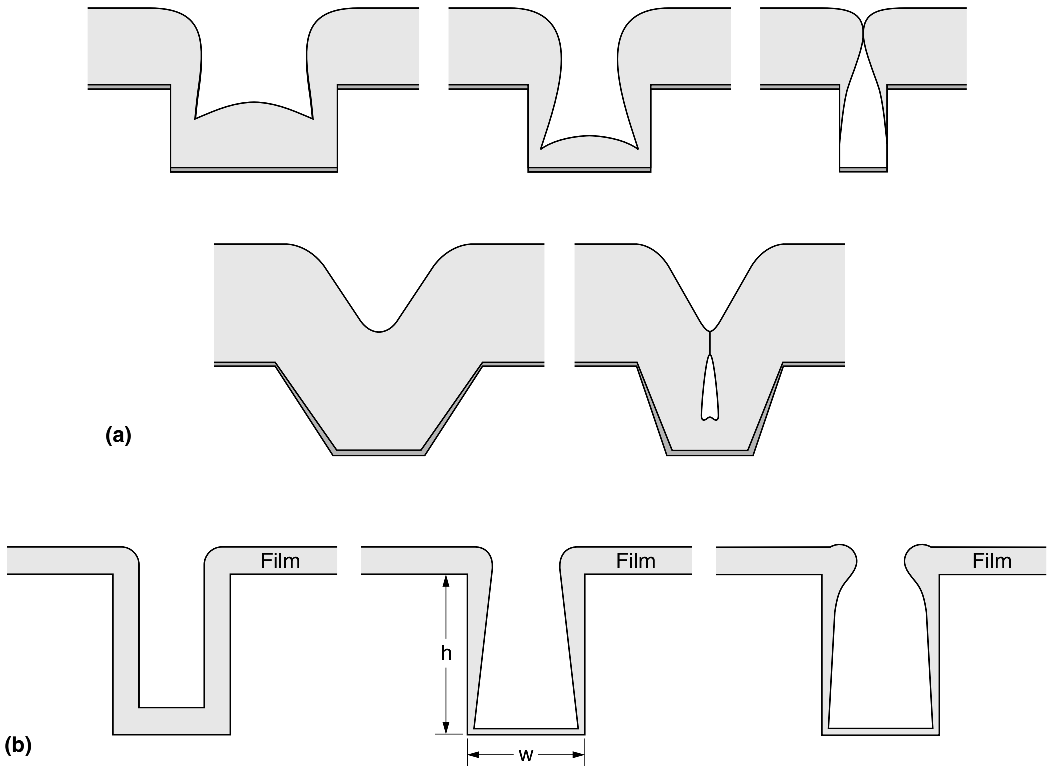

Figure 6.4 (a) Effect on step coverage of aspect ratio (top) and wall angle (bottom). (b) Typical step coverage profiles of deposited films. Top: conformal. Middle: nonconformal; long mfp, mobile precursor. Bottom: nonconformal; short mfp, little or no mobility.

very reliable. Although voids are not formed when the coverage is conformal, a seam may exist at the center of the space where the films growing out from each side merge. If conditions are optimal, W deposited by LPCVD from WF_6 and H_2 and SiO_2 deposited by HPCVD from TEOS plus O_3 exhibit conformal step coverage. The conformality of the SiO_2 film has been attributed to the liquid-like flow of the precursor. Figure 6.4b (middle) illustrates the coverage when the film precursor is mobile and the conditions are such that they have a long mean free path. SiO_2 deposited by PECVD using TEOS and O_2 is one example. Figure 6.4b (bottom) is an example of the coverage when the mean free path is short and/or there is little or no precursor mobility; reduced mobility apparently accounts for the SiO_2 profile when the film is deposited using SiH_4 as the precursor or in sputter deposition of Al.

6.4.2 CVD Oxides

Although in DD the dielectric film is deposited on a planar surface, in more traditional processing of devices (on which the feature sizes have not been shrunk toward the limit) the problems of coverage and fill are still important.

6.4.2.1 Models

The principal mechanisms describing step coverage of CVD SiO_2, as modeled by Cheng et al. (1989) and Rey et al. (1991) and confirmed by experiments, were direct deposition and re-emission;

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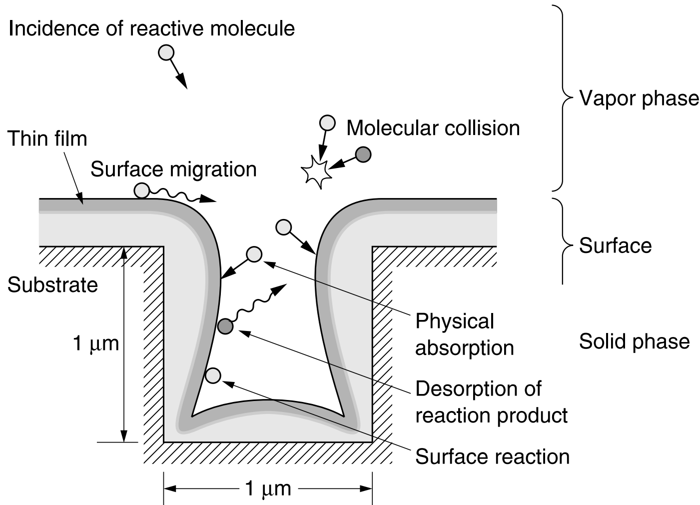

Figure 6.5 Species and processes involved in a physical model for thin-film deposition used in simulation by the Monte Carlo method. (Reproduced from Ikegawa, M. and J. Kobayashi, *J. Electrochem.Soc.*, 136, 2982, in *Multilevel Metallization, Interconnection and Contact Technologies*, L.B. Rothman and T. Hendon, eds., Electrochem Soc. Proc. Vol., Pv-87-4, 259, 1989. With permission of the Electrochemical Society, Inc.)

surface diffusion was negligible. Re-emission of deposited material is determined by the reaction probability or sc of the impinging species; a low sc is key to good step coverage. The value of sc decreases with increasing temperature and depends on the nature of the Si source: it is high for SiH_4 (leading to bread-loafing or overhang formation) and low for organic precursors. The lower the value of sc, the steeper the sidewall angle that can be filled without void formation (Rey et al., 1990). A more accurate simulation (Islam Raja et al., 1993) included two rate-limiting precursors, an intermediate species, sc ~ 1, formed by gas phase reactions, and one with low sc (formed from the source gas), reacting separately with the surface to form the film. The increase in step coverage and deposition rate with increasing pressure is due to the change in the ratio of the partial pressures of the two precursors with pressure.

Profile evolution for processes ranging from vacuum to atmospheric conditions was simulated by Ikegawa and Kobayashi (1989); the physical model of the deposition process is shown in Figure 6.5. Movement in the gas phase was characterized by the Knudsen number (Kn): $Kn > 10$, collisionless (PVD, LPCVD); $10^{-2} < Kn < 10$, transitional (APCVD). Other parameters investigated were sc and AR/feature geometry. The step coverage degraded as the value of sc increased. Coverage is better over trenches than holes and depends on the position in the hole as well. As observed experimentally, the simulation predicted that as the value of AR increased, step coverage degraded.

*6.4.2.2 Improvements**

The use of F-substituted Si sources improved step coverage and gap-fill.

The mechanism for gap fill has been postulated to be plasma-assisted etching of the depositing film by the F-species in the plasma (Matsuda et al., 1995). As discussed in Chapter 4, however, the reduced value of ε may be more of a driving force in the development of F-doped oxides while questions of stability, leakage, reliability, etc., may ultimately determine the acceptance of them.

Planarized, gap-filling SiO_2, which uses a CVD process called "FLOWFILL"™, is discussed in Chapter 4.

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6.4.3 Capacitively Coupled PECVD Oxides

The profiles of films deposited in these reactors are similar to those deposited by thermally activated CVD (Ross and Vossen, 1984) (except for those deposited using TEOS and O_3 which are usually conformal, as noted above).

6.4.3.1 Models

PECVD in a capacitively coupled reactor was studied by Chang et al. (1992) who expanded their model of CVD deposition to include ion bombardment. They concluded that the ion and neutral (LPCVD) components behave independently. The ion flux was responsible for the high rate and directionality of the deposit. Ion bombardment increased sc on the exposed surfaces; the neutral component was nearly isotropic with a low (~0.15) sc.

Cale et al. (1992) used a similar model which predicted that both conformality and rate decreased as the temperature increased and as the pressure increased (more collisions in the sheath). Conformaility increases as the input RF power increases since the fraction of ions increases.

*6.4.3.2 Improvements**

PECVD processes have been modified in an attempt to improve the conformality or gap-fill by changing the reactant mixture, surface mobility, etc.

6.5 *IN SITU* PLANARIZATION/GAP-FILL OF DIELECTRIC FILMS

6.5.1 Introduction

In situ processing refers either to the use of reactors in which deposition and contour modification occur simultaneously or else to the use of integrated reactors in which the films are deposited in one chamber and transferred *in vacuo* to a second chamber for modification.

6.5.2 Bias Sputter Deposition

*6.5.2.1 Planarization**

Planarization depends on the angular dependence of the sputtering yield (discussed in Chapter 1) leading to the formation of a stable facet angle. It is accomplished by the use of a high substrate bias, which promotes resputtering, during sputter deposition (Ting et al., 1978; Mogami, 1985; Singh, 1987). The process was used to deposit SiO_2 over etched conductors. Only narrow lines can be planarized by this technique in a reasonable length of time, limiting its usefulness.

*6.5.2.2 Gap-Fill**

A model based on the same phenomena used to describe planarization explained the difficulty of filling deep narrow vertical features and why filling improved as the substrate bias is increased (Logan et al., 1989).

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6.5.3 Biased PECVD in a Capacitively Coupled Reactor

6.5.3.1 Sidewall Tapering

Tapering the sidewalls of PECVD films depends on the angle-dependent sputter etch rate. In an early version of the process, deposition (using SiH_4) and etching occurred at the same time. This was accomplished by applying a large negative bias to the substrate and using an oxidant which etched the film as it grew (Smith and Purdes, 1985). Another version used $SiCl_4/O_2$ in which $SiCl_4$ was the etchant (Sato and Arita, 1986). McInerney and Avanino (1987) achieved the same result using cycles of deposition in SiH_4/N_2O and *in vacuo* transfer to a sputtering chamber in which Ar was the inert etchant.

6.5.3.2 Planarization and Gap-Fill

Sidewall tapering was inadequate for the needs of building multilevel structures. By increasing the substrate bias in the etch step, planarization of the oxide surface was achieved. It became more important, however, to use this technique for gap-fill rather than for planarization. Gap-fill was accomplished by (1) substituting TEOS for SiH_4 as the Si source to avoid the bread-loafing profile, typical when using SiH_4, which makes gap-filling extremely difficult and (2) using a process based on that of McInerney and Avinino (1987) and in a multichamber reactor with *in vacuo* transfer between a deposition and a sputter etch chamber. A typical process sequence is shown in Figure 6.6 (Bader et al., 1990).

The process then became known (in the jargon of the industry) as dep-etch, rather than biased PECVD. A simplification is to deposit only the thickness needed to cover the metal as the final step (Schwartz and Johns, 1992). The resulting structure may then be planarized by etchback or by CMP (Section 6.17).

As with bias sputtering, it becomes more difficult to fill gaps without forming voids if the AR, sidewall angle, or depth of the gap increase (Schwartz and Johns, 1992). The number of cycles

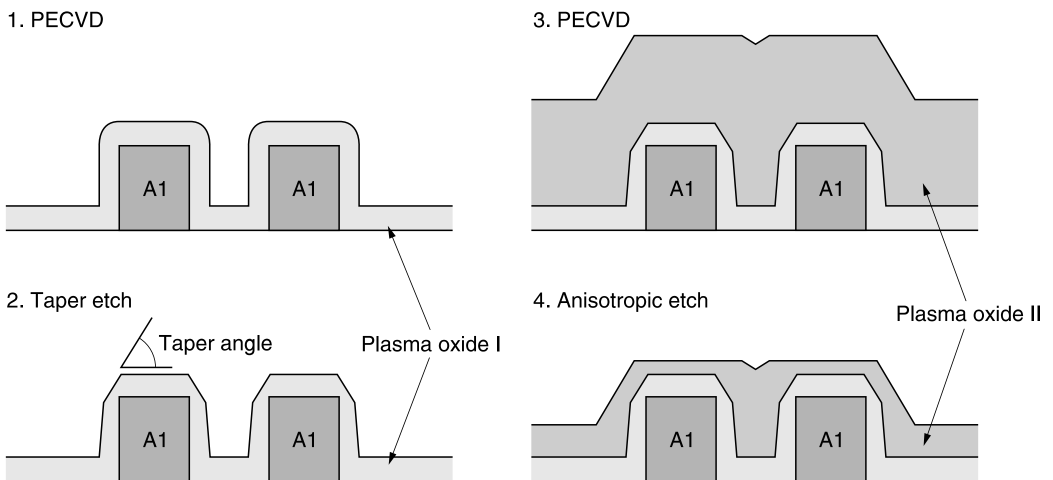

Figure 6.6 Integrated process for forming an interlevel dielectric using TEOS-based PECVD and thermal CVD oxide films and etchback. (Reprinted from Bader, M.E., R.P. Hall, and G. Strasser, *Solid State Technology*, 5/90,149, 1990. With permission)

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required for void-free fill depended on the characteristics of the gap. Their duration as well as their number can be tailored, to some extent, to fill very steep, deep, and narrow gaps. However, throughput concerns, rather than physical limits, restrict the ultimate process capability.

Another approach, which was reported to result in a greater degree of planarization as well as good gap-fill, used a sacrificial film of PECVD B_2O_3 which flows during deposition (Marks et al. 1989; Pennington and Hallock, 1990). This process is illustrated in Figure 6.7.

To minimize particulate contamination, reactive plasma cleaning of the chambers is often carried out after processing each wafer. This adds to the overall process time.

6.5.4 Biased High-Density PECVD

The most promising gap-filling techniques for deep, narrow holes with SiO_2 is independently biased PECVD in an ECR (Machida and Oikawa, 1986; Denison et al., 1989), induction-coupled (van den Hoeck and Mountsier, 1994), or helicon (Nishimoto et al., 1995) reactor, all of which produce similar results. Deposition and etching occur simultaneously. In these systems, SiH_4 has been used almost universally as the source gas, despite the superior step coverage of TEOS-based oxides. As discussed in Chapter 1, despite the high ratio of ion to neutral species and the low operating pressure minimizing collisions, bias is necessary to ensure gap fill. If the bias is too low, the oxide at the top corner of the gap grows faster than sputtering can remove it so that the gap is closed at the top, leaving a void (Patrick, 1991; van den Hoek and Mountsier, 1994; Nishimoto et al., 1995).

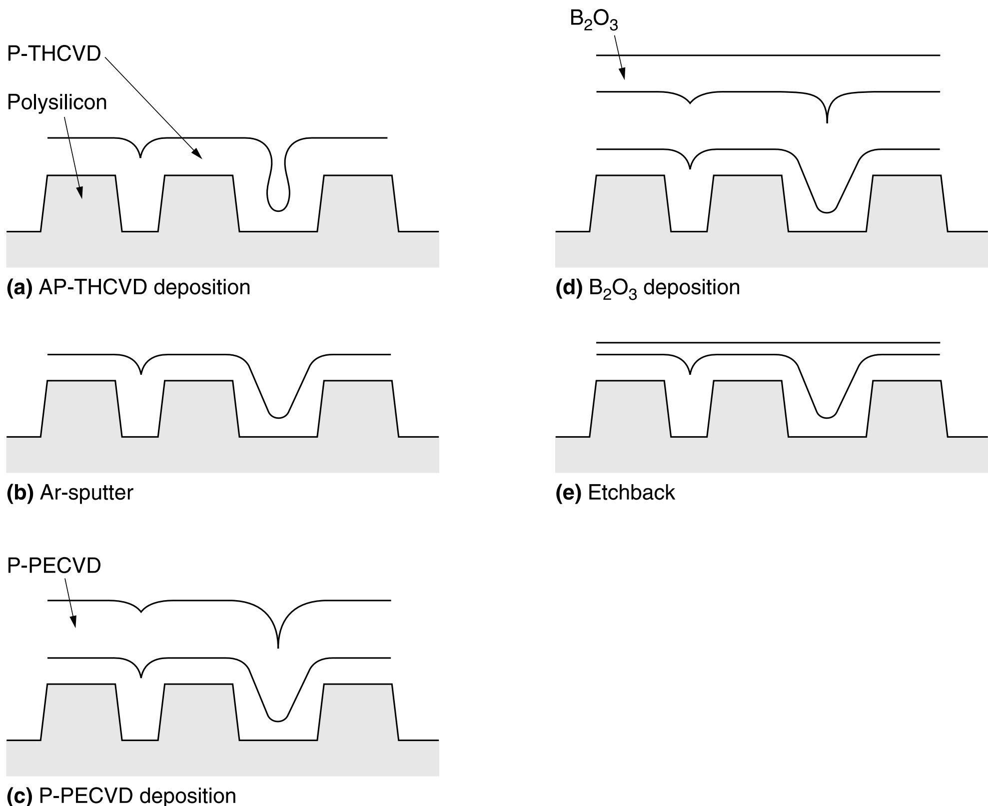

Figure 6.7 *In situ* gap fill and planarization using sacrificial B_2O_3 with P-doped thermal CVD and PECVD oxide films. (Reprinted from Pennington, S., and D. Hallock, *1990* VMIC, 71, 1990. With permission.)

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However, if the bias is too high, the corners of the metal become faceted (Tisier et al., 1991). As the AR of the gap increases, the process window becomes smaller.

The simulations for gap-fill and planarization of bias-ECR describe the other bias high-density PECVD processes as well.

Labun (1994) modeled the process as simultaneous PECVD (D) and sputter etching (E). In the simulation, the ratio E/D and the sticking coefficient sc were varied. High values of E/D, which result in low values of sc, improved gap-fill and planarization. The simulation of Lassig et al. (1995) was more complex. The components of the process, treated independently, are (1) a small LPCVD (low-pressure CVD) component, independent of ion bombardment, (2) IID (directional ion-induced deposition), the dominant component whose directionality is a result of high applied bias which narrows the angular distribution of the incoming ions, (3) angle-dependent sputter etching which prevents void formation by faceting the oxide at the top of the gap so that gaps fill from the bottom to the top, (4) direct line-of-sight-redeposition of sputtered material from the bottom of the gap to the sidewalls (~10 to 15%) which increases with bias and is responsible for the ability to fill a gap with an overhang or with a re-entrant sidewall, and (5) deposition of sputtered material backscattered from the gas phase (a negligible contribution). The simulation replicated the experimental results in which the evolution of the profile was delineated by periodic deposition of thin Si-rich oxide layers which were made visible by BHF etching.

It is possible to planarize small features by continued deposition at high bias but, as in the case of bias sputtering, it is an inefficient planarization technique.

6.6 ETCH-BACK PROCESSES*

Although many such processes (with and without sacrificial overcoats of various kinds) were developed they were discarded as better planarization techniques were developed.

6.7 STEP COVERAGE, HOLE-FILL PLANARIZATION OF METALS

When devices were large and packing density low, the only issue related to topography was the coverage, by the metal, of the steps in the insulator. Good step coverage prevented open circuit failure and early wear-out. But as devices became smaller and packing density greater, not only was there a need for improved step coverage but, beyond that, there was the need to fill small holes (contacts and vias). In addition, planarization during deposition, to simplify processing, became another goal.

The early work, using evaporation, is covered first, followed by the use of sputtering in a variety of configurations, beam techniques, CVD, flowage, and, finally, the first embedment methods.

6.8 EVAPORATION

Evaporation was used almost exclusively for metal deposition in the early years of device fabrication. As is the case for all deposited films, shadowing leads to poor step coverage with thinning or, in the worst case, cracks in the film in the inside corner, although crack-free deposits can be obtained by using elevated substrate temperature ($>300°C$). Another effect of shadowing is reduced density of the sidewall deposit. Blech's model of evaporation (1970) showed that step coverage is sensitive to the radius of curvature of the step (as shown in Figure 6.8) as well as AR and sidewall angle. A small radius results in a crack at the bottom corner but if the top is rounded the crack is not as deep. Increasing the radius of curvature improves the coverage.

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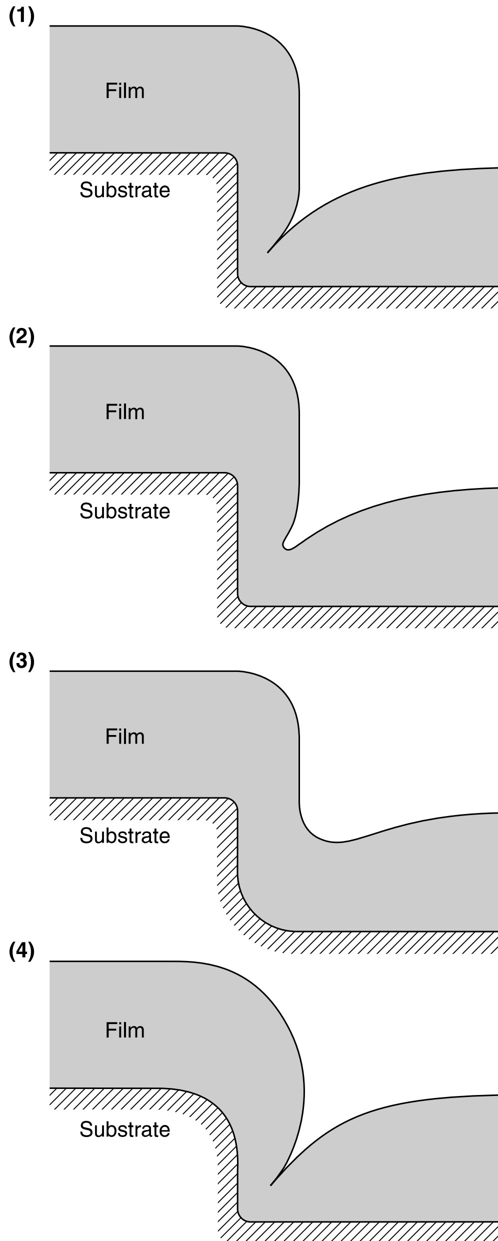

Figure 6.8 Simulated profiles of metal films evaporated over a step: (1) sharp step; (2), (3) increasing curvature at both bottom and top of step; (4) rounded at top but sharp at bottom. (Reprinted from Blech, I.A. *Thin Solid Films*, 6, 113, 1970. With permission. Copyright 1970, Elsevier.)

Step coverage is also dependent on the configuration of the evaporator. The geometry of the source was characterized as the ratio (source (target) to substrate distance)/(source diameter), called TAR by Bader et al. (1987) (illustrated in Figure 6.9a, which also shows the effect of TAR on the angle of incidence of the depositing species). The influence of TAR on profile evolution is shown in Figure 6.9b.

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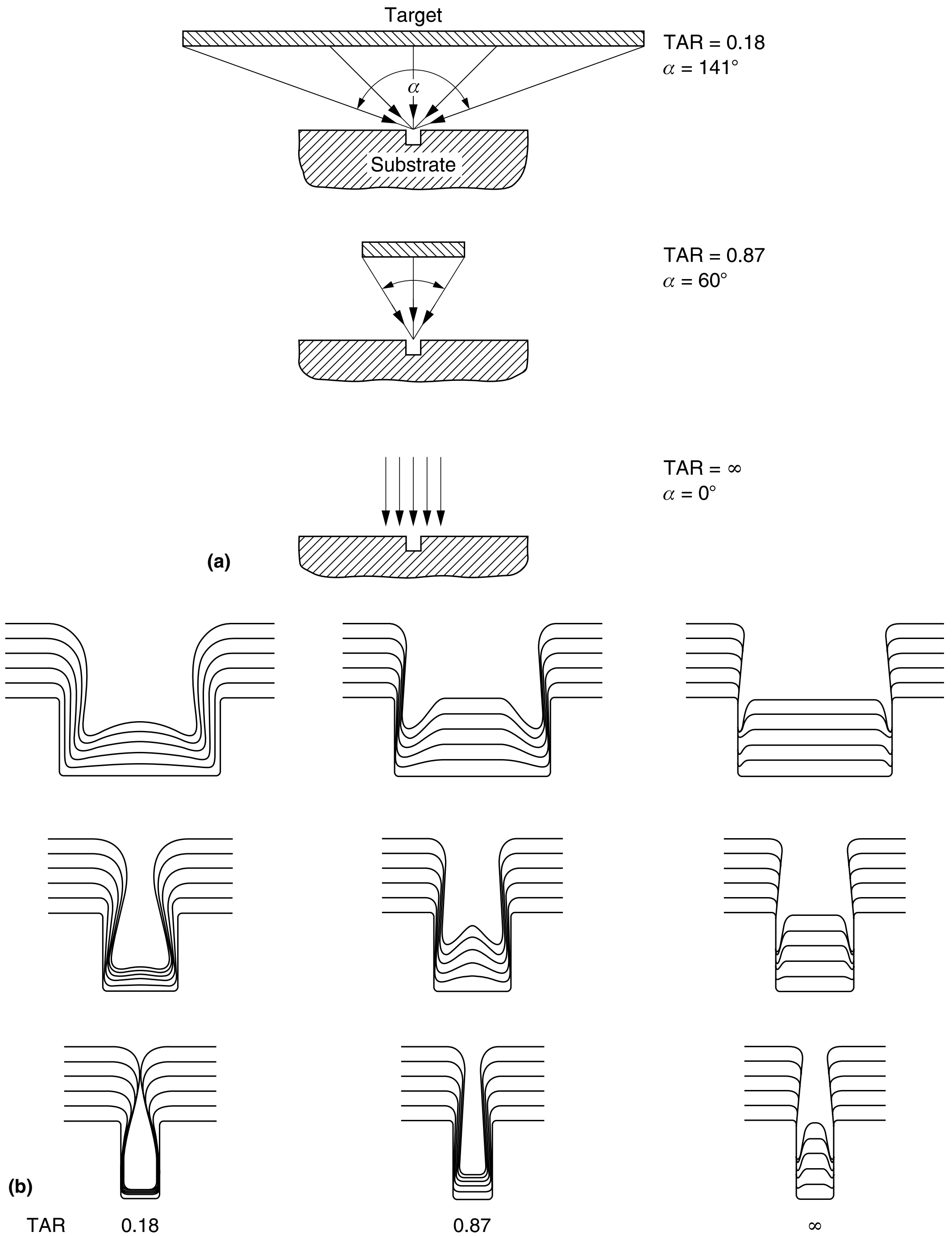

Figure 6.9 (a) Effect of target aspect ratio (TAR), the ratio of the distance of the substrate from the target (source) to the diameter of the target, on α, the angle of incidence with respect to the normal of the surface of the depositing species. (b) Simulation of the influence of TAR on profile evolution during evaporation into grooves with aspect ratios of (top to bottom) 0.5, 1.0, 2.0. (Reproduced from Bader, H.P., H.A. Lardom, and K.J. Hoefler, in *Multilevel Metallization, Interconnection and Contact Technologies,* L.B. Rothman and T. Herndon, Eds., *Electrochem. Soc. Proc.*, PV-87-4, 185, 1985. With permission of the Electrochemical Society, Inc.)

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Tait et al. (1990) simulated evaporation using a ballistic deposition model. Decreased density of the deposit and columnar microstructure were predicted and observed when the surface of the substrate was tilted away from the normal direction, as occurs when there is a step in the substrate.

6.8.1 Elevated Temperature

The reduction of dimensions, requiring more accurate pattern transfer, as well as the trend toward multilevel structures emphasizes the need for planarity. The use of high temperature (~450°C) to provide mobility to the incoming atoms had only limited success. The sensitivity to temperature of many of the low-ε films also restricts its use.

6.8.2 Evaporation/Sputter Etch Cycles

The step coverage of evaporated films can be improved by using alternate cycles of deposition and sputter etching (Lardon et al., 1986; Bader and Lardon, 1986; Bader et al., 1987). A simulation of the effect of sputtering on step coverage is shown in Figure 6.10. The processes cannot be done simultaneously; evaporation is a high-vacuum process (~2×10^{-3} Pa) whereas sputter etching requires a pressure of ~0.5 Pa. Evaporation using a directional source is required for filling and sputter etching for redistribution (discussed more fully below) to improve sidewall coverage. The effectiveness of the process is improved by increasing the number of cycles. The procedure is a slow one and there is a limit to the hole-filling capabilities.

6.9 SPUTTER DEPOSITION OF METALS

Sputtering in a capacitively coupled RF plasma system eventually replaced evaporation almost completely, both for control of the composition of alloys and the ability to apply substrate bias during deposition, rather than cyclically, as discussed above.

A sputtering target is an extended source; the pressure is higher during sputtering than in evaporation so that there is more scattering. Therefore the step coverage will resemble that obtained in low TAR evaporation unless bias is applied to the substrate.

6.9.1 Bias Sputtering

In bias sputtering, material deposited at the bottom of the step is resputtered at small angles, redepositing on the sidewalls (Vossen, 1971; Vossen et al., 1974). Material is deposited on the

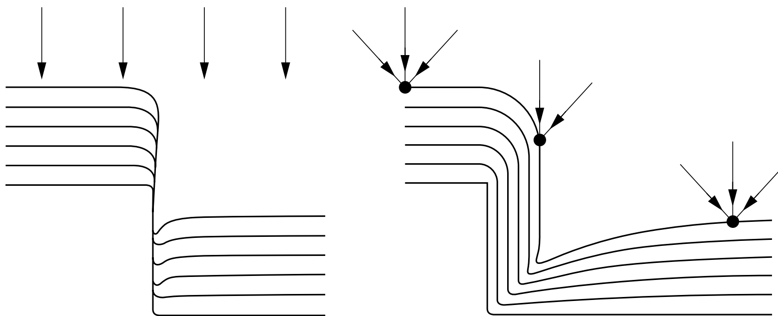

Figure 6.10 Simulation of step coverage. Left: evaporation; right: sputtering. (Reprinted from Lardon, M.A., H.P. Bader, and K.J. Hoefler, 1986 VMIC, 212, 1986. With permission)

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walls, instead of being sputtered away, because, when the incident ion energy is low (as it is when the substrate is biased), the angular distribution of the sputtered material is under-cosine (Chapman, 1980; Morgan, 1989), i.e., the material is directed more to the side than perpendicular to the surface, as illustrated in Figure 6.11. Since sputter etching of the sidewalls is negligible (ion impingement near the glancing angle), the material stays on the walls. As Vossen has pointed out, the arrival rate of material cannot be too high to ensure that the resputtering keeps pace with it. Substrate heating, due to ion bombardment (or an external heat source), enhances the effect of the ion-induced redistribution.

6.9.2 Simulations of Bias Sputtering

The simulation of step coverage/hole fill by Bader and Lardon (1985) showed that substrate bias improves the step coverage; adding redeposition results in planarity. Since at lower energies the stable facet angle is shallower, faster planarization occurs at low energy. They also showed that, although planarization (which is better at high AR than at low) is superior at low energy, the onset of void formation occurs at higher AR at the higher energy. The simulations agreed with experimental observations where the comparison could be made (Bader and Lardon, 1986).

Smy et al. (1990) and Dew et al. (1991) used a ballistic deposition model (SIMBAD) to predict step coverage and the structure of films deposited over topographical features. The model includes film resputtering, redeposition, ion reflection, and ion-induced diffusion. The angular dependence of the sputter yield, the ion reflection probability, the distribution of resputtered material, and the angular distribution of material arriving at the substrate from the target are all parameters included for the detailed simulation.

The simulations showed columnar microstructure (independent of ion bombardment), improved sidewall coverage with bias, and a decrease of the film density as the wall angle increased. They also showed (for W) the improvement of step coverage (approximately doubling the sidewall coverage) and surface planarity with increasing bias. It should be noted that as bias was applied, the net accumulation rate decreased, indicating the importance of resputtering.

As the AR of the hole was increased, the substrate was sputter etched.

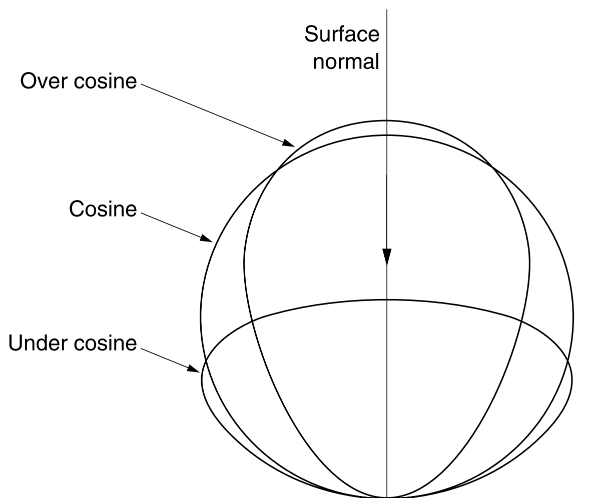

Figure 6.11 Possible angular distributions of sputtered material. (From Chapman, B. *Glow Discharge Processes*, Wiley, 1980. With permission. Copyright 1980, John Wiley and Sons, Inc.)

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6.9.3 Explanations (Models) of Bias Sputtering

There are many examples of improvement of step coverage, hole-fill, and planarization using bias sputtering, although, most often, not for the most aggressive dimensions. And there are several explanations (models) to account for the results.

6.9.3.1 Resputtering

The first is resputtering, but the issue is whether the bias should be low or high. Homma and Tsunekawa (1985), Mogami et al. (1985), and Lin (1988) all emphasized the use of high bias. The role of resputtering in hole-fill and subsequent planarization is seen in the SEM images of Figure 6.12 for AR = 1.The net accumulation rate decreased with increasing substrate bias, indicating resputtering was the operative mechanism. Any effect of increased temperature was discounted. Mogami et al. (1985) pointed out that when the bias was too high, regions in the underlying material were etched and subsequently filled with metal.

6.9.3.2 Low Bias

Homma and co-workers (1993), in contrast to their earlier work and the model of Bader, stated that a low bias was required for good fill (invoking under-cosine redeposition) since at high energies the angular distribution was over-cosine so that there was outward ejection of the resputtered particles.

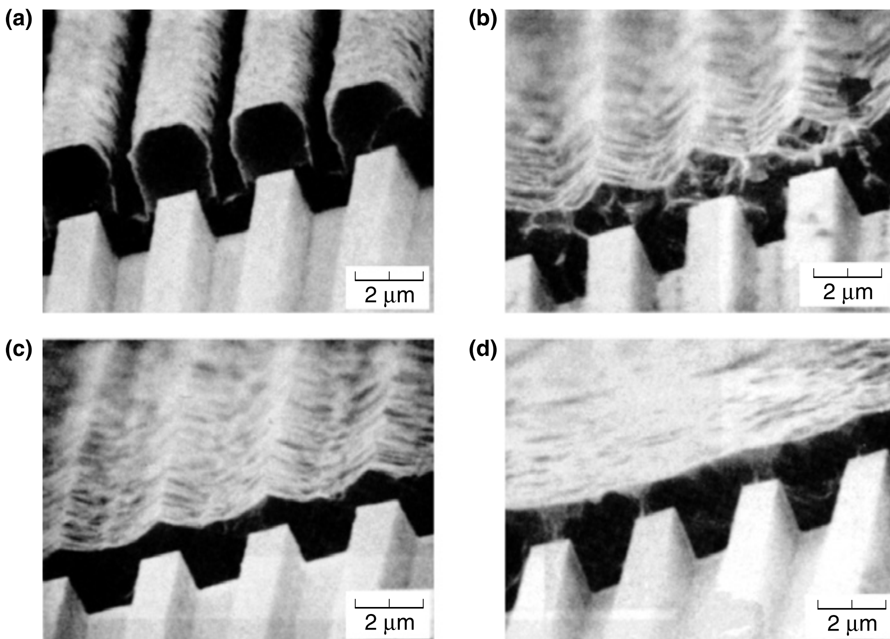

Figure 6.12 SEM images showing the effect of resputtering on step coverage of Al films deposited over grooves of aspect ratio ~1: (a) 0%, (b) 40%, (c) 50%, (d) 70% resputtering. (Reproduced from Homma, Y. and S. Tsunekawa, *J. Electrochem. Soc.*,132, 1466, 1985. With permission of the Electrochemical Society, Inc.)

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6.9.3.3 Enhanced Mobility

Other models discount resputtering because substrate biasing did not reduce the deposition rate. Smith et al. (1982) and Smith (1984) attributed the improvement in step coverage to ion bombardment-enhanced surface mobility (diffusion), or redistribution of material (Park et al., 1985). Forward scattering of surface atoms at the edge of the step by the incoming ions was proposed by Skelly and Gruenke (1986) who also stated that the effect of temperature could not be clearly separated. Demary et al. (1987) stated that, in a high growth-rate process, the primary role of bias is to provide effective rapid coupling of a front-side heat source to the film growth process to enhance mass transport.

6.9.3.4 High-Temperature Bias Sputtering

6.9.3.4.1 Introduction

High-temperature bias sputtering, i.e., the use of substrate heat (from an external source) in addition to bias, improves the results. In most cases, the high-temperature sputtering of the conductor metal is preceded by the lower temperature deposition of a thin underlay; this may be the conductor metal itself (Park et al., 1991; Talieh et al., 1993) or a film (e.g., Ti, TiW, Ti/TiN), which acts as a barrier against junction penetration and/or as a liner to improve wetting/flow (Gupta et al, 1987; Lin et al., 1988; Hariu et al., 1989; Chiang et al., 1994). Nishimura et al. (1995) found that filling vias with AlCuSi by sputtering at high temperature depended on the thickness of the underlying Ti layer. They postulated that the wettability of the metal film on the sidewall was affected by the uniformity of the reaction between the Ti underlayer and the AlCuSi film.

Collimated sputtering is sometimes used to deposit this thin layer (Talieh et al., 1993; Xu et al., 1994). The sample is transferred between deposition chambers without a break in vacuum; multi-chamber (cluster tool) systems (Chapter 1) are now usually used for this integrated processing.

The wafer temperature during high-temperature sputtering has ranged from ~400 to ~550ºC (Ono et al., 1990; Park et al., 1991; Nishimura et al., 1992; Xu, 1994). Taguchi et al. (1992) reported that diffusion of oxygen from the sidewalls of the via through the PSG ILD onto the surface of the Ti underlayer impeded the flow of AlSi sputtered at 500°C; SiN coating of the via walls acted as a diffusion barrier and improved the fill.

6.9.3.4.2 Mechanisms

Several mechanisms have been proposed to account for the improvement due to increased substrate temperature. Hoffman et al. (1987) concluded that thermally enhanced surface self-diffusion explains the results, eliminating viscous flow (temperature too low), evaporation/recondensation (vapor pressure too low), and volume diffusion (only insignificant contribution). Kamoshida and Nakamura (1987) demonstrated that planarization appeared to occur in Al films by plastic deformation. Since the temperatures are too low for plastic deformation, they invoke a decreased deformation resistance, a result of enhanced vacancy generation due to ion bombardment. Smy et al. (1992, 1994) have simulated step coverage, film density, and gap fill. The use of bias reduces the minimum temperature needed for fill, and increased temperature enhances the effect of bias, increasing the range of adatom surface diffusion so that material is transported from the top of a film into a hole and bulk diffusion of vacancies out of the hole (Figure 6.13a). Figure 6.13b simulates the progression with time of hole fill on a hot substrate.

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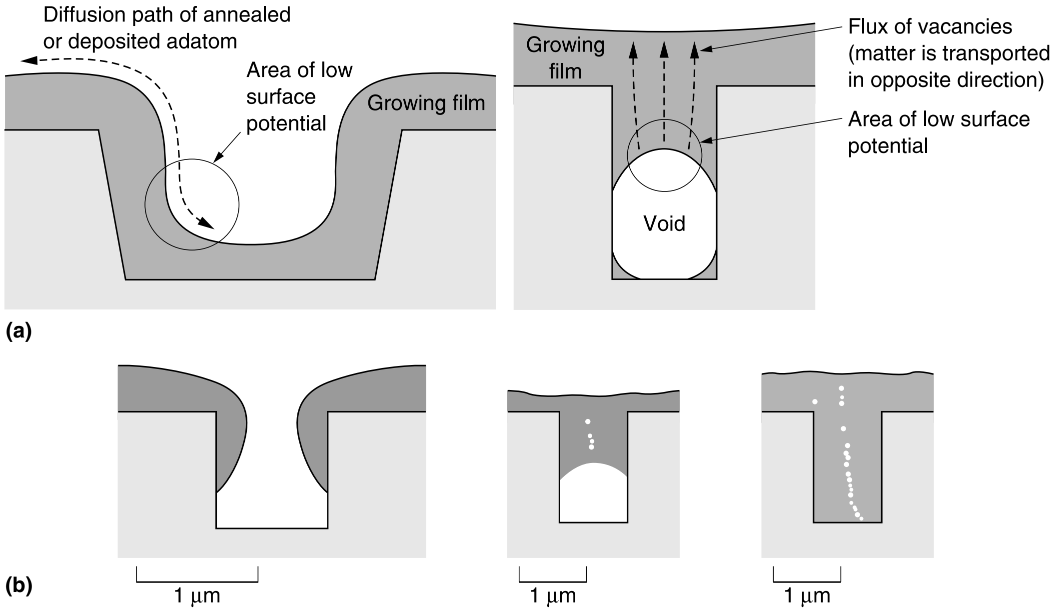

Figure 6.13 (a) Model of the effect of temperature on hole filling showing self-diffusion as a result of (left) surface diffusion and (right) bulk diffusion of vacancies. (b) Simulation of film growth on a hot substrate. Time increases from left to right. (Reprinted from Smy, T., S.K. Dew, M.J. Brett, W. Tsai, M. Biberger, K.C. Chen, and S.T. Hsai, 1994 VMIC, 371, 1994. With permission.)

6.9.4 Other Methods*

Among these were AlGe deposition, electron bias sputtering, selective sputtering, and sputtering using elevated temperature without substrate bias.

6.9.5 Concluding Remarks

Despite the improvements realized by the use of high temperature, usually with bias sputtering, its application may be limited because of incompatibility with the materials and performance of other components of the structure, e.g., low-ε interlevel dielectrics.

6.10 DIRECTIONAL SPUTTERING

Advances in hole filling using physical vapor deposition, beyond the capabilities of sputtering at elevated temperature, have been achieved by methods of directional sputtering.

6.10.1 Collimated Sputtering

The details of collimated sputtering are covered in Chapter 1.

Since the angular distribution of the impinging species is reduced, coverage of the bottom of a hole is increased significantly. This is due to the elimination of the off-normal particles which would lead to pinch-off at the top of the hole and to an increased flux at the bottom of the hole. However, the net accumulation rate is reduced, but, according to Bang et al. (1994), the deposition

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rate loss at the bottom of the hole is not as severe as measurements on a flat surface suggest. A natural consequence of directionality is a minimal, but more uniform, coverage of the sides of the hole; this prevents/delays closure at the top of a hole. As the fill proceeds, the microstructure of the film on the sidewalls becomes more columnar, but the fill is homogeneous if the substrate temperature is increased (200 to 300°C) or a low bias imposed.

The higher the aspect ratio of the collimator, the more directional the deposit. Liu et al. (1993), Dew et al. (1993), and Dew (1994) have compared experimental results with computer simulations of collimated sputtering over topographical features and concluded that the deposit on the sidewall is of lower density than that on the top surfaces, but the discontinuity at the bottom corners of a hole is reduced when a collimator is used. The thickness of the deposited film is not uniform; there are oscillations in the film thickness which correspond to the collimator pitch. Increased operating pressure would improve uniformity but the increased scattering would broaden the flux distribution, thus reducing the benefits of collimation. In addition, the holes in the collimator become plugged, reducing the deposition rate even further, so that collimator may eventually require cleaning or replacement.

6.10.2 Long Target-to-Substrate Sputtering

This method was described in Chapter 1 as an alternative to collimated sputtering (Turner et al., 1993; Broughten et al., 1995; Wagner, 1995). These system modifications result in a narrow angular distribution of the sputtered species and, as expected, the fill characteristics and reduction of net deposition rate are the same as those obtained with collimated sputtering. The longer the distance and the lower the pressure, the greater the coverage at the bottom of the feature (Kondo et al., 1997); coverage of trenches is greater than that of holes and coverage degrades as the AR of both kinds of features increases (Saito et al., 1997). For both collimated and long target-to-substrate (T/S) sputtering, deposition in holes at off-center positions is skewed (as seen in Figure 6.14) because the angular distribution of the flux is centered at a nonzero angle.

Another application of collimated or long T/S sputtering is the deposition of seed or liner layers at low temperature before filling a hole with the conductor metal. (Talieh et al., 1993; Broughton et al., 1995). The term “coherent sputtering” has been used for collimated sputtering (Xu et al., 1994). The directionality of the deposit makes this method suitable for lift-off patterning of a metal as well.

6.10.3 Hollow Cathode-Enhanced Sputtering*

Hollow cathode-enhanced magnetron sputtering has been suggested as another alternative to collimation but has not had commercial application.

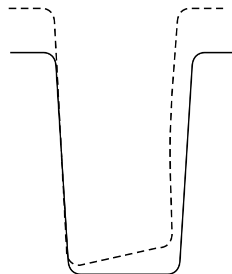

Figure 6.14 Asymmetrical deposition in a hole located away from the center of the substrate using long target-to-substrate (T/S) sputtering. (Reprinted from Wagner, I, 1995 VMIC, 226, 1995. With permission.)

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6.10.4 Self-Sputtering

Self-sputtering in a planar magnetron at very low pressures (<0.1 mtorr) (mentioned in Chapter 1) has also been suggested as a way of depositing thin films at the bottom of deep holes at high rates. Self-sputtering is the sputtering of metals using ions of the same element in the absence of an inert gas, eliminating diffusion of the sputtered atoms resulting in line-of-sight deposition. Self-sputtering can be initiated only when a critical plasma density is reached and the self-sputtering yield must be >1. Efficient ionization of the sputtered material must occur and the ions must be redirected to the target (Posadowski and Razzimski, 1993). Self-sputtering has been demonstrated for Cu and Ag, but not Al because of its low yield and negative effects of O_2 in the chamber. Asamaki et al. (1994) used the technique to deposit thin films of Cu and demonstrated that the thickness at the center of the bottom of a narrow deep trench is the same as that on the top surface. The deposition rate is high, making possible large T/S distances. However, the target lifetime is limited, even with improved target design so that the usefulness of the technique in production is questionable.

6.11 HIGH-DENSITY PLASMAS

6.11.1 Introduction

High-density plasmas were developed to overcome the limited capability of the RF sputtering systems, discussed above, to fill high-AR holes.

6.11.2 ECR

An ECR plasma reactor was used to fill high-AR holes with Cu using an evaporated source (Holber et al., 1993). The system configuration was somewhat different from the commercially available reactors described in Chapter 1.

The essential features are: the quartz window through which the microwaves enter the plasma region is out of line-of-sight of the plasma to prevent coating of the window and the substrate is out of line-of-sight of the resistively-heated Cu source. The evaporated Cu atoms are ionized in the ECR source; the flux at the substrate may be ~100% ionized (although this high degree of ionization may not be needed) and no buffer or carrier gas is used. The substrate temperature is controlled by the use of a helium-backed electrostatic chuck which can be biased by an RF or DC supply. The substrate temperature (which was usually ~150°C) appears to have no effect on the filling capability although it may affect the microstructure of the film.

The most important deposition parameter determining whether a hole of a given AR can be filled is the resputtering rate at the surface. If the substrate bias is too low, voids are formed; if too high, the net accumulation of Cu on the top surface is very small. The best results were obtained using a high/low bias process in which a hole of AR ~ 4.2 (depth ~ 3 μm) was filled solidly.

This system can also be used to line high-AR features conformally with a thin film. Hole filling with Al, in a conventional ECR system using a sputtering target, and a moderately high substrate temperature of 300°C (to assist by a flow effect) appeared to be equally feasible (Ono et al., 1994).

6.11.3 Inductive Plasma: Ionized Metal Plasma (IMP) Deposition

This technique, now used widely, is magnetron sputter deposition combined with an RFI plasma to produce high levels of metal ionization (Rossnagel and Hopwood, 1993; Cheng, et al., 1995; Hamaguchi and Rossnagel, 1995). The essentials of the reactor are discussed in Chapter 1. In the absence of the additional ionizing plasma, the system is, of course, a conventional sputtering

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system incapable of filling high-AR trenches/holes without voids. The advantages cited are: (1) the use of a sputtering target instead of an evaporation source (more compatible with alloy deposition) and (2) an RFI system is simpler than an ECR system (as seen in Chapter 1). A large fraction of the sputtered atoms is ionized in the RFI plasma and accelerated across the sheath of the negatively biased sample holder to be deposited at normal incidence. In addition to the vertical energetic ion flux is the neutral flux which has a large angular distribution. Both fluxes contribute to the deposit. The thickness of the deposited film is influenced by the sticking probability of the incoming species and on the sputtering yield since the energetic ions remove some of the deposit by sputtering. Sputtering also bevels the corners of the features. The material resputtered from the top surface is returned directly to the plasma but that from the bevel may either leave the feature or be incorporated into the sidewalls. Bevel formation has two opposing effects: (1) reduction (possibly elimination) of overhang formation, increasing the acceptance angle of the arriving particles and (2) formation of a lateral buildup, by material sputtered from the bevel, which shadows the trench, resulting in void formation.

Directional deposition results in good coverage of the bottom of a hole with a dense film but on the sidewalls there is a low-density, columnar deposit because of the grazing incidence of the incoming particles. Figure 6.15a shows the growth of a Cu film. As the substrate bias is increased, increased reflection and sputtering help fill the corners and deposit film on the sidewalls; elevated substrate temperature (~250°C) also helps to fill the corners.

Under the proper conditions a trench can be filled completely as was demonstrated for dual damascene structures using both AlCu and Cu.

Increasing the RF power increased the relative ionization of the sputtered atoms, increasing the deposition rate, directionality, and bevel angle. Increasing the Ar pressure decreased the overhang

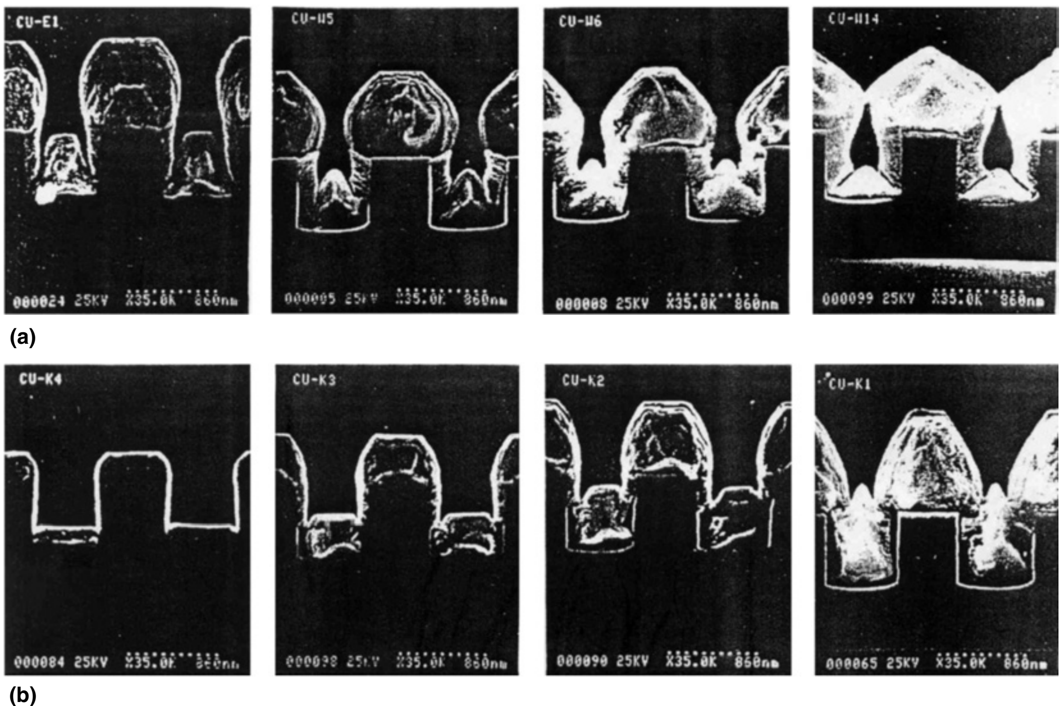

Figure 6.15 (a) SEM images showing time evolution (time increases from left to right) of films deposited in an IMP reactor. (b) SEM images showing effect of substrate bias (bias increases from left to right) on films deposited in an IMP reactor. (Reprinted from Cheng, P.F., S.M. Rossnagel, and D.N. Ruzic, *J. Vac. Sci. Technol.*, B13, 203, 1995. With permission.)

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thus improving the fill. A decrease in magnetron power lowers the density of sputtered particles in the plasma, increasing the relative ionization and hence results in more directional sputtering.

The mechanisms for highly ionized magnetron sputtering have been discussed by Hopwood and Qian (1995).

6.12 BEAM TECHNIQUES*

Beams of various kinds have been reported in the literature but they have not been used in large-scale wafer fabrication.

Several kinds of ionized beams have been described: (1) ionized cluster beams (ICBs, also called nozzle jet beams), (2) partially ionized beams (PIBs), and (3) energetic cluster impact beams (ECIs).

Neutral beam molecular beam deposition (MBD) plus annealing has also been described.

6.13 FLOWAGE OF METAL FILMS

Postdeposition heat treatment is still another way of filling via holes in the interlevel dielectric layer and of planarizing the surface. There have been two approaches: laser reflow and thermal annealing (1) in the deposition system, (2) in a furnace, (3) using a rapid thermal processor, and (4) by the use of high pressure in addition to heat.

6.13.1 Laser Reflow*

Flashlamp-pumped dye lasers and pulsed excimer lasers of shorter wavelength have been used for this purpose but this technique has generally been abandoned.

6.13.2 Thermal Annealing*

Thermal annealing has been used successfully for Al(alloy)/SiO_2 structures, using RTP, heating in high vacuum (at $> 500°C$), or with the use of high pressure (FORCEFILL™) to reduce the required temperature to ~430°C.

Flowage of Cu deposited into deep Ta-lined SiO_2/SiN trenches was described by Gardner and Fraser (1995) and simulated by Friedrich et al. (1997).

Advances in void-/seam-free Cu electrodeposition for filling high-AR features (followed by CMP) probably makes postdeposition flow unnecessary. If incomplete filling does occur, the use of low-ε interlevel dielectrics requires a relatively low flow temperature; this increases the flow time. Even if the mechanism of flow is the one with the lowest E_{act} (~0.8 eV), i.e., surface diffusion which requires a continuous path, decreasing the temperature from 450°C (used for flowage in SiO_2 trenches, e.g., Kondo et al., 1997) to 350°C, filling requires more than an order of magnitude increase in the flow time. This makes the process impractical for chip manufacturing.

A short (or possibly a low-temperature) anneal might be useful for improving the bottom coverage after directional sputtering as suggested by Saito et al. (1997).

6.13.3 Modification of Underlay*

Underlayers have been modified in various ways to improve their wetting characteristics for both Al and Cu deposition.

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6.14 CVD METALS

One of the attractive features of this method of deposition is its superior step coverage and hole-fill capability. The principles of CVD are covered in Chapter 1 and the specifics in Chapter 5.

6.14.1 CVD of W

6.14.1.1 Introduction

CVD W has been studied more extensively and is used more widely than the other CVD metals. The first widespread use of CVD W was as a contact plug (to planarize the substrate, after completion of the processes of fabricating and passivating the active and passive devices in the substrate) before the first metallization layer was deposited. The next application was as a vertical interconnection between successive wiring levels in a multilevel structure.

6.14.1.2 Selective CVD

Selective deposition of W is discussed in Chapter 5; it is intrinsically a hole-filling technique, and is not discussed further in this section.

6.14.1.3 Blanket CVD

Blanket CVD W films can be deposited with 100% step coverage, filling holes without void formation, when the reaction of $WF_6 + H_2$ is carried out under optimal conditions. The higher the AR of the hole, the more difficult it is to get good step coverage; step coverage is higher in trenches than in holes of the same dimensions. Although there are no voids, seams that are more vulnerable to etchants than the bulk W, may exist. All the experimental observations, both LPCVD (e.g., McConica and Churchill, 1988; Chatterjee and McConica, 1990; Schmitz and Hasper, 1993) and HPCVD, i.e., 80 torr vs. 0.5 to 10 torr (Clark et al., 1991), showed that optimization of the deposition conditions for plug applications included lowering the temperature and the partial pressure of H_2 and raising that of WF_6. It was also found that reducing the spacing between the gas inlet (showerhead) and the wafer (i.e., reducing the reactor volume) also improved step coverage.

Blumenthal and Smith (1988) examined, in detail, the effect of temperature on step coverage. In the higher temperature (higher deposition rate) regime in which the reaction rate is controlled by mass transport and therefore nonactivated, the step coverage was nonconformal and depended strongly on the size of the groove. In the lower temperature range, the surface reaction-controlled region (activated), 100% step coverage could be attained for grooves larger than 1 μm.

Schmitz and Hasper (1993) emphasized that when the step coverage is less than 100%, the existence of a void (and its size) has a greater impact on etchback complications and reliability than does the value of the step coverage, i.e., the ratio of film thickness at the top of the hole to that at the bottom.

When SiH_4 was used to reduce WF_6, to increase the deposition rate in a cold-wall LPCVD reactor, sizeable voids were formed (Schmitz et al., 1987, 1988; Lee et al., 1989); H_2 reduction, in the same reactor, did produce void-free fill. Better hole-fill was obtained when SiH_2F_2 was used instead of SiH_4, but H_2 reduction resulted in the best fill (Goto et al., 1991).

Adding H_2 to a SiH_4/WF_6 mixture (under conditions of equal growth rate) degraded the step coverage dramatically (Schmitz et al., 1988) although a two-step process, in which the initial reduction with SiH_4 was followed by H_2, resulted in void-free fill (Lee et al., 1989).

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6.14.1.3.1 Step-Coverage/Hole-Fill Models

A model was developed by McConica and Churchill (1988) for predicting the step coverage during blanket CVD W deposition by the WF_6/H_2 reaction. When diffusion and reaction occur simultaneously in a deep hole, concentration gradients of the reactant species are established along the length of the pore. This occurs because in LPCVD processes, transport in small holes is dominated by Knudsen diffusion which is slower than bulk diffusion. This limited transport, combined with the decrease in the radius of the pore as deposition proceeds, restricts access of the reactant. The deposition rate at any location in the hole is dominated by the local reactant concentration but the concentration gradient within the hole does not itself result in a thickness gradient. The nonuniform step coverage results from a limiting W thickness which results when the WF_6 concentration reaches zero and all growth stops. The time growth stops is a function of the hole characteristics, the reaction rate, and the mass of the diffusing species. The predictions of the model agree with the experimental results described above. McConica and Churchill (1988) pointed out that, although the reaction rate is zero order in WF_6 (the diffusion limited species), the step coverage is not.

Schmitz and Hasper (1993) simulated the hole-filling process, basing it, as did McConica and Churchill (1988), on the balance between diffusion and consumption of reactants. They found that the size of the void depended on the length of the hole but not its radius, i.e., not on AR. Thus the attempt to decrease capacitance by increasing the thickness of dielectric films through which vias must be etched and then filled, will exacerbate void formation. They also found that when the AR of the hole was less than one, including the surface curvature of the film at the top of the hole improves the calculated step coverage but had a negligible effect when AR is larger.

Hsieh (1993) modeled conformality using a two-parameter analytical mass balance method to couple molecular scattering and a two-step surface-activated reaction. The reaction consisted of the adsorption of the precursor molecule on the surface followed by the reaction of the sorbed species on the surface. The two parameters used in the simulations are the intrinsic sticking coefficient of the precursor, determined by the nature of the precursor species, and the degree of surface saturation, which is process-dependent. The sticking coefficient, if small, reduces the influence of geometric shadowing. However, the value of the sticking coefficient was determined experimentally as 0.48 (Yu et al., 1989) so that the only adjustable parameter is the saturation factor. Step coverage increased as this factor was increased. In practice, this means increasing the surface flux or decreasing the reaction rate, in agreement with experimental results.

However, it has been possible to simulate the step coverage/gap fill of CVD W and obtain results agreeing with the observed profiles by assuming a sticking coefficient close to zero (Rey et al., 1991; Hsieh, 1993). Thus, the agreement between a simulation and experimental results does not guarantee the correctness of the model.

The poor step coverage observed when W was deposited by the $WF_6 + SiH_4$ reaction was explained by the fact that although the reaction rate was increased, the diffusion rate was unchanged, resulting in depletion of WF_6. The reaction rate is first order in SiH_4. This implies worse step coverage than a reaction of lower order: the reduction of WF_6 by H_2 is half-order in H_2. Finally, since SiH_4 is a bigger molecule than H_2, its transport into and within the hole is inhibited (Chatterjee and McConica, 1990; Hasper et al., 1991).

6.14.1.3.2 Etchback

When blanket W is used to fill contact/via holes, the excess metal must be removed. In this section, etchback processes are discussed; CMP is discussed later.

Many processes using F-based etchants (NF_3, but more usually SF_6) have been proposed. One of the earliest was simply to RIE the blanket film using an isotropic etchant at high pressure to increase the etch rate of W with respect to the underlying oxide surface. The etchant attacked the

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seam in the via leaving a wide gap but the sides of the vias are now sloped so that they are easily covered by the next conductor layer (Smith, 1985). By reducing the loading effect, the amount of W remaining after etch was maximized. A number of processes have been proposed; they involve, for example, the use of different etchants or multiple steps (Lee and Hartman, 1987), precision determination of the endpoint (Clark et al., 1990), different etchers, e.g., magnetron (Clark et al., 1990; Berthold and Wiecorek, 1989), triode (van Laarhoven et al., 1989), and transformer coupled reactor (Allen, 1993), use of a clamp ring (Wilson et al., 1992) or an electrostatic wafer clamp (Marx at al., 1994), and coating the oxide with nitride (van Laarhoven et al., 1989). Nowicki (1994) patented the use of a sacrificial ring whose etch rate equaled that of metal in the vias and thus avoided microloading.

A sacrificial layer was used in an etchback process to improve uniformity, to ensure that no plug was submerged, but severe microloading was observed. By using a consumable cathode (i.e., carbon) and a CCl_2F_2/O_2 mixture, the uniformity was improved further and there was minimal microloading. The equality of etch rates (resist/W) was maintained by adjusting the pressure (Saia et al., 1988).

Mihara and Nakamura (1994) studied the effect of wafer temperature on loss of W in the plug during RIE etchback in SF_6/N_2 of W on a TiN adhesion layer. Reduced wafer temperature during overetch suppressed the loss of W because of the formation and subsequent deposition on the W surface of TiF_x sputtered from the exposed TiN.

Etchback may also be required when the W is deposited selectively. Small protrusions above the vias may be formed because of different via depths or inadequate process control during deposition. However, this presents fewer difficulties than etchback of blanket W. The loading effects are minimized because the area of W is very much smaller than that of the dielectric layer. Saia et al. (1987) used a sacrificial layer which compensated for the nonuniform W thickness.

6.14.2 CVD Aluminum, Aluminum–Copper, and Copper

6.14.2.1 Introduction

The principles of CVD are covered in Chapter 1 and the specifics in Chapter 5. Aluminum and its alloys, and more recently copper, films are used for interconnection metallization. Therefore, the use of such metals, prepared by CVD, would not be expected to be restricted to hole filling, as is the case for W with its much higher resistivity. Their use as plugs has the advantage over W of reduced interlevel resistance. Both blanket and selective deposition have been reported.

6.14.2.2 Selective Deposition

Selective deposition is, as already noted, intrinsically a hole-filling process. For example, Ohta et al. (1994) were able to demonstrate, by taking SEM images at various times during the deposition process, that CVD Al grew from the lower Al surface, filling the vias, when the lower surface was cleaned of its native oxide (by etching in a BCl_3 plasma).

After plug formation, the next interconnection level has been fabricated by etching the same metal formed by blanket PVD or CVD processes so that the surface is no longer planar. For example, Amazawa et al. (1988), Ohta et al. (1994), and Takeyasu et al. (1994) sputtered the interconnection Al; Tsubouchi et al. (1990) and Tsubouchi and Masu (1992) used the same process for both Al levels but insured blanket deposition of the second one by exposing the surface to an RF plasma after hole-fill.

After selective hole-fill by Cu, Awaya et al. (1990) used sputtered Cu which was patterned by RIE in $SiCl_4/N_2$ at 250°C; Kim et al. (1994) used blanket CVD Cu on a Ta seed layer.

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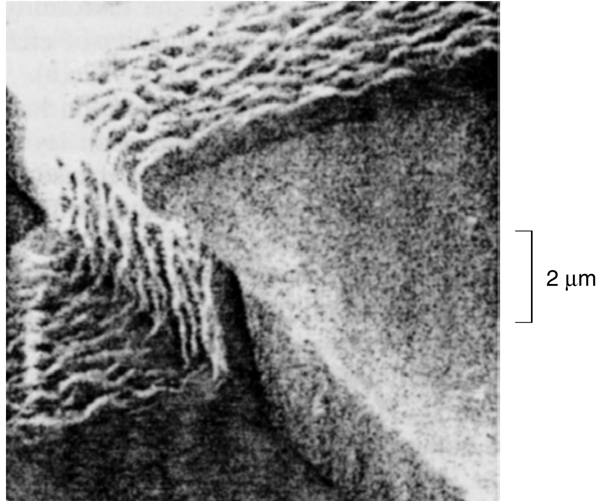

Figure 6.16 SEM image showing step coverage by CVD Al of a vertical step with an overhang. (Reprinted from Cooke, M.J., R.A. Heinecke, and R.C. Stern, *Solid State Technology*, 12/82, 62, 1982. With permission.)

To recover the planarity, one could envision a process in which the second metal pattern would be formed using a damascene CMP process (see below) after CVD deposition of the same metal into the stencil etched into the interlevel dielectric layer.

6.14.2.3 Coverage by Blanket CVD Films

The mechanism of step coverage by blanket films of these metals has not been studied extensively. The coating of an overhang structure and vertical wall by CVD Al, shown in Figure 6.16, is an indication of superior step coverage (Cooke et al., 1982). Sugai et al. (1993) used blanket CVD Al to fill via holes; sputtered AlCu was used for the interconnection metallization.

As mentioned in Chapter 5, blanket CVD Cu covered an overhang structure exceedingly well. The results were consistent with a very low sticking coefficient (~0.015). Figure 6.17 is an example of void-free filling by CVD Cu of high-AR trenches; the SEM image was taken after the excess metal on the surrounding insulator was removed (Cho et al., 1992). RIE, ion milling, or CMP can be used for this purpose. Gelatos et al. (1993) and Awaya and Arita (1993a,b) also reported excellent fill. Instead of removing the excess metal, additional Cu can be deposited by sputtering and the interconnect completed by RIE (Awaya, 1993) resulting in a nonplanar surface. Blanket CVD Cu has also been used both to fill the vias and form the planar interconnection using a dual damascene CMP process (Krishnan et al., 1992).

6.15 ELECTROCHEMICAL DEPOSITION OF COPPER

The principles of both electroless and electrochemical deposition are covered in Chapter 1 and Chapter 2 and the specifics in Chapter 5. Electroplating of Cu has become the method of choice for void-/ seam-free filling the high AR-vias and the trenches in the damascene process.

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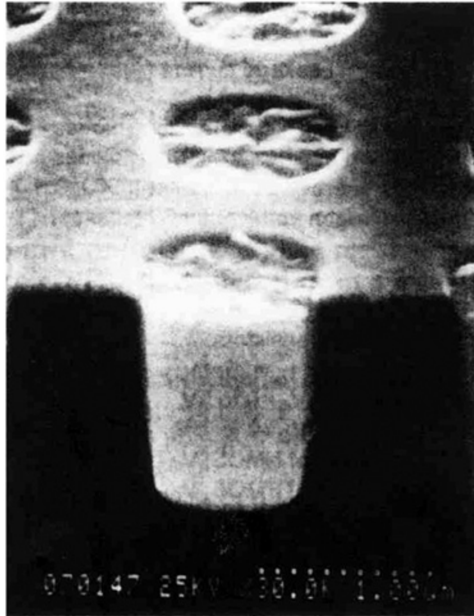

Figure 6.17 SEM image showing hole fill by CVD Cu after fill and removal of excess Cu. (From Cho, J.S.H., H.-K. Kang, and S.S. Wong, IEDM 92, 297, 1992. With permission. Copyright 2004, IEEE)

6.16 EMBEDMENT (INLAID) PROCESSES

6.16.1 Introduction

Except for the oxide lift-off process (Section 6.16.2.4), in these processes the metal is deposited into recesses etched into a permanent dielectric layer.

6.16.2 Early Processes

6.16.2.1 Metal Lift-Off

Metal was evaporated through a lift-off mask to fill holes etched in an oxide matrix. Since the metal does not fill the holes completely, SOG was used to fill the gaps before deposition of the interlevel dielectric (Sumitomo and Ohashi, 1978). In the same way, metal was deposited into recesses etched in a polyimide layer, but, in this case, the gaps were filled when the next polyimide layer (the interlevel dielectric) was spun-on (Rothman, 1983). The process was repeated for each vertical (plug) and horizontal (conductor) metal layer to build a planar four-level structure.

6.16.2.2 Sputtered Metal

Wu (1986, 1987) described a process for embedding sputtered metal in oxide, building layer by layer, a coplanar conductor/insulator composite for dense multilayer metallization. The process was called “PRAIRIE,” patterns recessed by anisotropic reactive ion etching.

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6.16.2.3 CVD Metal

Blanket CVD W was used to fill deep grooves in a dielectric layer to form thick films for the primary levels of interconnection in a multilevel structure. A thin metallic layer was first sputtered into the grooves to promote the adhesion of W. After deposition the W was etched back (in NF_3/O_2 using laser interferometry for endpoint detection) to expose the dielectric layer, thus producing a planar structure of W embedded in the insulator (Broadbent et al., 1988).

Processes called “reverse pillar” (Yeh et al., 1988) and self-aligned contact, SAC (Ueno et al., 1992), are etchback versions of the dual damascene CMP process. The interconnect patterns and then the contacts were etched into the dielectric layer and filled simultaneously with CVD (but not sputtered) metal; the excess metal is etched back, leaving the recessed metal. If blanket instead of selective CVD metal is used, the metal lines should be limited to a single minimum width; if wider lines are used, resist etchback is required (Yeh et al., 1988).

6.16.2.4 Oxide Lift-Off

A different approach to embedment is oxide lift-off. Ehara et al. (1984) formed the metal pattern by RIE, and leaving the resist mask in place, deposited the oxide in an ECR reactor. The oxide was etched briefly to expose the resist which could then be dissolved, lifting the oxide over the metal, leaving it embedded in the surrounding oxide. The subsequent interlevel dielectric filled the gaps in the lower oxide encapsulating the metal. Another version (Rothman et al., 1985) used sputtered oxide over an AlCu/Hf conductor, capped by MgO. The oxide was sputter etched to expose the edges of the MgO layer which was then dissolved, lifting the overlying oxide. The Hf layer protected the underlying conductor from attack during dissolution of the MgO.

6.16.2.5 Electroless Metal Fill

Because it is a selective process, electroless Cu film grows from the bottom of a properly activated hole. It is a good choice for filling high-AR vias without voids or seams. This capability has been demonstrated by Dubin et al. (1995) for 0.35 μm vias with an AR ~ 4. The Cu film penetrated beneath the oxide interlevel dielectric layer increasing the mechanical stability of the metallization system, but might cause shorting or reliability problems when vias are closely spaced. The deposition rate was a function of the via size; a smaller hole (higher AR) was filled more slowly than the larger one (lower AR). This same size dependence was observed when plating Ni(P) on Al (Schwartz and Platter, 1974). However, there was no barrier layer on the sides of the Cu plugs. If migration of Cu through the dielectric films must be avoided, this process is of questionable value.

Cho et al. (1993) described a process for building a structure in which selective electroless Cu was fully encapsulated (in TiW) and, they claimed, was planarized as well. Nitride spacers were required to protect the upper part of the sidewall exposed when the blanket TiW was etched from the top surfaces. The combination of spacer and barrier material restricted the conductor width so that the process is not suitable for submicrometer features. Also, the assumption that the level of the deposited Cu is the same in features of different sizes is questionable so that additional planarization, by some other method, would probably be required.

Another approach is the use of blanket electroless plating, after collimated sputtering of a liner, Ti/TiN, and a thin Cu seed layer. This process was used to fill 0.35 μm holes, AR ~ 3, without voids. Hole-filling capability depended on the thickness of the Cu seed layer; if it was too thin, the results were unacceptable (Shacham-Diamand et al., 1995). Removal of the excess Cu, planarizing the surface at the same time, would have to follow.

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6.16.3 Damascene Processing

The name damascene comes from an ancient inlay process used to make enamelware. It is the use of CMP to remove excess metal that distinguishes this process from some earlier embedment processes such as those described above.

In the process used for ULSI (1) a permanent dielectric film is deposited, (2) coated with a resist layer, (3) the interconnection metal pattern (the inverse of that used for the subtractive process) created by standard lithographic procedures, (4) the features etched into it by RIE, (5) the metal(s) deposited into the recesses, and finally (6) the excess metal removed by CMP. The metal pattern may be either the horizontal or vertical interconnection. In what is called the dual damascene (DD) process, they are formed concurrently (Kaanta et al., 1991), thus eliminating an interface, which forms and must be removed when the metals levels are deposited separately. Thus there are fewer process steps than in traditional planarized technology with vertical studs and reactive ion etched wiring levels as well as improved process-line logistics, i.e., process and equipment clustering. The need for etch/polish stops, however, adds to the complexity (and cost) of the interlevel dielectric deposition process.

Initially the dielectric layer was SiO_2 and the metals were W as a contact plug and Al-based metallization for the remainder of the interconnections. There were several choices for hole fill, as described previously; many involved the use of elevated temperatures, compatible with SiO_2.

As the aspect ratios increased and low-ε dielectric films introduced, the choices for filling the features with metal, without seams or voids, were limited. CVD and/or directional sputtering were used initially (and the only practical options for Al-based interconnections) but for Cu electroplating (Chapter 5) is now used as the more satisfactory, economical process.

6.16.3.1 Process Steps

After the contacts to the active regions are made, the first-level metal interconnection is formed by a single damascene process.

Figure 6.18a shows the layers at the start of the DD process for the next levels using (encapsulated) Cu and a low-ε interlevel dielectric. It shows, as mentioned earlier, that step (1) above may not be a simple process if etch/polish stops are included and that the full benefit of the low-ε interlevel dielectric is not realized because of the higher ε of such layers (e.g., SiC:H, or SiN). Figures 6.18b–e show possible processing sequences characterized as via-first and trench-first with several options for the total process (Maenhoudt et al., 2001).

In the via-first process, via lithography is done on a planar surface. For the full etch (Figure 6.18b), resist erosion and the integrity of the etch stop are the concerns because of the of the depth to be etched. Trench lithography is a challenge because of the severe topography. To counter attack of the etch stop at the Cu layer, an organic film is deposited into the bottom of the via. DeJule (2000) described the use of a BARC layer for completely filling all of the etched holes so that the resist layer is planar, eliminating the impact of the hole sizes and distribution on lithography. Maenhoudt et al. (2001) found that planarization required a double coating. This sequence is insensitive to misalignment, i.e., the critical dimension specification is met, even if the trench overlaps the via differently at the sides. After the trench is etched and the organic material stripped, both via and trench are filled with the metals in a single step. When the via is partially etched (Figure 6.18c) the via bottom must be completely cleared, making the trench etch easier but the lithographic problem of the topography remains. This sequence is sensitive to misalignment in that the via may be smaller than specified, resulting in poor fill and yield loss.

In the trench-first process, the trench lithography is done on a planar surface. When the trench only is etched (Figure 6.18d) no top etch stop is required over the interlevel dielectric; the etch terminated by a stop layer. The via topography is more severe than in the via-first process because of

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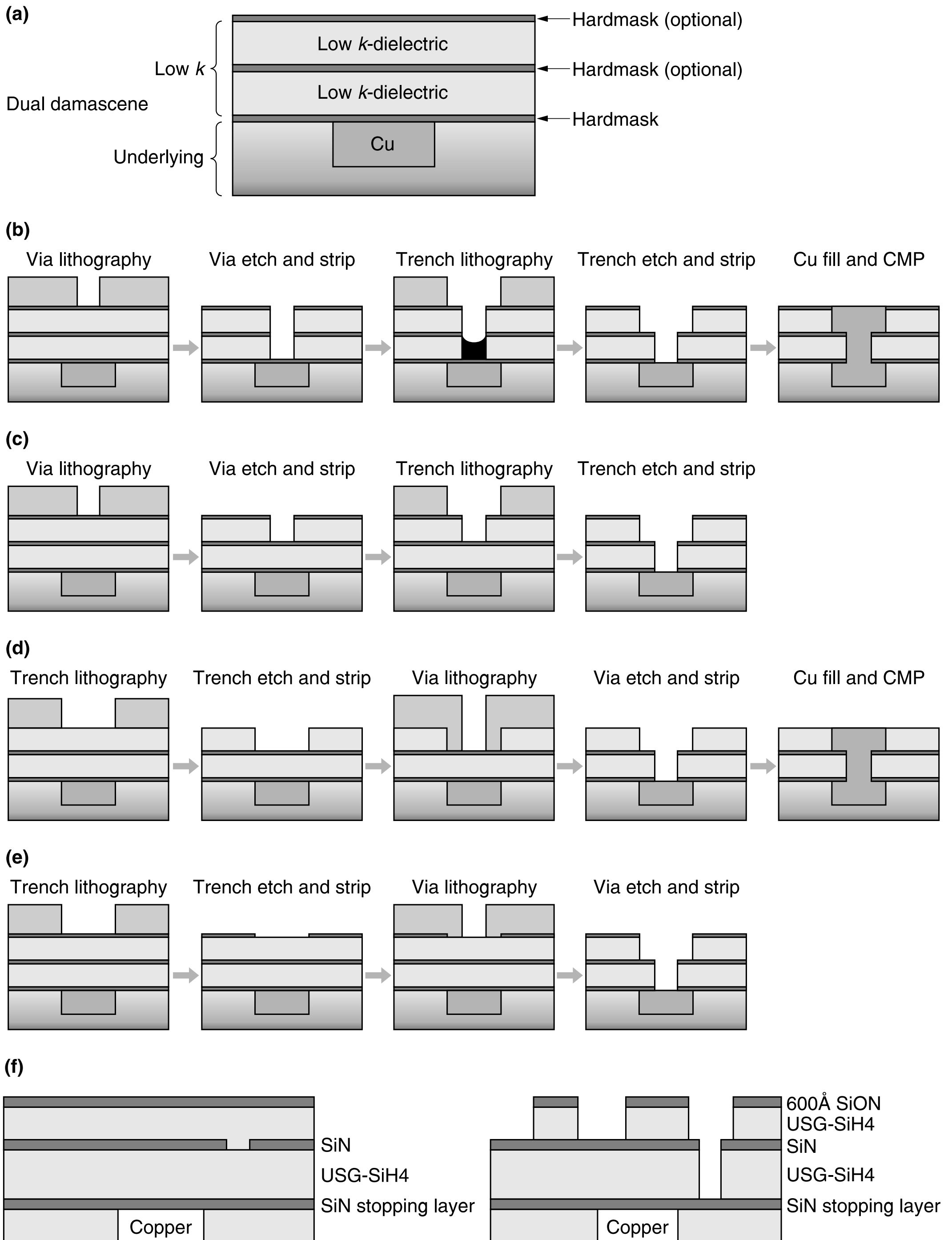

Figure 6.18 Dual damascene process. (a) Typical stack with low-ε interlevel dielectric. Processing sequences for (b) full via-first at trench level, (c) partial via-first at trench level, (d) full metal-first at trench level, and (e) partial metal-first at trench level. (Reprinted from Maenhoudt, M., I. Pollentier, V. Wiaux, D. Vangoidsenhoven, and K. Ronse, *Solid State Technol.*, 4/2001, S15, 2001. With permission.) (f) Self-aligned, and via-first structure construction. (Reprinted from Y. Morand, *Microelectron. Eng.*, 50, 391, 2000. With permission. Copyright 2000, Elsevier.)

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the possible variety of trench widths and pitches making lithography even more of a problem. This sequence can be alignment insensitive. In the partial etch of the trench (Figure 6.18e), only the top hard mask is etched in trench pattern in the first step. This minimizes the topography impact on via lithography but the process is sensitive to misalignment if the via etch is selective to the hard mask.

Another DD sequence is the self-aligned process, shown schematically in Figure 6.18f; inorganic dielectrics are used throughout. A dielectric film and a stop layer are deposited sequentially; the via pattern is etched into the stop layer which is then coated with the remainder of the interlevel dielectric + a hard mask The trench pattern is formed in the hard mask followed by etching both vias and trenches in a single step. This process is sensitive to misalignment.

DeJule (2000) stated that "some believe dual-damascene is pretty much an etch issue." The etching steps involved are the via, trench, and bottom protective layer etches and the polymer strip. Successful processing results in a trench profile that is rectangular with no fences (ridges) in the via holes.

6.16.3.2 Problems

Several unwanted features in the etched trenches during RIE of the interlevel dielectric in the trench etch of the via-first process are undercut, bowing, oxide ridges (fences) faceting, bottom rounding, and microtrenching. An organosilicate glass used to study fencing was treated as a composite of a traditional Si–O material and a C-based one by Jiang et al. (2001). It is expected that oxide ridges can form whether a film consisting of Si, C, H, O, or SiO_2 is used as an interlevel dielectric.

Microtrenching (Figure 6.19a) is enhanced etching at the edges of a feature. It can result in poor seed layer coverage and high electric fields at the highly curved microtrench bottoms (Keil et al., 2001). The profile has been attributed to forward reflection of ions onto the foot of the sidewall. Seta et al. (2001) postulated that at higher pressures (e.g., > 40 mtorr) the effect occurs because fluorocarbon films are formed more easily at the center of a feature (due to shadowing of CF radicals), resulting in enhanced etching at the edges.

Bottom rounding (Figure 6. 19b) is typically AR dependent leading to a loss of line resistance control (Keil, et al., 2001). Their model of the etch process indicated that a neutral-limited ion-assisted etch regime is required for a flat etch front, since microtrenching is to be expected in a strongly ion-limited regime and rounding in a strongly neutral-limited one.

Faceting at the top of the via (due to the angular dependence of the sputtering yield) and fencing around the via hole during the trench etch in the via-first process are particularly detrimental to yield and performance since the thin barrier layer may not cover such features adequately and oxide ridges may fall into the vias during a presputter etch (Jiang et al., 2001).

An example of an oxide fence is shown in Figure 6.19c. The simulation of oxide fencing by Jin and Sawin (2003) indicated that the evolution of the profile is controlled by the ion and neutral flux distribution along the surface and the angular-dependent etching yield (as affected by a polymerizing etchant). Their conclusions, which were in agreement with those of Kropewncki et al. (2001), were that the shape of the via and the etch rate ratio SiO_2/BARC affected oxide fencing. Fencing is due to ion and neutral shadowing by the BARC in the via and trench. It was absent when the vias were bowed because shadowing by BARC is at a minimum. Since ions are not perfectly directional and neutrals are cosine distributed, the vertical BARC in straight-walled vias does not eliminate shadowing so that there was some fencing. The shadowing effect is greatest and the fences tallest in the case of tapered vias. Bowed profiles are not, however, the optimum shape for coverage by a seed layer. There is no ion shadowing and, thus, no fence if etching selectivity of oxide to BARC is decreased sufficiently so that the height of the BARC film is always lower than that of the etched trench surface. However, this also lowers the etching selectivity of oxide to photoresist, not a practical solution since resist thickness is kept to a minimum.

Some specific suggestions that have been made to eliminate or minimize fences have been: (1) decreasing the N_2 content of a C_4F_8/N_2/Ar etchant to increase physical sputtering (Jiang et al., 2001)

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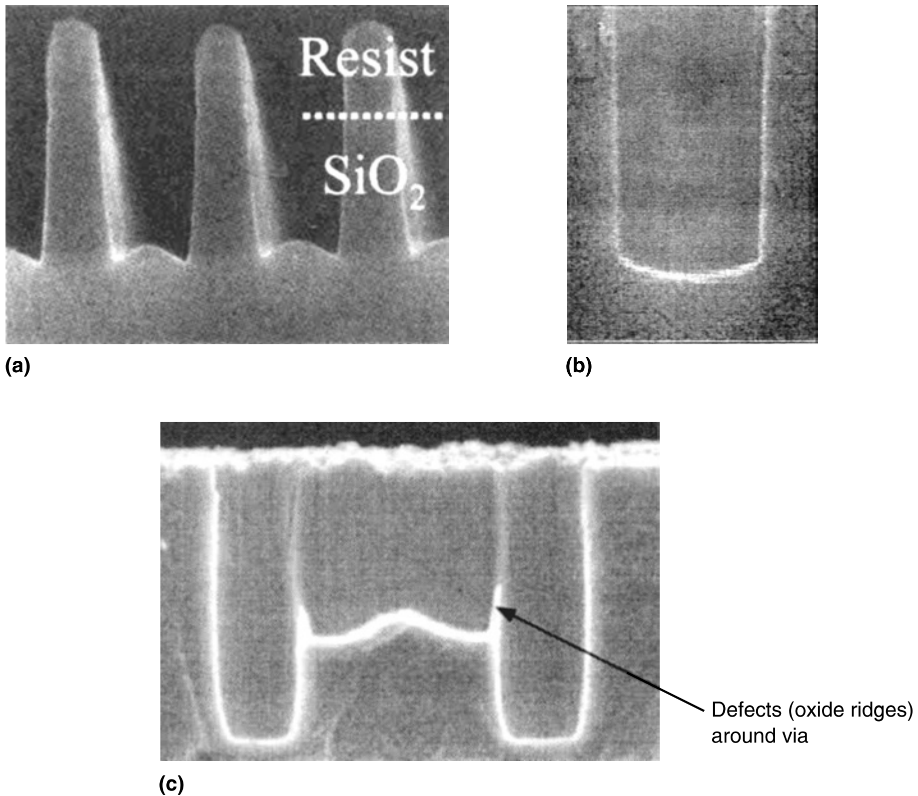

Figure 6.19 Problems encountered with RIE of the interlevel dielectric. (a) Microtrenching. (From Seta, S., M. Sekine, H. Hayashi, Y. Yoshida, T. Yamauchi, *Jpn. J. Appl. Phys.*, 41, 5769, 2002. With permission. NOTE: Figure only, not text) (b) Bottom rounding. (Reproduced from Keil, D., B.A. Helmer, G. Mueller, and E. Wagganer, *J. Electrochem. Soc.,* 148, G383, 2001. With permission of the Electrochemical Society, Inc.) (c) Oxide fences (ridges). (From Jiang, P., F.G. Celii, W.W. Dostalik, and K.J. Newton, *J. Vac. Sci. Technol.*, A19, 1388, 2001. With permission.)

and (2) using a less polymerizing etchant to minimize deposition on the sidewalls (Jin and Sawin, 2003). A last resort is the use of a middle stop layer at the cost of increasing ε of the stack.

Poisoning of DUV photoresists is a problem when low-density or nanoporous films are exposed to N_2 in the processing cycle. Amines are produced, trapped in the film, and then diffuse into photoresist so that the exposed resist cannot be developed. Although a cap layer may prevent poisoning during the via etch, it will occur as the walls are exposed during the trench etch (Shannon, 2001).

6.16.3.3 Cleaning

Finally there is the problem of stripping the photoresist and unetched BARC layers. The smaller features make residue removal more difficult.

The traditional ashers are no longer adequate when the interlevel dielectric is a low-ε film. These films are usually degraded by an O_2 plasma and Cu is sensitive to oxidation. Although the Cu surface is usually protected by a cap layer, inadvertent etching of the cap can expose the Cu to an O_2-containing plasma which may result in increased via resistance (Krishnamoorthy et al, 2002).

Stripping in a downstream microwave plasma reactor using 5% H_2 in He at 250 to 300°C was effective for resist strip and had minimal impact on porous MSQ (Waldfried et al., 2003).

A method known variously as cryogenic, cryogenic aerosol, or aerosol cleaning is based on the Joule–Thompson effect, i.e., the cooling of a pressurized gas as it is expanded in a nozzle. Upon

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cooling, solid particles of the gaseous species are formed. The particles are directed toward a contaminated surface where they displace the contaminants which evaporate, leaving the surface together with the gas. One version used CO_2 (inventors, dates for US 4,806,171). McDermott et al. (1991) stated that CO_2 was prone to contamination and therefore substituted an aerosol of very pure solid argon particles in an N_2 carrier gas. Rotating the substrate and spraying the aerosol in conjunction with the rotation help remove the particles from the substrate (Srikrishnan and Wu, 1994).

Supercritical CO_2 ($SCCO_2$) liquids containing tetraethylammonium hydroxide (TMAH), methanol, and water used at high pressure (3000 psi) and moderately elevated temperature (70°C) were effective in removing residues. The liquid is in the form of droplets dispersed in the CO_2, which provides efficient transport of the droplets of active chemicals into small features. The mechanism of removal appeared to be undercutting and dissolution of the soft resist beneath the crust (Myneni and Hess, 2003).

6.16.3.4 Drying

A technique based on the Marangoni principle was proposed as a residue-free alternative to spin drying. It is compatible with both hydrophilic and hydrophobic surfaces. "Drying is based on a physical force that moves liquids with areas of differing surface tension. Small amounts of low-surface-tension water (including absorbed IPA) are pulled into the bulk liquid, which has a normal surface tension" (Wolke et al., 1996) taking with it loosely adherent particles. The principle was applied to drying wafer surfaces in an IPA-N_2 atmosphere by smoothly removing wafers from the bath. According to Wang et al. (1998), the weakness of the process is the need to lift the wafers mechanically and the use of very large volumes of deionized (DI) water. To circumvent these problems, with the surface tension gradient (STG, i.e., Marangoni principle) process, point-of-use DI water filtering, to provide ultrapure water, was incorporated. After cleaning, the water is drained slowly and followed by *in situ* motionless drying in which the hot N_2 is introduced after the water is drained.

6.17 CHEMICAL MECHANICAL PLANARIZATION (CMP)

6.17.1 Introduction

This technique, also called chemical mechanical polishing, was used for many years in semiconductor fabrication for wafer polishing and surface treatment. When it was first applied to the conductors and insulators on the wafer surface (Chow et al., 1988; Beyer et al., 1990), it was viewed as an interesting demonstration but too dirty to be used in back-end processes. Now, however, it is a standard procedure for many steps in manufacturing facilities.

Despite problems to be discussed, it is a simpler method than those described earlier, and results in better planarization over longer distances and over a wider range of pattern factors and feature sizes. It is the most effective method for achieving global planarization.

6.17.2 Principles

CMP differs from mechanical grinding which is used, for example, for polishing lenses. In grinding the abrasive particles are pushed into the substrate by the polishing pad and remove that material. In CMP the slurry in which the abrasives are suspended and the polishing pad in which the abrasives become embedded (not the abrasives alone) are involved in the process.

A model for CMP (Figure 6.20) was proposed by Kaufmann et al. (1991) for CMP of W and has been accepted, generally, as a framework for all CMP processes. CMP was viewed as a sequence of two steps which is repeated until the endpoint is reached: (1) a chemical reaction with slurry

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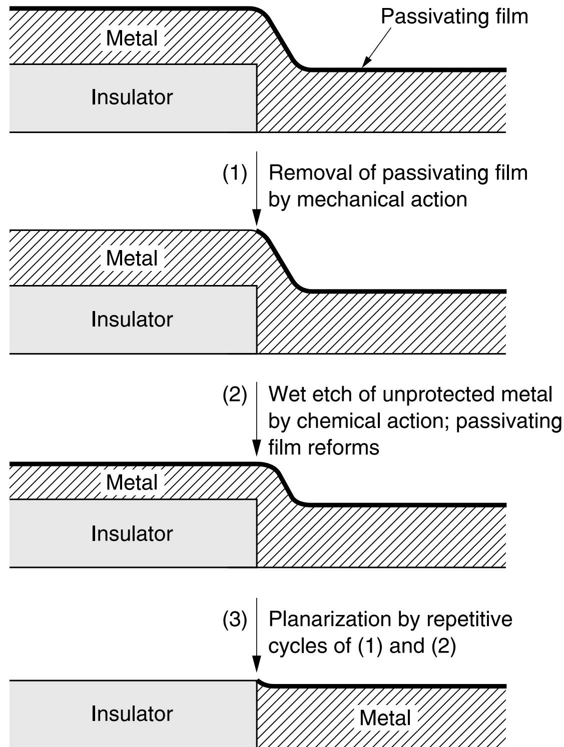

Figure 6.20 Model for CMP of W. (Reproduced from Kaufman, F.B., D.B. Thompson, R.E. Broadie, M.A. Jaso, W.L. Guthrie, D.J. Pearson, and M.B. Small, *J. Electrochem. Soc.*, 138, 3460, 1991. With permission of the Electrochemical Society, Inc.)

components to form a passivating surface layer which is easily removed and (2) mechanically enhanced abrasion of the converted surface layer by polishing grains in the slurry and/or dissolution of the layer and, to a limited extent, of the substrate, under the influence of pressure applied to the polishing pad in which the grains are embedded. The mechanical action is responsible for planarization since the pad exerts a force on the high points, increasing their removal rate, while the surface layer protects the low regions. Ideally, the abraded material is removed mechanically or dissolved and then carried off by the flowing slurry, not redeposited. In CMP there should be no direct action on the bare substrate that result in scratching, and, in the case of metals, corrosion.

The removal rate is affected by the type of pad, the pressure, i.e., the load applied to the pad (affects the real contact area between the pad and the wafer surface), the active species in the slurry (affects the chemical nature of the surface layer), the nature of the abrasive, the pH of the slurry, the speeds of the wafer and the polishing pad (the removal by abrasives is proportional to the area swept out), as well as by the chemical and physical properties of the substrate. For example, softer films polish at a higher rate than do harder ones (Izumitai, 1979; Dai et al., 1995); this is illustrated by the increase in the CMP rate of a plated Cu film as the grain size increased (and the hardness decreased) (Jiang and Smekalin, 1999). Tseng and Wang (1999) found that Al and W films with smaller gains polished more rapidly and attributed this to a larger grain boundary area available for slurry attack. A tensile stress of an oxide film, by weakening the bond structure, enhanced the chemical component of CMP (Tseng et al., 1999b). There was an influence of the grain structure of W on its CMP rate. An increased area of the (114) phase, which occurred at elevated deposition temperatures and increased thickness, resulted in a decreased rate (Maynard et al., 2002).

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6.17.3 Models

The polishing rate is often described by the Preston equation for the mechanical polishing of glass (Cook, 1990):

$$\Delta H/\Delta t = K_p(L/A)(\Delta s/\Delta t)$$

where H = height, t = time, L = load, A = surface area, Δs = relative travel speed between wafer and pad, and K_p = Preston coefficient (area/force).

For purely mechanical polishing (e.g., grinding)

$$K_p = 1/2E$$

where E = Young's modulus of the material being polished (Steigerwald et al., 1997). For CMP K_p is process dependent, related to chemical erosion processes and material properties.

It is usually written as

$$\mathrm{RR} = K_p P V$$

where RR = removal rate, P = polish pressure, and V = velocity of the wafer across the pad.

Tseng and Wang (1997) found that the Preston equation did not describe the results for CMP polishing of SiO_2 and proposed an alternative:

$$\mathrm{RR} = mP^{5/6}V^{1/2}$$

where m = a constant associated with properties of pad/material to be polished, slurry concentration, and chemical processes during CMP. This equation arose from a model combining fluid flow and solid deformation. It fit the experimental data at high pressure and high carrier speed but not at low pressure and high speed. They postulated that under such conditions, the flowing particles are swept away before they can indent the surface of the wafer.

This equation (as does the Preston equation) implies that the chemical and mechanical contributions are independent. However, they found that m was not constant but had a slight pressure dependence, due probably to stress-assisted chemical attack by the slurry. There may also be an influence of the speed so that the equation becomes

$$\mathrm{RR} = m(P, V)P^{5/6}V^{1/2}$$

The nonlinear dependence of the rate on V was explained by a deterioration in slurry abrasion capability (Tseng et al., 1999a).

The equation of Tseng and Wang was modified by Hernandez et al. (1999) for CMP of Al and SiO_2 as

$$\mathrm{RR} = mP^aV^b$$

In addition to the latitude in the values of the exponents (both almost always < 1), the constant m is now independent of P and V. A slightly better fit to their data was a second-order polynomial (not specified) but they said that only the power function satisfied the experimental condition that the CMP rate for Al rate becomes zero at P and $V = 0$.

If there is any significant removal of material in the absence of pressure and velocity (i.e., etching), then the equation is modified by an additional term to account for it:

$$\mathrm{RR} = mMP^aV^b + \mathrm{RR}_o$$

Paul (2001) developed a model for CMP which correlated the rate of polishing with the kinetics of the chemical and abrasive reactions. The effective abrasive concentration is determined by the number of available sites on the pad. The general form of the rate equation was given as

$$\mathrm{RR} = R_o + \mathrm{C} \times M/(C + M)$$

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where R_o is the rate in the absence of abrasion and C and M represent the chemical and mechanical processes. C depends on the nature of the surface layer (thickness, surface coverage, kinetics of formation and loss) which is determined by the chemical components of the slurry and the nature of the substrate. M depends on the characteristics of the pad and abrasive and interactions between pad and substrate as well as the pressure and the polishing speed. The implication is that increasing either component separately can increase the polish rate to some limiting value which can be extended by changing both at the same time.

Paul (2002) expanded his model to include the effect of pressure which affects the real contact area between the pad and the substrate and the depth of material removed. The mechanical removal was assumed to be simply proportional to speed. It predicted both Preston and non-Preston behavior in different limits.

Sorooshian et al. (2004) suggested a new definition of the Preston constant K which "considers the effect of the polishing temperatures through an Arrhenius relationship and a newly defined thermally independent constant K":

$$K = \mathrm{K}\exp(-E_{\mathrm{comb}}/RT)$$

where E_{comb} denotes the combined activation energy of the process, both chemical or mechanical. A high value of E_{comb} indicated a thermally dependent process. The thermal contribution to CMP of Cu was about 9 times that of the CMP of thermal oxide. They suggested that determining E_{comb} "can be critical in designing novel pads and slurries with controlled chemical and mechanical properties" although they did not give any solid examples.

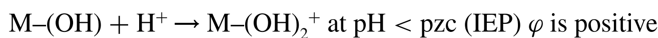
A model based on a stress-enhanced nucleation of etch pits and their annihilation that removes the surface layer led to a dependence of the rate on the 2/3 power of the pressure. When polishing a patterned sample, the pressure exponent was ¾ because of the small area being polished (Sukharev, 2001).

There have been many other attempts at understanding CMP. Among these are: tribology analysis (Runnels and Eyman, 1994), stress analysis (Wang et al., 1997), a model incorporating a lubrication model for slurry transport and a mass transport model for material removal (Sundarajan et al., 1999), pattern planarization model (Chen and Lee, 1999a,b), a model of mechanical wear and abrasive particle adhesion (Ahmadi and Xia, 2001), and a contact mechanics model (Lai et al., 2002). Examples of the kinds of investigations into the basic processes in CMP are: a study of slurry transport (Coppeta et al., 2000) and the effect of particle size on rate and defects (Basim et al., 2000), and a simulation of CMP by the use of an AFM-scratched metal wafer under a range of conditions (Devecchio et al., 2000).

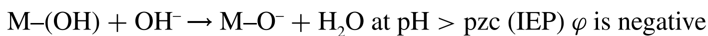
6.17.4 Role Of Electrostatic Forces

The electrostatic interactions between the substrates and the slurry particles play an important role in determining the dependence of the polish rate on the pH of the slurry. The charges, developed in an aqueous slurry, on the surfaces of the substrate and on the slurry particles are measured by the zeta potential, φ. In addition to φ are the electrical double layers immediately adjacent to the solid surfaces and the van der Waals forces (Mazaheri and Ahmadi, 2003).

The zeta potential is the one most easily measured and the one to which most attention has been paid. The reactions occurring in solution are



$$\mathrm{M{-}(OH)} + \mathrm{H^+} \rightarrow \mathrm{M{-}(OH)_2^+} \text{ at pH} < \text{pzc (IEP) } \varphi \text{ is positive}$$



$$\mathrm{M{-}(OH)} + \mathrm{OH^-} \rightarrow \mathrm{M{-}O^-} + \mathrm{H_2O} \text{ at pH} > \text{pzc (IEP) } \varphi \text{ is negative}$$

where M = Si, Cu, Ta, etc., and pzc is the pH at the point of zero charge, i.e., the isoelectric point (IEP). Zero charge means no net surface charge, i.e., the concentrations of positively and negatively charged species at the surface are equal. At the pzc the colloidal particles of the abrasive agglomerate.

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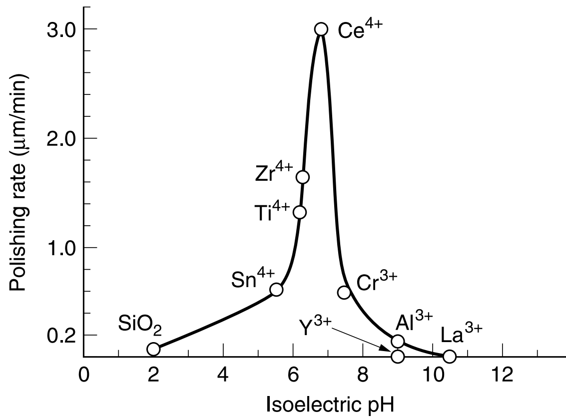

Figure 6.21 Polishing rate of silica in a near-neutral slurry vs. the isoelectric pH. (Reprinted from Cook, L.M., *J. Non-Cryst. Solids*, 152, 1990. With permission. Copyright 1990, Elsevier.)

Cook (1990) discussed the relationship between the polishing rate of silica in a near-neutral slurry and the pzc values of the abrasive oxides involved; this is illustrated in Figure 6.21. He therefore concluded that the surface conditions for the best removal of silica in a neutral slurry are a negative charge on the silica surface and a neutral abrasive.

Osseo-Asare (2002) offered an explanation of the trend in Figure 6.21. He visualized CMP as a two-step process: dissolution followed by adsorption of these species by the abrasive particles. The mass action equations proposed for the processes led to the conclusion that, for a given series of abrasive particles with different values of pzc, the highest silicate adsorption and thus the highest rate would occur using the abrasive whose pzc coincided with the selected slurry pH.

Ramarajan et al. (2000) and Mazaheri and Ahmadi (2003) found, however, that the pH for the maximum polish rate occurred when the charge on the substrate surface was opposite to that of the slurry. At a pH where the charges were the same, so that the surfaces repelled each other, opposing the applied external pressure, the rate dropped. Increasing the ionic strength of the slurry by the addition of a salt decreases both the magnitude of the zeta potential and the width of the double layer; decreasing the electrostatic interaction between the particles and the substrate (Ramarajan et al., 2000). Thus, rates decrease at pH values at which the substrate and particle are oppositely charged and increase at pH values at which the charges are the same.

Electrostatic forces also play a role in contamination; strong repulsive forces minimize particulate contamination by slurry particles. Lee et al. (2003) measured the interaction forces between various surfaces and the particle contamination on polished wafers using an AFM and an SEM. For example, in an alkaline slurry the attractive force between silica and SiLK was the weakest and that on TaN was the strongest and the number of particles on the polished surfaces was highest on the TaN and lowest on the SiLK.

6.17.5 Equipment

6.17.5.1 Polishers

The early CMP equipment, the *rotary* polisher, was based on that used for polishing Si substrates, i.e., to smooth the surface and remove damage. A schematic view of the essentials of a rotary polisher is shown in Figure 6.22. The heads are flat plates attached to templates which have recesses for the wafer to constrain the wafers mechanically. They contain wet inserts which set the

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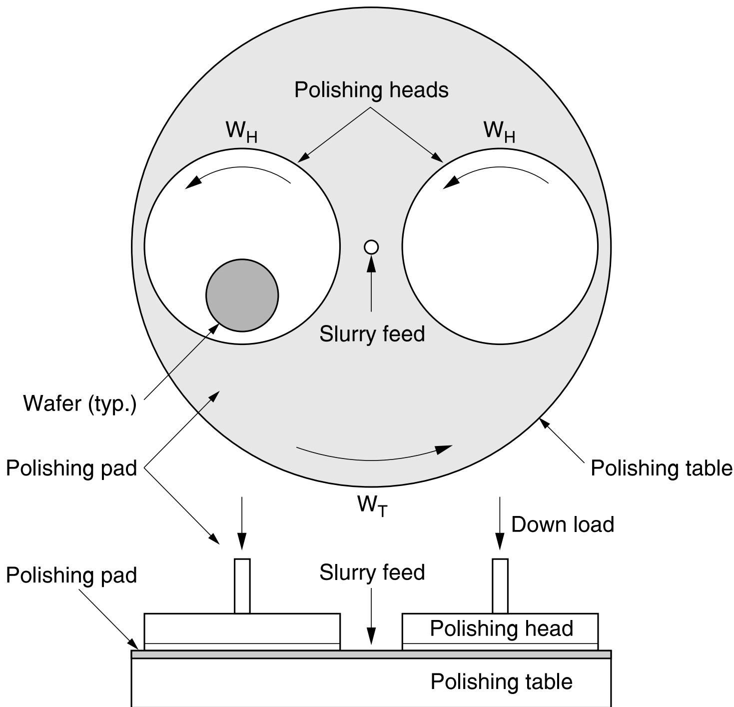

Figure 6.22 Essentials of a rotary polisher. (Reproduced from Patrick, W.J., W.L. Guthrie, C.L. Standley, and P.M. Schaible, *J. Electrochem. Soc.*, 138, 1778, 1991. With permission of the Electrochemical Society, Inc.)

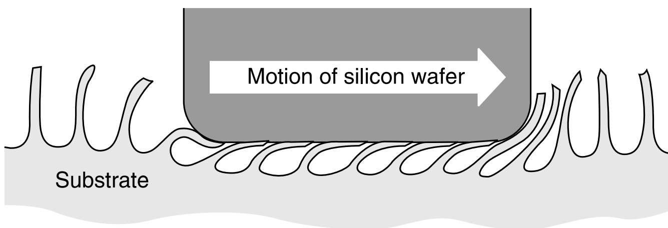

Figure 6.23 Schematic showing the interaction between the polishing pad and the wafer to be polished. (Reprinted from Ali, I., S.R. Roy, and G. Shinn, *Solid State Technology*, 10/94, 63, 1994. With permission.)

wafers slightly above the surface of the templates; the wafers are held in place by surface tension. A downward force is applied to the head. The polishing pad is mounted on the table (platen). The slurry is pumped to the center of the table. Both table and heads are rotated at a constant angular velocity.

The interaction between the polishing pad and the wafer to be polished is shown schematically in Figure 6.23. A new design of a polishing head was introduced by Applied Materials: it has a "flexible membrane that applies uniform pressure over the wafer backside while conforming to the wafer shape" (Wjekoon et al., 1998).

The orbital polisher is a variant of the rotary polisher, in which the head containing the polishing pad orbits as the carrier holding the wafer rotates about a central axis. Gotkis et al. (1998) cited the advantages of orbital polishing as "high material removal uniformity, planarization efficiency, high throughput, small footprint and low cost of ownership."

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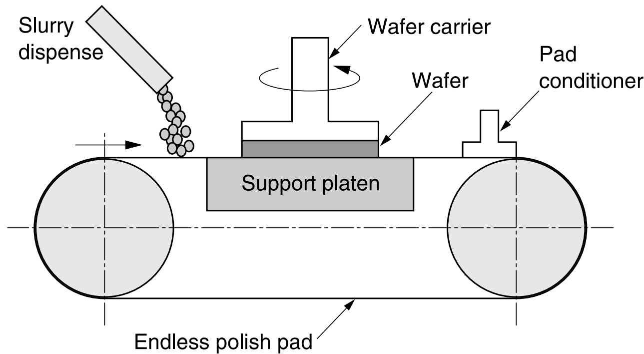

Figure 6.24 Linear polisher. (Reprinted from Jairath, R., A. Pant, T. Mallon, B. Withers, and W. Krusell, *Solid State Technol.*, 10/96, 107, 1996. With permission.)

An improvement combines orbital motion with one or more motions: rotational, oscillating, sweeping, and linear. This apparatus has been designated as an oscillating orbital polisher. These combined motions have also been used for conditioning polishing pads to make conditioning more uniform and extend the life of the pad (Adams et al., 2001).

A linear polisher (OnTrak System's Linear Plamarization Technology, LPT™) was designed specifically for planarizing integrated circuits. A schematic of the system is shown in Figure 6.24. "The polishing pad is an endless loop of conventional pad material which is continuously driven past the wafer by a pair of pulleys. Slurry is fed to the pad upstream of the polishing region, and a diamond grit pad conditioner sweeps across the polish pad downstream of the polishing region" (Jairath et al., 1996, 1997). The substrate is rotated onto the linearly traveling pad, planarizing the features. Beneath the belt is a proprietary fluid bearing which also controls the pressure distribution on the wafer surface. The usual slurries and pad materials are used in LPT™.

The advantages cited for LPT™ (as compared with rotary polishers) are higher operating speeds (improvement of removal rate and planarization) and controlled lower pressure (improvement of planarization efficiency), the polishing pressure across the pad is controlled and the wafer rotated, resulting in a radially symmetric polish profile. Lower within wafer nonuniformity (WIWNU) has been reported. In addition, there appeared to be only marginal dependence on pattern density variations; peeling at the edges of Cu/low-ε wafers has been eliminated (Jairath et al., 1996; Jin et al., 2001).

A polisher designed to reduce the mechanical stress on low-ε films during CMP is called "PASCAL CMP" (pad scanning local-CMP) (Hyashi, 2000). The wafer is held face up against a small polishing pad which is rotated very rapidly as it scans the wafer using very low pressure.

The machine variables are the pad pressure, rotational speed of the pad and of the table on which the wafer is mounted, and the flow rate of the slurry. There is no intentional heating of the slurry or wafers but the temperature of the pad rises during CMP due to the wear process and possibly chemical reaction (Stein et al., 1999a,b).

6.17.5.2 Consumables

The pads and slurries are called the "consumables"; there is significant activity this area, e.g., Wrscka et al. (2001), Hernandez et al. (1999), Sandhu and Doan (1996), Cadien and Feller (1994), Tuttle (1993), and Budinger and Jensen (1990). Cast polyurethane or polyurethane-impregnated felt are the most common pad materials. They are classified as hard or soft; particles can be added to the pad material to modify its mechanical properties. Yang (2000) defined a hard pad as one that has a high Young's modulus (low compressibility) and low conformity, i.e., limited pad bending over topographical features. The porosity of the pad (both macro and micro) is controlled by the cure

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dynamics during pad manufacture and by the use of mechanically punched perforations (holes, channels). Another kind of pad material has open cells (Anjur et al., 1998). Grooved pads allowed for better transport of slurry across the wafer and thus resulted in better polish uniformity (Zabasajja et al., 2001).

The thickness, roughness, and compressibility are other important properties of the pad. They all have an influence on both the removal rate and the surface finish of the polished wafer. According to Ahmadi and Xia (2001), "pads with random surface roughness lead to a Preston type removal rate and those with wavy surface roughness lead to sublinear dependence of removal rate on external pressure."

The surfaces of a hard and a soft pad are shown in Figure 6.25. As the pad is used, the pores in which the slurry is transported across the wafer are filled and the pad becomes smooth; the process is called glazing. To restore the surface of the pad to its original state so that the removal rate stays constant (with no degradation of uniformity) and to extend the life of the pad, it is conditioned (dressed, scrubbed) between each wafer using brushes, emery paper, etc. A new and a glazed pad are compared in Figure 6.26. Figure 6.27 shows changes in a soft pad as it is used and then conditioned. In this case there was no glazing, just dried slurry particles accumulating on the surface; these were removed by conditioning. The particles embedded within the pad remain and stiffen the pad (harden it slightly). Although some of the pad specifications are covered by patents, many of them are proprietary.

Hard, incompressible pads will achieve the best planarity since they require more force to deform and exert more pressure on the high areas but improved uniformity and smoother surfaces are obtained using softer pads (Morimoto et al., 1993). "Removal rates for a soft pad are lower than those for a hard pad under equivalent conditions" (Mazaheri and Ahmadi, 2002).

The slurries contain abrasive particles of various sizes, shapes, and concentrations; the most widely used are oxides of Si and Al; Ce (Homma et al., 1995), Mn (Hara, 1999), and Zr oxides (Chen et al., 2000) have also been investigated. Both fumed and colloidal (Kallingal et al., 1998) alumina have been used. Usually fumed silica is used but silica particles grown by hydrolysis of TEOS was suggested by Wrschka et al. (2001). In this system, the shape (nodular or spherical) and size of silica particles was controlled by adjusting the reaction time, temperature, and concentration of TEOS. Basim et al. (2000) reported that when particle sizes are small a contact area-based mechanism is dominant but as particle sizes increase, an indentation mechanism becomes more important. They also found that coarser particles tended to create critical defects on an oxide film and

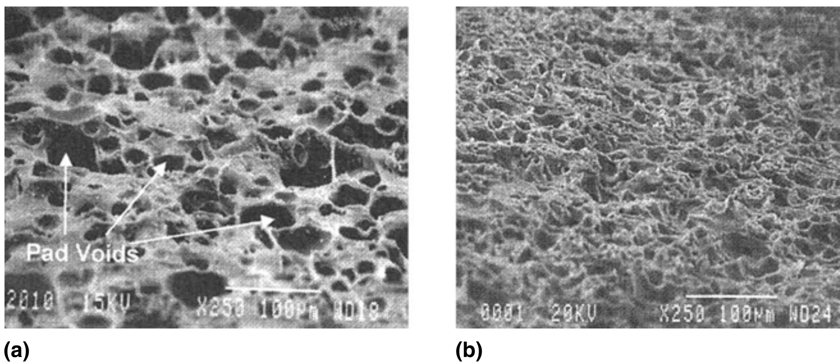

Figure 6.25 SEM images of the surfaces of (a) a hard and (b) a soft pad. (Reproduced from Hernandez, J., P. Wrschka, Y. Hsu, T.-S. Kuan, G.S. Oehrlein, H.J. Sun, D.A. Hansen, J. King, and M.A. Fury, *J. Electrochem. Soc.*, 146, 4647, 1999. With permission of the Electrochemical Society, Inc.)

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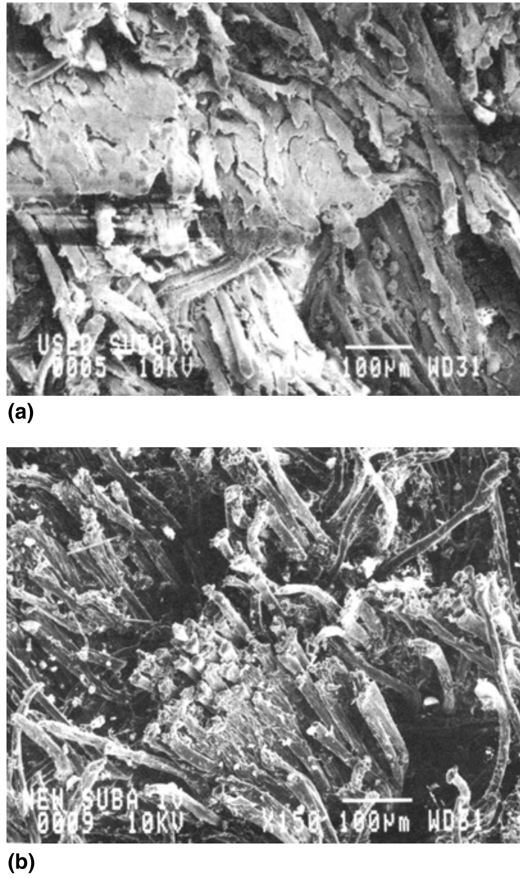

Figure 6.26 SEM images comparing (a) a new and (b) a glazed pad. (From Steigerwald, J.M., S.P. Murarka, and R.J. Gutmann, *Chemical Mechanical Planarization of Microelectronic Materials*, John Wiley, New York, 1997.)

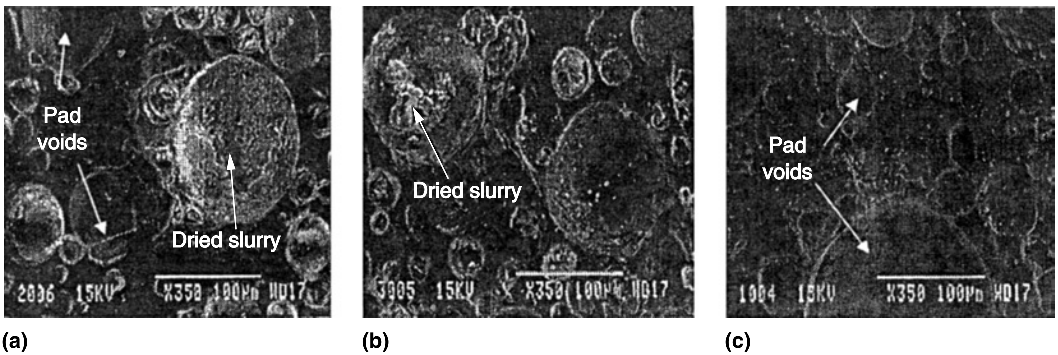

Figure 6.27 SEM images illustrating the changes in a soft pad (a) soaked, (b) soaked and polished, and (c) soaked, polished, conditioned. (Reproduced from Hernandez, J., P. Wrschka, Y. Hsu, T.-S. Kuan, G.S. Oehrlein, H.J. Sun, D.A. Hansen, J. King, and M.A. Fury, *J. Electrochem. Soc.*, 146, 4647, 1999. With permission of the Electrochemical Society, Inc.)

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the damage increased with increasing size and concentration of coarser particles. Mazaheri and Ahmadi (2002) reported that "CMP with bumpy abrasives generally has a lower removal rate when compared with that having smooth spherical particles under similar conditions." Other components of the slurry are compounds for pH adjustment and control (buffers), surfactants (Neirnck et al., 1996; Chen et al., 2000), and, for metal CMP, oxidizers and complexing agents (e.g., Kaufman et al., 1991; Steigerwald et al., 1995). As noted above, there are commercially available slurries (e.g., Rodel QCTT 1010, Cabot SS-25). Because this is still an emerging technology, the compositions of slurries are often proprietary (until a patent is issued). Since they are often reported as slurry "A" vs. slurry "B," or additive "X," it is difficult to evaluate the results. Slurries are usually premixed in large containers and pumped through a dispenser; an *in situ* slurry delivery system which mixes the components just before delivery to the table has been proposed by Murphy et al. (1995).

The consumables interact, so that, for example, when oxidants in a slurry were compared and contrasted, different pads and/or abrasives may be employed (e.g., Wijekoon et al., 1998). The variability in the choice of the consumables probably accounts for many of the apparent contradictions reported in the literature.

The variables studied in the development of a CMP process are, therefore, the pad characteristics, the pressure on the pad, the speed of the pad and wafer, the composition of the slurry (chemicals and abrasives), and its flow rate. The results that are examined include the rate of planarization (throughput), selectivity to barrier layers, reproducibility, WIWNU, pattern geometry effects, surface quality/defects, and finally, device performance. Other factors are the costs of the slurries, pads, ease of slurry use, and reliability of the polishing apparatus. Often design of experiment techniques are used to evaluate and optimize a specific process.

There are many suppliers of polishers, slurries, and pads. There are both single- and multiple-head polishers, usually computer controlled with load/unload cassettes for easy integration into the processing flow.

6.17.5.3 Endpoint Detection

Reliance on polishing time, using the results obtained from dummy wafers, to determine the endpoint is inadequate as well as time-consuming and costly. Endpoint detectors have, therefore, become mandatory.

There are many kinds of systems offered commercially and a large number of patents covering the details of the methods. A selection from the vast literature follows.

The change of friction between the rotating wafer and the polishing surface can be sensed by measuring the change in motor current which can be used to adjust or stop the process (Cote, 1990; Sandu et al., 1991; Cote et al., 1994; Litvak, 1995). Better results have been obtained for CMP of metals than for oxide. Monitoring the drag forces is another method (Moore, 2001).

The capacitance method (Miller and Wagner, 1992; Lai et al., 1993) is useful for polishing a dielectric film since it forms a capacitor with the slurry acting as the counter electrode. Although it works well with blanket films, topography and pattern density affect the output so that calibration for each type of device wafer is needed. Lustig et al. (1994) claimed to improve on Miller's method by using center and guard electrodes embedded in the polishing table and connected to the wafer through the slurry and by applying a high-frequency sinusoidal voltage (0.5 V). The response current flowing through the center electrode is monitored by a differential amplifier. The output voltage is inversely proportional to the remaining insulating film thickness. Another detector uses center and guard electrodes connected to a high-frequency, low-voltage generating circuitry for converting a current into an analog voltage. The current is inversely proportional to the thickness (Lustig, 1994).

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Another method appropriate for dielectric films uses a laser interferometer, directed at an unpatterned die on the wafer to determine thickness (Schultz, 1993). Insulator thickness change can be determined by irradiating the back side of a wafer with IR (emitter and detector located in the polishing head assembly).

The method of Fukuroda et al. (1995) using polish head vibration measured with an accelerometer can determine smoothing of insulator peaks but not the remaining thickness.

Broadband optical reflectance measurements plus signal processing techniques (using the optical properties of the metals and dielectric films given in the standard references) were said "to provide the means to extract precise endpoint signals" (Bibby et al., 1999). IR spectroscopy was used to detect the change in absorptivity as succeeding layers are exposed (Chang, 2002).

Another method measures the thickness of a dielectric layer by exciting surface plasmons in a conductive grating below the dielectric layer and collecting the reflected photons to determine the change in the surface plasmon resonant angle, which, in turn, determines the thickness of the dielectric layer. This method requires a test site (Lansford and Lansford, 2003). Meloni (2001) disclosed the use of a surface plasmon sensor to monitor the progression of chemical reactions during polishing.

A method for determining the endpoint in metal polishing uses a four-point probe array embedded in the surface of the polishing pad to determine the voltage drop from which the thickness may be calculated as polishing proceeds (Adams and Bibby, 2003). Another electrical technique uses sensors embedded in the wafer (Lyons et al., 2003).

An x-ray probe mounted into a recessed region in the polishing platen measures the emitted fluorescent beam to determine the thickness and composition of the layer(s) being polished (Meloni, 2002).

The pad temperature close to the contact area between the pad and the wafer indicated the endpoint of W polishing (van Kranenburg and Woerlee, 1988). The temperature change is caused by the frictional heating of the polished wafer, the slurry/pad system, and the heats of reaction (Chen and Diao, 1996). Several methods of temperature monitoring have been used to detect the interface change between layers. A noncontact thermal probe sensor system used two thermo-sensors, one fixed on the polishing arm to monitor the temperature of the pad, the other to collect the reference platen temperature, and sensed the change between two kinds of polished layers (Chen and Diao, 1996). Substituting a thermal camera for the pad probe, to obtain the two-dimensional thermal temperature of the pad, provided more accurate and reliable information (Chen et al., 1998).

The endpoint of Cu polishing was determined by measuring (1) the decrease in the Cu ion concentration in the slurry, using a capillary and an ion-selective electrode (Zeidler et al., 2000), (2) the concentration of the oxidizing agent in the slurry byproduct (Simon, 2003), or (3) the amount of copper dioxide removed by analyzing the surface of the pad using a laser beam reflected off it (Hu et al., 2003).

Conversion of a reaction product to an easily measurable chemiluminescent material permits monitoring the removal of a film by CMP (Li et al., 2002). A processing monitor sampling the acoustic emission and analyzing them using a Fourier transform detects wafer vibration characteristic of scratching. When excess noise levels are detected the process can be terminated (Sampson, 2002).

The addition of easily detectable impurities such as an isotope of Cu (Lee et al., 2001) or a colorant added to the planarizable layer at the appropriate level (Zhou et al., 2000) add complexity to the wafer processing and appear to offer no advantages over other methods. It is clear that much effort has been expended on EPD devices, based on a variety of principles and techniques, because as the dimensions shrink, the need for accurate process control becomes increasingly important.

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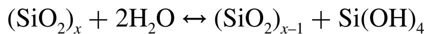
6.18 CMP OF INORGANIC DIELECTRIC FILMS

6.18.1 SiO_2

The chemical component of oxide polishing is the slurry which contains colloidal particles in an alkaline medium (aqueous KOH or NH_3 to reduce ionic contamination). Polishing is critically dependent on the presence of water, since interaction with water is the primary reaction. The attack under load of siloxane bonds (Si–O–Si) by water, to form a hydrated surface, controls the rate of surface dissolution. It is, therefore, not unexpected that silanol groups are found on the surface after polishing (Kaufman et al., 1995). Cleavage of Si–O–Si bonds below the surface is controlled by the diffusion of water in silica. Polishing occurs when the reversible hydration (polymerization) reaction



$$(SiO_2)_x + 2H_2O \leftrightarrow (SiO_2)_{x-1} + Si(OH)_4$$

proceeds in the forward direction, i.e., in the direction of hydration (depolymerization) (Cook, 1990). Material is removed as single silica tetrahedra or small clusters (Izumitani, 1979; Cook, 1990; Sivaram et al., 1992; Ali et al., 1994). The role of polishing compounds had been conceptualized as a chemical tooth expediting bond shearing at the surface and transport of the reaction products away from the surface faster than redeposition.

The influence of the zeta potential on he polish rate of silica is discussed in Section 6.17.4 and illustrated in Figure 6.21 which shows that the highest polish rate for silica in a near-neutral slurry was obtained using a ceria abrasive (pzc ~ pH 7). The choice of polishing agent, however, is not determined solely by polishing rate. For example, although ceria particles in the slurry polish SiO_2 at higher rates than do silica, silica is preferred because it produces smoother surfaces. Increasing the particle size and concentration of the abrasive particle increases the rate because this increases the penetration depth of water, essential for the reaction. The effect is more pronounced at higher pad pressures. Rounder particles increase surface solubility. The nature of the SiO_2 also affects the polishing rate, e.g., BPSG polishes faster than does thermal or PECVD oxide; the rate of PSG increases with increasing concentration of P. Addition of a surfactant with a large polar component produced better uniformity but lower rates (Achuthan et al., 1995).

Wallace et al. (1996), using x-ray reflectivity, found that CMP decreased the surface roughness of PECVD SiO_2 and increased the density of the near-surface region. They concluded that the SiO_2 network was compacted under the applied pressure of the polishing pad which led to enhanced dissolution in the slurry as well as a very smooth surface.

An example of the application of dielectric planarization to circuit fabrication is shown in Figure 6.28. The horizontal and vertical AlCu interconnections were formed by a lift-of process, coated with bias-sputtered SiO_2 and then polished (Patrick et al., 1991). Another example is planarizing a dielectric layer before etching grooves to be filled with metal.

6.18.2 Alternative to Conventional CMP of SiO_2

6.18.2.1 Slurry-Free

In this process the abrasive particles were embedded in the pad and polishing done in water or a basic solution. The advantages cited were: higher throughput (faster polish rate), simple polishing fluid, pad conditioning or break-in not needed, and pad-to-pad consistency. The limitations were: buffing required, further work to determine defectivity levels, and lifetime of the pad (Fayolle et al., 1998).

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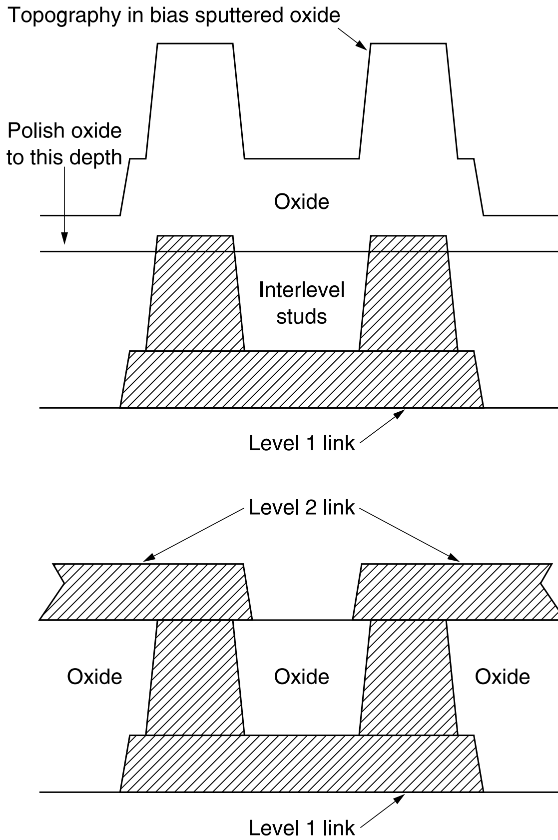

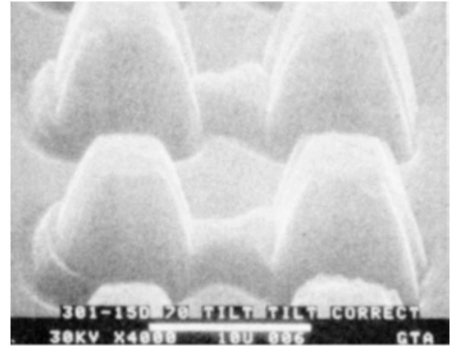

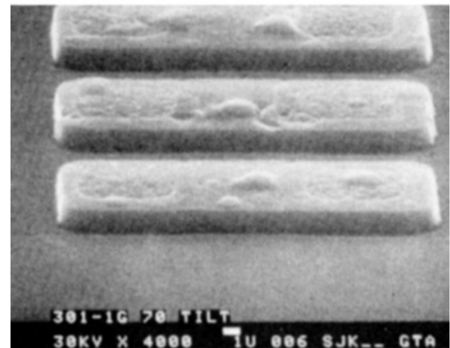

Figure 6.28 Dielectric planarization using CMP. (Reproduced from Patrick, W.J., W.L. Guthrie, C.L. Standley, and P.M. Schaible, *J. Electrochem. Soc.*, 138, 1778, 1991. With permission of the Electrochemical Society, Inc.)

6.18.2.2 Mixed Abrasive Slurry

The mixed abrasive slurry (MAS) consisted of colloidal ceria and calcined alumina in DI water at pH = 4. Addition of ceria lowered the isoelectric point of the alumina slurry. The quality of the surface was very good; it was much poorer when calcined ceria was used with the alumina. The advantage cited for this slurry was an excellent polish rate selectivity of oxide over nitride. The polish rate of oxide in an alumina slurry was low and the surface quality poor. It was suggested that the small ceria particles in a ceria slurry are confined mostly to the pores in the pad and thus their chemical tooth property for removing oxide is inhibited. The enhanced performance of the MAS was postulated to be due to the increased effectiveness of the ceria particles when they are adsorbed on the larger alumina particles, as shown in Figure 6.29 (Jindal et al., 2003).

6.18.3 Silicon Nitride

Two slurries were investigated by Hu et al. (1996). One contained powder-based alumina, DI water, and NH_4 or acetic/nitric acid for pH adjustment, the other colloidal silica in DI water stabilized with KOH or NH_4OH. In the alumina slurry, the polish rate was insensitive to pH at low

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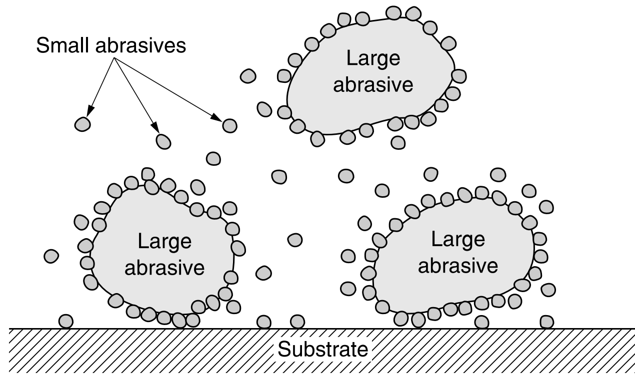

Figure 6.29 Schematic of the proposed polishing mechanism by abrasives in a mixed abrasive slurry. (Reproduced from Jindal, A., S. Hegde, and S.V. Babu, *J. Electrochem. Soc.*, 150, G314, 2003. With permission of the Electrochemical Society, Inc.)

powder concentration; increasing the powder concentration increased the rate. The polished surface was scratch-free but contaminated with particles. The rates were higher in the alkaline silica slurries and the surfaces were scratch- and particulate-free. Reducing the pH decreased the rate, uniformity, and surface finish. Underlayers, especially metals, influenced the polish rates significantly.

Nitride hydrolysis was proposed as the dominant chemical reaction during CMP by Hu et al. (1998). They based their conclusions on XPS and FTIR measurements before and after polishing LPCVD nitride films (which polished at a rate comparable to that of PECVD nitride films although their etch rate in BHF was substantially lower). The reactions between nitride with water, in sequential steps, produced Si–OH, NH_3, and, finally, ≡S–O–S≡ which reacts with water to yield $Si(OH)_4$. This modified surface is assumed to be readily abraded away and also be dissolved in the slurry.

6.19 CMP OF LOW-ε FILMS

6.19.1 Introduction

The components for high-speed, low-crosstalk interconnections, as has been emphasized repeatedly, are (lined) Cu and a low-ε dielectric film. The damascene process is the one of choice. After the barrier layer and Cu are deposited into the patterned dielectric layer, CMP is used to remove completely the excess of Cu and the barrier layer, ideally stopping at the dielectric layer without scratching, delaminating or otherwise changing its properties (e.g., making it susceptible to moisture absorption which increases ε). The lower mechanical strength and hardness of the low-ε films (compared with SiO_2) as well as their chemical properties (unlike those of SiO_2) require modification of the pad or the slurry used in the CMP process or of the film surface, or else the addition of a CMP stop layer (SiO_2, SiC-H, or SiN in the order of increasing ε) to the film stack. Then the decision must be made: should the CMP process be designed to remove all, some, or none of the stop layer?

6.19.2 F-Doped SiO_2

As a result of the incorporation of F into the O–Si–O network, the chemical reactivity is increased and the elastic modulus and hardness are decreased. Thus the removal rate is higher than that of undoped SiO_2 under the same polishing conditions. The removal rate increased as the stress increased. It was suggested that the polish rate is limited not only by breaking the Si–O bonds but also by diffusion of water into the films (Chen et al., 1996). The refractive index of the film

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increased after CMP, presumably due to increased attack by moisture. Capping the F-doped SiO_2 with a Si-rich SiO_2 stabilizes the F and reduces the moisture absorption but increases the capacitance and complexity (and cost) of processing.

6.19.3 Spin-On Films

6.19.3.1 Xerogels

The porosity and low mechanical strength of xerogels have led to capping them with PECVD oxide or nitride films so that they are not exposed to the slurry (Jin et al., 1998). After polishing a single damascene structure using a standard Cu CMP process, the xerogel (Nanoglass) remained intact in areas with a high density of metal lines but there was a significant loss of the Nanoglass in large dielectric areas (Case et al., 2000). It was not clear whether this was due to cohesive failure of the Nanoglass or adhesion failure at the cap/Nanoglass interface. Jin et al. (2000) postulated the Cu lines embedded in the Nanoglass film provide additional mechanical support for them. However, Jin et al. (2000) did not observe delamination after CMP of blanket wafers; in this case the SiO_2-capped Nanoglass was deposited on a thin layer of SiN. It is not clear whether this accounts for the difference in results. They also reported successful polishing of uncapped Nanoglass blanket wafers which they said indicated good mechanical integrity, but they did not state the elastic modulus of the films used in the test.

6.19.3.2 HSQ, MSQ, HOSP

These films have an Si–O–Si backbone. As the organic content increases (from 0% for HSQ to 12% for HOSP and 22% for MSQ) the polishing rate decreases, probably due to the increasing hydrophobic character of the surface. Removal rates in various slurries depended on the abrasive and the pH of the slurry (related to the IEPs). The rates decreased in the order $Al_2O_3 > ZrO_2 > SiO_2$. The hardness of the abrasive and the electrostatic interactions between the film surface and abrasive can explain this result. Despite its higher polishing rate, an Al_2O_3-based slurry was not suitable because of severe scratching of the surfaces. Surfactants may increase the area of contact between the abrasive and the hydrophobic surface of the film but they can change the pH of the slurry and thus the electrostatic interactions so that the rates are, instead, reduced (Chen et al., 1999; Chen and Yen, 2000). Addition of TMAH to the SiO_2-based slurry increased both the polishing rate of MSQ and HOSP and essentially eliminated surface scratching on MSQ (Liu et al., 2001). Exposure of the polished surface of MSQ to an H_2 or an NH_3 plasma restored the dielectric constant to nearly its prepolish value (Liu et al., 2000, 2001).

6.19.3.3 Porous HSQ, MSQ, HOSP Films

These films are softer and have a lower modulus than the films from which they are derived. And so might be expected to have a higher polish rate and more surface damage. The dielectric constant was about doubled after CMP, due, probably, to trapping of water and, perhaps, abrasives and surfactants from the slurry. A post-CMP heat treatment may be adequate to remove the liquids; residual abrasives, however, may remain a problem (Block and Rayle, 2002).

6.19.4 Vapor Deposited α-SiCOH Films

These films have been called C-doped SiO_x, silicon carboxide, and organosilicate glasses, because of the Si–O–Si bonds in the network. The films are sometimes labeled SiOC and, in some fabs, called "SYCO." The reactants and deposition conditions determine the stoichiometric proportions of the

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constituents; thus the film properties can vary from film to film among those called SiCOH. For example, the hardness (*H*) reported for several films ranged from 0.25 to 3–4 GPa (Block and Rayle, 2002; Fayolle et al., 2002; Mountsier et al., 2002; Yau et al., 2000).

One commercially available film, with a small amount of C and a dielectric constant of ~2.9 is CVD Black Diamond (BD) (Applied Materials). The mechanical hardness was the highest of any of the SiOCH films; it was stated to be similar to that of SiO_2 (Lou et al., 1999). The BD film adhered well to SiO_2, SiN, Ta, TaN, etc.; there was no delamination of BD after CMP of Cu deposited on BD. The polish rate, dishing, and erosion (slurry not identified) were comparable to those of PETEOS. There was only a minimal effect of polishing on the electrical properties of the film (Lou et al., 1999; Yau et al., 2000; Wjikoon et al., 2001).

A range of commercially available PECVD films is provided by Novellus Systems under the label of Coral (Jin et al., 2001). One that may be typical has a dielectric constant of 2.85 and a value of *H* of 1.45 GPa (vs. 9 for SiO_2) (Mountsier et al., 2002). The process used for CMP of this film included a high rate abrasive-free step for Cu, a low-abrasive step for TaN_x, a brief buffing step, and a post-CMP clean to remove the slurry from the hydrophobic surface. Minimal erosion was observed; there was localized over-polishing in dense arrays of metal lines and dielectric spacers. The resulting resistance increase was minimal. After fabrication into a Cu/Coral integrated structure, ε was virtually unchanged from its as-deposited value. There was no delamination or cracking of the integrated structures.

CMP could be performed directly on a PECVD SiCOH film containing 20 at% C ($\varepsilon = 2.9$, $H = 1.7$ GPa) film without scratching or change in ε (Fayolle et al., 2002).

Cui et al. (2000) described CMP of a film, CVD "Flowfill low-*k* oxide" which consists of an SiO_2 network incorporating CH_3 groups. The polishing rate in an SiO_2-based slurry decreased as the concentration of CH_3 groups incorporated in the film increased. It was suggested that the CH_3 groups reduce the diffusion rate of water in the SiO_2 thereby reducing the CMP rate of the film. The polish rates of the films were proportional to their etch rates in buffered HF. The film surface was very smooth both before and after polishing, with very few shallow scratches (AFM). Post-CMP cleaning with DI water left the surfaces free of abrasive particles. Only blanket films were examined.

6.19.5 Organic Films

CMP of these softer and chemically stable films challenges the known technology since the process involves reaction with the surface followed by mechanical removal. A hard layer (e.g., SiN or SiCH) may be deposited over the low-ε film to protect it, but this increases the dielectric constant of the interlevel dielectric (partially defeating the benefit of the low-ε film) as well as adding a processing step.

In optimized slurries (designed for CMP of Cu) the rate for BCB was low (45 to 55 nm/min) but (SiLK™) polymer was polished rapidly (300 nm/min, a rate similar to that of Cu). To explain differences in rates, Borst et al. (1999) proposed that the reactivity between the slurry and the polymer structural bonds determined the CMP rate.

A slurry containing no surfactant did not remove either polymer but scratched them heavily. However, with a surfactant, scratching and surface roughening were minimal. There was a latency period in CMP of BCB. Borst et al. (1999) suggested that this may be due to the time needed for adsorption of the surfactant on the surface of the polymer and abrasive particles. The oxygen content of the surface layer (>10 nm) increased significantly. The low rate may be due to "a lack of a polymer-weakening surface reaction or to the formation of a protecting passivating layer (due to surfactant adsorption and oxidation) which inhibits mechanical removal." They characterized the CMP of BCB as "controlled abrasion."

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There was no latency period in CMP of SiLK; the oxygen content of the surface layer (>10 nm) was increased. "The increased removal rate and absence of a latency period suggest a rapid chemical reaction at the SiLK surface, which breaks structural bonds to form an altered layer" easily removed by shear and abrasion. This process was characterized as "synergistic chemical/mechanical CMP."

CMP of blanket films of BCB was also compared with that of parylene N (PA-N) films using Al_2O_3-based slurries at several pH values, with and without the surfactant Triton X. For both polymers (1) the composition of the slurry will affect the quality of the polished film, (2) the quality of the film before CMP will affect the quality of the polished films, and (3) CMP depends on the different structures, i.e., the weakest bonds of the polymer films. The differences between them are: (1) the surface structure BCB but not PA-N films is very sensitive to polishing time, (2) the morphology of PA-N films both before and after CMP is not as good as that of BC, and (3) a different slurry must be used for each film in order to produce the highest rate and best surface quality (Yang et al., 1997).

The polish rate and surface smoothing of polyarylether (FLARE) films were substantially higher in MnO_2 and Mn_2O_3 slurries than in an SiO_2-based one. The rate increase was attributed to a chemical reaction at the surface of the polymer layer. To prevent peeling from the TaN barrier layer, low pressure was used in CMP. The polish rate of the organic layer was, however, somewhat higher than that of the barrier layer (Hara et al., 1999). Since the aim in polishing the damascene structure is to preserve the interlevel dielectric, the usefulness of this process is doubtful.

6.19.6 Porous Organic Films

Among the spin-on films that have been studied are XLK™ (porous SiLK™) and ELK (porous poly(arylene ether)). Typically such films are covered with a cap layer such as SiO_2 or Blok™ for protection during CMP; this requires excellent adhesion between the PECVD and SOD films.

One advantage cited for ELK films is that an edge bead removal process is used; this helps reduce edge peeling. In one process (Wijekoon et al., 2001) both SiO_2 and Blok™ layers were used as dual caps; the CMP process was designed to remove only the top layer.

6.20 CMP OF METALS

The basic concept of CMP of metals is shown in Figure 6.20 (Kaufman et al., 1991). The formation of the passivating film is an oxidation reaction and thus slurries used for metal CMP contain an oxidizer; among these are H_2O_2, HNO_3, $K_2Cr_2O_7$, $KMnO_4$, KIO_3, $K_3Fe(CN)_6$, and $(NH_4)_2Ce(NO_3)_6$.The slurry must be constituted so that chemical etching (corrosion) of low areas is inhibited (ideally prevented) and the passivating layer on the high spots readily abraded or dissolved while leaving the surface free of defects.

CMP is used most frequently to remove the excess of metal in a recessed metal (damascene) process. Figure 6.30 compares dielectric and metal planarization processes.

The CMP processes to be covered are those for W plugs and Al(Cu) and Cu interconnections. Since these metals are encapsulated in a liner/barrier layer, after the bulk of the metal is removed, the underlying films must also be removed. Although Kondo et al. (2000) suggested the use of RIE for this purpose, CMP is preferred for simplicity and process compatibility. Thus, the question arises whether a single step is adequate or whether clearing the bottom layer requires a change of process.

Since corrosion and the formation/dissolution of passivating films on metal surfaces are electrochemical reactions, electrochemical measurements have been used to elucidate and optimize

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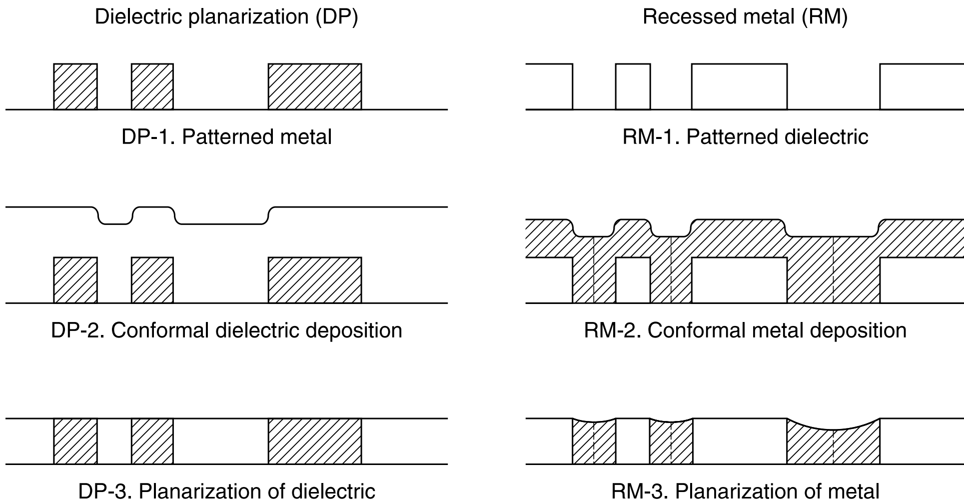

Figure 6.30 Comparison of (left) dielectric and (right) metal planarization processes.

the chemical aspects of CMP of metals, i.e., the chemical components of the slurry and their interaction with the metals being polished. These involve the use of Pourbaix diagrams (pH–potential diagrams) and potentiodynamic polarization (potential vs. current density) data. An excellent exposition can be found in Steigerwald et al. (1997).

6.20.1 CMP of Tungsten

CMP has replaced etchback by RIE of the CVD W plugs (mentioned in Section 6.14.1.3) in a single damascene process. Tungsten is a hard metal, unlike Al and Cu, so that scratching is expected to be minimal. This property has led to the use of W caps on Al and Cu to prevent scratching when these metals are polished (e.g., Joshi et al., 1994).

Steigerwald et al. (1997) have reviewed the early work on CMP of W.

Many oxidizers have been used in the process, e.g., $K_3Fe(CN)_6$, KIO_3, H_2O_2, $NH_6Mo_7O_{24}$, $Fe(NO_3)_3$, KNO_3, $(NH_4)_2S_2O_3$, and $Ce(NO_3)_4/HNO_3$. Ferric nitrate is a very aggressive oxidizer and $NH_6Mo_7O_{24}$ very protective (Kneer et al., 1997). Although addition of H_2O_2 resulted in rapid repassivation, the film was porous since H_2O_2 dissolves W (Kneer et al., 1996). The complexing agent used was ethylene diamine. The abrasive is usually colloidal alumina and the pH between 2 and 4.

The passive layer formed on W is a duplex oxide WO_2/WO_3; the passivation is due primarily to WO_3. The oxide layer formed in KNO_3 at $pH = 2$ is a better passivant than the one formed at $pH = 4$ (Kneer et al., 1996). Electrochemical measurements were performed during CMP (Kneer et al., 1997); an increase in the corrosion current density during abrasion was measured, which, the authors said, was an indication that a highly protective layer was being removed. The dissolution rates of W determined from electrochemical measurements, however, were a very small fraction of the typical rates during CMP of W. The conclusion was that oxidation + oxide abrasion and dissolution may not be the primary mechanism for W CMP, but that corrosion-assisted fracture (observed by AFM scans) may be important as well. On the other hand, Stein et al. (1998) also making electrochemical measurements during polishing, stated that although "passive film formation was found to occur in several oxidizing slurries in the absence of polishing, there was no evidence of passive film formation on W during polish." Since the polish rates were much higher than expected from

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electrochemical measurements during polish, they concluded that "the removal mechanism of W during CMP does not require a blanket passive film or the oxidation of all the removed W." But what protects the low-lying features?

Paul (2001b) applied his model (see Section 6.17.3) to W CMP in terms of the oxides of W and the interactions between slurry and substrate and was able to show the dependence of the experimental polishing rate on the concentration of chemicals and abrasives in the slurry.

Turning away from the question of a protective layer, Stein et al. (1999a,b) examined the chemical and physical interactions between the surfaces of the colloidal abrasive species and the W surface and reported they played an important, complex role in the mechanism of W removal in CMP, some of which were also mentioned by Paul (Section 6.17.3).

Uniformity of polishing was improved by reducing the backside pressure (larger pad-to-wafer gap) so that slurry transport was enhanced (Zabasajja et al., 2001).

Erosion in a $Fe(NO_3)_3$ slurry of W inlaid in an oxide matrix increased linearly with polishing time and nonlinearly with pattern factor. Dishing depended on the type of oxide, pattern factor, and groove width, but not on overpolish time if the selectivity between the W and oxide is large and the pad becomes more relaxed as dishing proceeds (Elbel et al., 1998). Van Kranenburg and Woerlee (1998), however, reported that a large percentage of not only the final erosion but also of dishing was generated during overpolishing.

Whatever the underlying mechanism is proved to be, practical procedures have been developed and implemented on the production line (e.g., Wijekoon et al., 1998).

6.20.2 CMP of Aluminum (Alloys)

When the dual damascene process was introduced, Al alloys were the interconnection and SiO_2 the interlevel dielectric. The processes developed "provide an evolutionary path to Cu dual damascene" (Iggulden et al., 1998). The metals were deposited by a combination of CVD and PVD designed to fill the features etched in the interlevel dielectric without voids or seams. In 2000 it was argued that the process was viable for 0.175 μm DRAMs and beyond (Schnabel et al., 2000).

Slurries for polishing Al usually contain alumina particles and an oxidizer; the pH is in the acid range.

Aluminum is a very soft metal (~2 on Mohs' scale). Early attempts at polishing Al were hampered by scratching of the surface and corrosion. Whereas a soft pad might limit that damage, it might also result in dishing and erosion of the interlevel dielectric. Nevertheless, success has finally been achieved. It is believed that the hard Al_2O_3 (~9 on Mohs' scale) layer that forms on the Al surface during polishing makes it possible to polish Al films (Wrschka et al., 1999.). Larger removal rates correlated with thinner Al oxide films. The surface film is the same material as the abrasive; if it is not removed completely by abrasion or dissolution but stays suspended in the slurry, it can scratch the metal surface.

The need for etchants in the slurry was emphasized by Kallingal et al. (1998) who used $K_2Cr_2O_7$ to form a thick passivating layer. They argued that it was necessary to dissolve the abraded particles in the slurry volume near the surface in order to obtain a smooth and clean surface.

Although an oxidant has been considered a necessary ingredient of the slurry for CMP of Al, Hernandez et al. (1999) reported that a strong oxidizer, such as H_2O_2, in the slurry had almost no effect on the removal rate. It was not needed to form a protective oxide layer which would form upon exposure to air and water.

Thus far only pure Al has been discussed but AlCu alloy as well as Ti/TiN layers are used to enhance the electromigration performance. The slurries can polish these metals as well, although sometimes a two-step process is used. In the process reported here, a silica slurry was used in the second step. Between steps the pad was changed, the flow of slurry stopped, and water introduced to the polish pad. After polishing the Ti/TiN pits were observed on the surface near Al_2Cu precipitates.

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These can act as cathodic sites for corrosion of adjacent Al sites where the passivation may be defective due to the presence of Cu. Floating wires were less likely to have pits. Benzotriazole (BTA), a corrosion inhibitor, added to the step two slurry or to the DI water in the water–polish step, eliminated the pitting (Lin et al., 1999). In addition, Cu plated out on the Ti layer when the alloy was polished in a neutral silica slurry. Ronay (2001) reported that adding $(NH_4)_2Ce(NO_3)_6$ as the oxidant in an alumina slurry at pH = 2 prevented the plating. The explanation offered was that the oxide thus formed during CMP was a mixed Ce–Al oxide, less dense and able to incorporate the Cu ions. Addition of Ce ions increased polish rate of the Al; this was attributed to the weakening of the oxide. Although an oxidizer had no effect on the CMP rate of Al, it drastically increased that of TiN which dissolves in it (Hernandez et al., 1999).

6.20.3 CMP of Cu

The increasing use of Cu interconnections formed by the damascene process has heightened the importance of CMP of Cu. Many of the studies of the process are of the Cu/SiO_2 system and are concerned with the selectivity $Cu:SiO_2$, despite the decreasing use of the higher ε interlevel dielectric. Cu is harder than Al but softer than W; therefore Cu will not scratch as easily as Al but will abrade more easily than W. Although Cu is more noble and oxidizes less readily than either, there are several oxygen-containing films, Cu_2O, CuO, $Cu(OH)_2$, that may form on the Cu surface in various slurries depending on the conditions.

Among the slurries that have been used are NH_4OH, $NH_4OH + K_3Fe(CN)_6$ (Steigerwald et al., 1995), neutral glycerol (CH_2OHCH_2OH) (Kumar and Murarka, 1996), H_2O_2 + glycine (NH_2CH_2COOH) (Hirabayashi et al., 1996), HNO_3 + BTA (Steigerwald et al., 1997), H_2O_2 and a phthalic acid salt, i.e., phthalate anions ($R–COO^-$) (Hernandez et al., 2001), and KIO_3 (Hsu et al., 2002). Both alumina and silica abrasives have been used successfully.

Although Cu can be polished in NH_4OH slurries, addition of $K_3Fe(CN)_6$ to an alumina-based slurry increased the polish rate significantly. In this mixed slurry a surface film, thought to be $[Cu_3Fe(CN)_6]$, forms rapidly, protecting the low areas from dissolution. The complexing capability of NH_3 ensures the dissolution of the abraded material. A surface film does not form in HNO_3 but addition of BTA provides an effective protective layer on the low regions while enhanced etching by HNO_3 in the abraded high areas yields high polish rates and planarity. In the neutral glycerol slurry the polish rate depended on the abrasive size (higher rate with a large particle) and the concentration of glycerol (reaching a maximum at an intermediate concentration, depending on the particle size). The size effect was explained in terms of the energy imparted to the grinding process. The maximum in the rate was explained by a complex interplay among the dielectric constant, pH, and viscosity. According to Aksu and Doyle (2002), " a complexing agent such as glycine would be expected to improve the planarization efficiency by promoting a higher electrochemical dissolution rate from surfaces freshly exposed by abrasion." The role of phthalate anions in alumina-based H_2O_2 slurries to complex the cupric species produced as a result of the applied stress. In this slurry CuO and $Cu(OH)_2$ were detected on the polished surface. The removal of Cu was said to be limited primarily by the oxidation rate of Cu, which depended on the concentration of the oxidizer, and the solubility of a cupric film (Hernandez et al., 2001). In a silica slurry formulated with KIO_3 as the oxidizer, at acid pHs the passivating layer was CuI and in alkaline slurries, where the polishing rate was significantly reduced, it was the more protective layer of Cu_2O (Hsu et al., 2002).

The process was reported to follow the Preston equation, indicating its pseudo-mechanical nature (Steigerwald et al., 1997; Gotkis et al., 1999). On the other hand, Stavreva et al. (1997) reported that "polishing pressure had no impact on the planarization rate" but that low velocities were to be avoided because this would lead to a slower planarization rate. Wrschka et al. (2000) reported that the removal rate (RR) $= kp^a v^b$ where a and b were < 1, $a \sim ½b$ in alumina, and $a \sim b$ in silica slurries; b was about the same in both slurries. They concluded that the high selectivity $Cu:SiO_2$ and the low polish rate of SiO_2 indicated that while SiO_2 removal is dominated strongly by

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mechanical abrasion in this slurry, Cu is not. Evidence of a strong chemical contribution to the process is its sensitivity to temperature (Chiou et al., 1999; Sorooshian et al., 2004).

The presence of the liner, almost universally Ta/TaN, poses a serious challenge for planarizing the metal stack since Ta and TaN are hard and chemically inert. Ta is oxidized readily and the oxide, Ta_2O_5, is highly protective. The highest CMP of Ta was obtained using a slurry of abrasives in DI water. Addition of an oxidant decreased the polish rate, possibly due to an increased thickness of the hard-to-remove oxide film. In an alumina-based slurry, a low Ta polish rate equal to that of Cu was realized in a DI water slurry. As the alumina particle density increased, both rates increased, with the Cu rate increasing more rapidly. Silica abrasive had a higher polish rate which suggested that there may be a chemical component (Hariharaputhiran et al., 2000). The polish rate was affected by the pH of the slurry; it was a maximum at pH $=$ 3.5 in a silica slurry and at pH $=$ 8 in an alumina slurry. This was attributed to variations in electrostatic interactions between the abrasive particles and the oxide-coated Ta surface, determined by zeta potential measurements. The rate maxima occurred when the abrasive particles and the surface were oppositely charged. Increasing the ionic strength of the slurry by the addition of a salt decreases the polish rate at pH values where the particles and the surface are oppositely charged and increases at pH values where the surfaces have the same charge (Ramarajan et al., 2000).

There appears to be a consensus that a multiple step/multiple slurry process is required. Two approaches have been considered for the second step: (1) a highly selective process, stopping at the barrier and then using a barrier-selective slurry/pad combination or (2) a nonselective approach, stopping as soon as or immediately after the barrier is exposed and then polishing the Cu/interlevel dielectric/barrier at equal rates to clear the barrier. The integrity of the barrier layer during CMP must be maintained; this is difficult since it is very thin to avoid a large increase in resistance. Slurries that attack the barrier layer chemically do so by reacting with the Ta and TaN but not with the oxide, proceeding through defects in the oxide layer, so that scratching, layer cracking, etc., occur (Gotkis et al., 1999). Thus the safest approach is to remove the barrier mechanically.

The concept of a selectivity switch was proposed by Gotkis et al. (1998, 1999). When the field Cu was removed, the slurry and processing was switched from one in which the Cu polished at a high rate, but was very selective with respect to the interlevel dielectric and the barrier, to a different slurry with considerably lower Cu:barrier selectivity ($s < 1$ is the best case) using a hard pad and low polishing pressure. This requires reliable endpoint detection to switch processes at the right time. A two-step process uses an alumina-based slurry to remove all the Cu, stopping before the liner is removed completely. In the second step, a neutral pH silica-based slurry, selective to the barrier, removed the remaining film (Landers et al., 1997).

Another problem arising from the use of a Ta barrier is that, at some point in the CMP process, Cu and Ta will be exposed to the slurry at the same time, while electrically connected, forming a short circuited electrochemical cell. This can result in anomalous Cu dissolution and extreme pattern dependent polishing (Evans, 1996).

6.20.3.1 Modification of CMP of Cu

6.20.3.1.1 Abrasive-Free (AF) (Slurry-Free Polishing in a CMP Apparatus)

There are several variants of this technique. There is no abrasive in the polishing solution; this has led to the terminology slurry-free, implying an abrasive-free polishing solution is not a slurry. The advantages cited for all of them were cleaner post-CMP surfaces (easy post-CMP cleaning) and less dishing and erosion. Kondo et al. (2000) used a standard CMP apparatus with a foamed polyurethane pad. The polishing solution contained an etchant, and a corrosion inhibitor (not identified) and the oxidizer, usually H_2O_2.The removal rate increased and the within-wafer-nonuniformity (WIWNU) decreased with increasing down force and platen speed, eventually approaching a

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constant value. The maximum removal rate of Cu was ~180 nm/min and the WIWNU $<12\%$. The polished surface was very clean (postcleaning only with water brush-scrubbing needed), scratch free, and corrosion resistant. The total depth of erosion and dishing after 100% overpolishing was reported to be about one fifth of that obtained with conventional CMP.

The mechanism proposed was the formation of an oxidized surface protected by an inhibitor which is removed by soft friction with the pad and then the oxide is dissolved by the etchant. The AF process automatically stopped when the barrier metal was reached; it was then etched in an ICP reactor. The protection layer must be able to be removed by the pad but at the same time protect recessed regions from the etchant. Additional advantages of AF processing were a possible reduction in cost (consumables and waste disposal) and particle reduction (possibly elimination).

Nguyen et al. (2001) used the term slurry-free. A fixed-abrasive pad was used in a standard CMP apparatus; the polishing solution contained an amino acid as a complexing agent as well as H_2O_2. The pH of the solution as well as the concentration of H_2O_2 were important factors. The best results (346 nm/min, no SiO_2 removal and WIWNU = 3%) were obtained at a pH of 3 and a concentration of H_2O_2 of 15 vol%. The dependence of the Cu removal rate on pattern density and feature size, and dishing, was less than that for conventional CMP. They also noted the ease of post-CMP cleaning. Ohashi et al. (2001) emphasized the role of the corrosion inhibitor but, unfortunately, did not identify it. They found that the residue resulting from the difference in plated Cu film thickness in high and low-density patterns could be eliminated.

6.20.3.1.2 Mixed Abrasive Slurries

This concept is described in Section 8.18.2.2. A slurry consisted of 2.5 wt% colloidal silica (better performance than fumed silica) and 0.5 wt% alumina in DI water (with KOH/HCl for pH adjustment). The polish rate of Ta was high and that of Cu and oxide was low; thus this slurry is a potential candidate for the second step of Cu polishing, i.e., for removal of the barrier layer (Jindal et al., 2002).

6.20.3.1.3 Abrasive-Free Micelle Slurry

The micelle slurry is based on a mixture of a surfactant and a heteropolyacid (HPA); an example is a nonionic detergent, such as PEG, plus the HPA vanadmolybdic acid. HPAs are strongly oxidizing and strongly acidic and thus excellent etchants of Cu. By enveloping the HPA in a surfactant, which takes the form of micelles in water, there is no reaction with Cu in the absence of applied pressure. The micelles are expected to deform under applied pressure, exposing the raised Cu surface to etching by the HPA. The recessed areas will be relatively free of such exposure, as illustrated in Figure 6.31. Polishing can thus be said to occur by a chemical reaction with little or no mechanical abrasion. Since this can be accomplished using minimum pressure, dishing, scratching, and erosion should be minimal.

It was reported that the polishing rates, at low pressure with a nonfoamed hard pad, were very high. Pad dressing was unnecessary; this means increased pad life, reduced process costs, and simplification of the process (Matsuda et al., 2003). The ability to achieve high polish rates at low pressure makes the slurry attractive for polishing Cu/low-ε structures.

6.20.3.2 Alternatives to CMP of Cu

6.20.3.2.1 Introduction

The advantage cited for most these alternative planarization processes is that they do not involve direct contact between the surface being planarized and a polishing pad and thus are more compatible with the low-ε films which have reduced resistance to the mechanical component of CMP.

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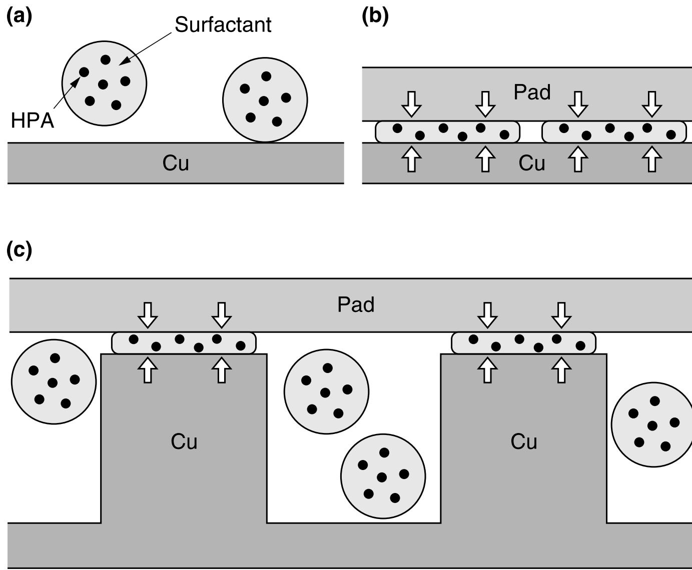

Figure 6.31 Conceptual configuration and polishing mechanism of the micelle slurry: (a) no applied pressure, (b) deformation by polishing pad, (c) difference between raised and recessed regions during polishing. (Reproduced from Matsuda, T., H. Takahashi, M. Tsurugaya, K. Miyazaki, T.K. Doy, and M. Kinoshita, *J. Electrochem. Soc.*, 150, G532, 2003. With permission of the Electrochemical Society, Inc.)

6.20.3.2.2 Electrochemical Planarization (ECP)

This technique was first described by Contolini et al. (1994) for use in electronic packages and then in 1997 for ULSI devices. After cathodic plating of Cu into the features etched in the interlevel dielectric, anodic electropolishing is carried out "to remove protruding surface features at a faster rate than those in valleys or crevices." A viscous electrolyte, H_3PO_4, is used in ECP. "The highest, sharpest features stick up through the boundary layer and dissolve more rapidly than recessed ones." To avoid overetching, they terminated the process before completion and removed the remaining Cu in a wet etch.

Excellent electropolishing was achieved using concentrated H_3PO_4 in the mass-transfer-limited plateau region (i.e., the region in which the current density remains essentially unchanged as the applied voltage is varied (Chang et al., 2002). They concluded (from XPS and electrochemical impedance spectroscopy) that the presence of a passivating film on the Cu surface contributed to the microleveling effect and smoothness of the surface. The drop in the current as polishing proceeds indicates the endpoint for Cu polishing and the exposure of the barrier. Padhi et al. (2003) reported that process parameters such as current density, rotational speed, and flow rate influence planarization. A resistive viscous boundary layer, which requires a finite amount of dissolved Cu to form, is necessary for polishing to occur. The amount of Cu dissolved before its formation decreases with increasing current density; to minimize etching before polishing, high current densities are required. If the speed of rotation of the wafer was too high, center to edge uniformity was degraded. If it was too low bubbles were trapped. Planarization and uniformity were achieved when the flow rate was high enough to push the electrolyte over the polishing chamber.

What was termed "superpolishing" with a high planarization efficiency was achieved by the addition of citric acid to the H_3PO_4 which increased its conductivity. PEG was added to increase the overpotential of O_2 formation and thus avoid the formation of etch pits (Chang et al., 2003). It was proposed that a concentration gradient of citric acid results in a dissolution gradient, i.e., a higher removal rate on the outside of a feature than on the inside, leading to planarization.

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6.20.3.2.3 Spin-Etch Planarization (SEP)

This is a noncontact, nonslurry process in which the metal is removed by exposure to a reactive chemical solution (ingredients not given) while the substrate is spinning. The wafer is suspended horizontally on an N_2 cushion above a rotating chuck. The wafer is held in place laterally with locking pins on its edge. As the chuck and wafer are spun the etchant solution is dispensed onto the wafer. A proposed 2-step process for Cu/barrier included (1) use of an etchant selective to Cu and (2) selective passivation of Cu and use of an etchant with a high selectivity to the barrier layer. There are no particulates in the etchant and there is no mechanical contact with any solid. The wafers are cleaned and dried by exposure to DI water and N_2 with no need for scrubbing. This technique is "inherently applicable to surface that have a low modulus or low abrasion resistance" (DeBear et al., 2000; Mukherjee et al., 2000).

6.20.3.2.4 Reactive Ion Planarization (RIP)

This technique, based on a thermodynamic analysis of the Cu–Cl system, was proposed for both low-temperature RIE and for planarization as alternatives to CMP (Kulkarni and DeHoff, 2002). It depends on the volatilization of metastable $CuCl_2$-Cu_3Cl_3(g) in the presence of H_2. The reactions are:

$Cu + Cl_2$ ($\leq$25°C, HD plasma) $\rightarrow CuCl_2 + CuCl$

$CuCl_2 + H$ (formed in plasma) $\rightarrow Cu_3Cl_3$ (g)

Subject newly exposed CuCl layer to Cl_2 plasma $\rightarrow CuCl_2$

Repeat (2)

To be useful for planarization the surface features should etch in the following order: convex > flat > concave. This does occur because "the chemical potential of Cl_2 on convex $CuCl_2$ gas interfaces is increased in relation to flat interfaces while that on concave interfaces is reduced." The technique was merely proposed; there were no experiments performed to demonstrate its practical value.

6.20.3.2.5 Electrochemical Mechanical Deposition (ECMD)

This process involves simultaneous ECD and mechanical polishing of the surface. The Cu layers grow preferentially in cavities so that flat profiles result. Once bottom-up filling of high-AR features is complete, mechanical action is initiated to arrest overplating of small features and accelerate growth within large features, resulting in a flat profile with a much smaller overburden than that of conventional ECD (Basol et al., 2002). It does not have the better compatibility with low-ε films as do the others mentioned above.

6.21 POST-CMP CLEANING

CMP is a dirty process so that effective post-CMP cleaning is an essential part of the overall process. The cleaning procedures and the chemicals used must not damage the finished wafer and must accommodate a wide variety of materials, i.e., insulators and metals, as well as forces, i.e., electrostatic, van der Waals (physisorption), capillary, and chemical bonding.

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The contaminants include particles from the slurry, the pad, or the abraded surface, chemical residues from the slurry, adsorbed species, etc. These adhere to the surface or are embedded in it.

Although Cu is contained within the device by barrier layers, if Cu particles generated during CMP are not eliminated, they can produce serious damage to Si devices, since Cu diffuses readily through Si and dielectric layers and can reduce minority carrier lifetime, compromise field and gate oxide integrity, and cause high leakage currents between adjacent conductors.

Cleaning immediately after polishing is important since particle adhesion strength increases with time (Burdick et al., 2003). Keeping the wafer wet or out of the air flow can minimize contamination from the environment. The forces that act on the particles play a role in contamination. As noted earlier, if the surface and particle have like charges (by adjusting the pH of the slurry at or near the endpoint), repulsive forces will reduce contamination.

HF-based cleaning is used to remove ionic and metallic contaminants. Drying problems associated with surface heterogeneity (e.g., hydrophilic oxide, hydrophobic Cu) as well as pattern dependent corrosion of Cu structures not connected to the substrate were reported by Fyen et al. (2000). They also found that, after the spin-rinse and dry cycle when using an alumina-based slurry, the particles redeposited at the edge of and on the Cu lines.

Surfactants, to reduce surface tension, and megasonic cleaning in various solutions to remove particles, and the use of a secondary platen buff process are other procedures that have been used.

Cooper et al. (2001) suggested that the applied load be reduced near the end of polishing, using a buffing step to follow primary polishing. This would remove particles embedded earlier but not likely to add significant numbers of new ones. Mechanical force has been found to be a necessary component of the particle removal process. In a study of a single-sided brush apparatus, Burdick et al. (2003) found that "hydrodynamic forces can remove some of the adhering particles from wafer surfaces, but brush–particle contact must occur for complete particle removal.

Double-sided scrubbers, in use since the early days of CMP, clean both sides and the edges at the same time, while rotating the wafers. After scrubbing, high-speed spin stations spray both sides of the wafer which is then dried (Krusell et al., 1995).

A noncontact method for removing particles uses ultra high frequency ($>$850 kHz), i.e. megasonic agitation of the cleaning bath. The technique was reported to be highly efficient and to perform as well or better than brush methods (Morrison et al., 1997; Olesen and Franklin, 1998).

Another source of Cu contamination is the exclusion zone in plating and at the bevel edge. This is a problem in addition to those resulting from CMP since the Cu can be transferred to wafer carriers and then to other wafers. Spin-etch cleaning (Lysaght and West, 1999) has been proposed as a method or dealing with this problem A chemical etchant (a mixture of acids) is dispensed from a radially oscillating overhead nozzle onto the backside of a spinning wafer held frontside down by an N_2 cushion; there is a wraparound effect that removes contamination from the bevel and front side.

All of the cleaning procedures, as well as CMP itself, generate huge amounts of waste liquid whose disposal adds significantly to the cost of device fabrication.

6.22 PROBLEMS WITH CMP

6.22.1 Nonuniformities

There are several kinds of nonuniformities that must be minimized (if not entirely eliminated) in order to produce reliable devices.

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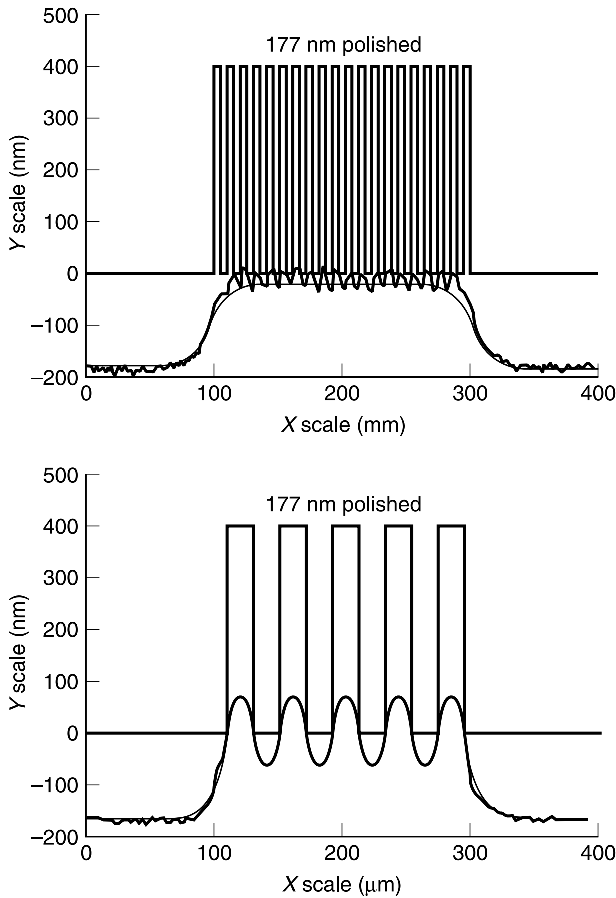

Figure 6.32 Influence of pitch on polishing results. Top: 5 μm × 5 μm; bottom: 20 μm × 20 μm. (Reprinted from Ali, I., S.R. Roy, and G. Shinn, *Solid State Technology*, 10/94, 63, 1994. With permission.)

Although CMP has been described as a process for achieving global planarity, pattern sensitivity does exist. The polish rate of a feature can be influenced by the topography of surrounding features (Warnock, 1991). The initial rate of material removal depends on the width of the feature. At the start of the process, raised features are polished at a greater rate than recessed areas (the basis for planarization). As polishing continues, decreasing the step height differential, the rates tend to become equal (Renteln et al., 1990). Narrowly spaced features are polished at a greater rate than widely spaced ones as seen in Figure 6.32. Small isolated raised features polish at a higher rate than groups of features, and wide gaps are polished at a higher rate than small ones as illustrated in Figure 6.33. This figure also shows the rounding of the edges of lines (due to higher local pressure), although harder pads tend to produce less and more gradual corner rounding than soft pads (Burke, 1991). The influence of structure size on the final polish result is shown in Figure 6.34.

The polish rate of blanket films is often used in preliminary experiments to determine the processing parameters and as a rate monitor; it is equivalent to that of a large raised area.

Large raised features and large recessed areas polish at about the same rate as a blank film (or background). The intrinsic high polish rate of raised features and nonpolishing of depressions is not realized in these cases and, therefore, planarization by just polishing is extremely difficult. Further,

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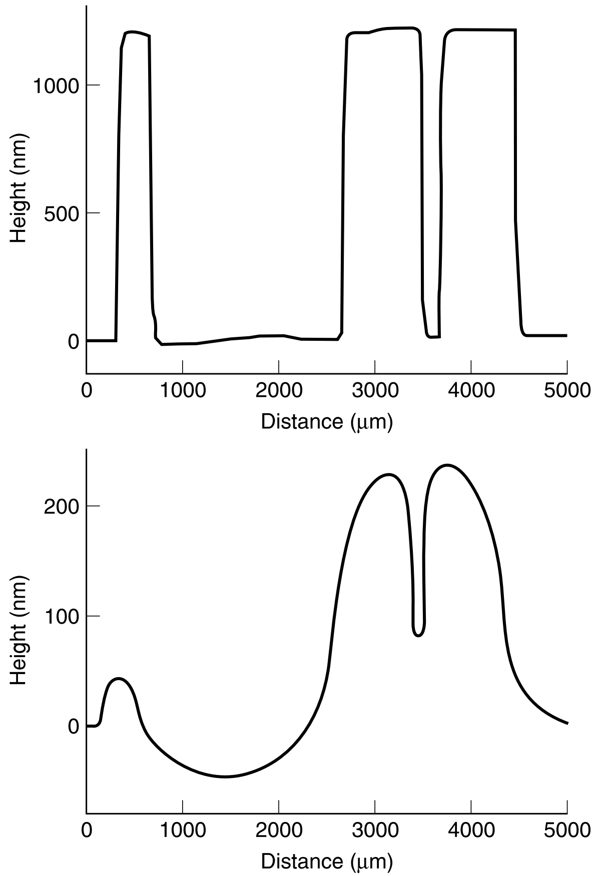

Figure 6.33 Effect of feature spacing on polishing rate and rounding of edges of lines. Top: before polishing; bottom: after polishing. (Reprinted from Sivaram, S., H. Bath, R. Leggett, A. Maury, K. Monnig, and R. Tolles, *Solid State Technol.*, 5/92, 87, 1992. With permission.)

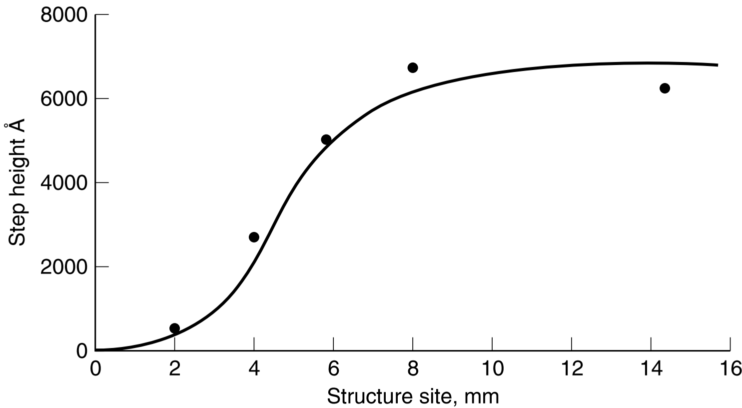

Figure 6.34 Step height vs. structure size. (Reproduced from Morimoto, S., R. Breivogel, R. Gasser, S. Louke, P. Moon, R. Patterson, and M. Prince, *Electrochem. Soc. Proc/PV 93-1*, 449, 1993. With permission of the Electrochemical Society, Inc.)

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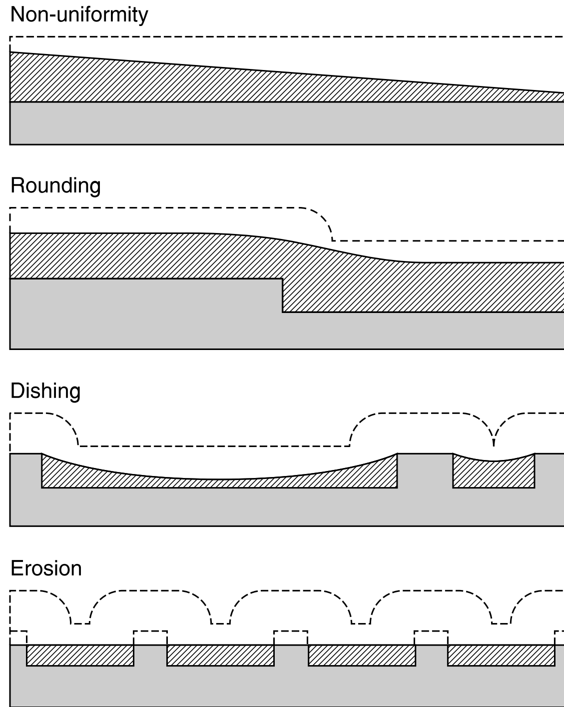

Figure 6.35 Some limitations of CMP: (1) nonuniformity, (2) rounding, (3) dishing, (4) erosion. (Reprinted from Landis, H., P. Burke, W. Cote, W. Hill, C. Hoffman, C. Kaanta, C. Koburger, W. Lange, M. Leach, and S. Luce, *Thin Solid Films*, 220, 1, 1992. With permission. Copyright 1992, Elsevier.)

clusters of closely spaced narrow features act as a large feature, with a corresponding slower polish rate, which also works against achieving global planarization.

Landis et al. (1992) described other limitations as well, illustrated in Figure 6.35 (the original surfaces are indicated by dotted lines). (1) Nonuniformity arises from polish-rate variations across a wafer. Nonuniformity from center to edge can be minimized by shaping or contouring template or carrier (Currie and Schulz, 1993). Variable backside pressuring of the wafer was reported to improve polish uniformity as well as pad lifetime (Jansen and Hanestad, 1996). (2) Rounding of corners, usually seen in oxide polishing, occurs because the protruding corners are overloaded and convex while recessed corners are underloaded and concave. Rounding is governed by the pad's ability to adjust itself to the topography of the wafer surface and is determined by the hardness of the pad, loading condition, and relative motion (Gotkis et al., 1998). (3) Dishing refers to the thinning of the fill material in the center of a wide inlaid feature; it is commonly associated with the use of soft pads which can bend slightly into recesses (e.g., Steigerwald et al., 1994), although Wrschka et al. (2000) related dishing during CMP of Cu in H_2O_2/acid slurries to a chemical etch. Fu et al. (2003) showed that dishing is more severe in a line than in a bond pad even when the linewidth and the side length of a square pad are the same. This effect was stated to be due to the fact that the polishing pad is restricted over all sides of the surrounding area but only on two sides in the case of a line. The roughness of the polishing pad was also a factor in determining the extent of dishing (Nguyen et al., 2003). (4) Erosion of the dielectric layer in which the metal is embedded is most severe when the trench area fraction is high or when the polish selectivity is low.

Dishing and erosion are often found to be worsened by overpolishing.

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The severity of these effects can be reduced by modifying the process or reducing the variation in the pattern density. Instead of changing the chip layout, difficult to implement since it involves changing the chip design, several approaches, said to be successful and have wide acceptance are: (1) dielectric dummy fill approach, i.e., support wide metal lines with embedded pillars of dielectric, (2) metal dummy fill approach, i.e., create dummy metal features in the dielectric to increase the uniformity of a densely patterned circuit (Pan and Li, 2000), and (3) step-to-edge approach, i.e., print partial dies at the wafer's edge to minimize or eliminate the effect of the transition from flat dielectric to patterned (Smekalin et al., 2001). Mosig et al. (2002), however, have pointed out that unconnected metal parts of the dummy fill may have an undefined electrical potential, possibly having a detrimental effect on high frequency behavior. They also noted the positive effect of the dummy fill, i.e., increased heat conductance.

6.22.2 Defects

Although CMP has been used successfully in the fabrication of high-performance devices, defects introduced during CMP have been observed:

- Metal roughness.
- Residual passivating films on metals: lead to high contact/via resistance (unless removed by sputtering or etching).
- Residual slurry particles.
- Alkali ion contamination. Can be minimized by using non-K^+ slurry.
- Microcracking of insulator due to stress-induced diffusion of water into oxide. Can be minimized by use of softer pads.
- Scratching of oxide surface (possibility of metal deposition into scratches causing shorts when metal is etched by RIE but not when metal removed by CMP (Figure 6.36).
- Corrosive attack by slurry, leads to pits, metal thinning.
- Gouging.
- Uniformity degradation with increasing pad use.
- Scratches in metal surfaces. Can be removed from Cu films using a chemical solution without or with a very small quantity of abrasive (Hegde and Babu, 2003).
- Metal thinning during removal of a liner/barrier layer (Gotkis et al., 1999).
- Missing metal; galvanic enhanced corrosion due to, for example, simultaneous exposure to the slurry of the barrier layer and Cu (e.g., Zeidler et al.,1997; Ernur et al., 2000) or Al(Cu) (Lin et al., 1999).
- Photocorrosion: anodic corrosion observed only after the electrodes connected to active devices are electrically separated from each other by CMP. The positively biased electrodes corrode rapidly in diluted slurries, even with added BTA. Leads to pattern-specific corrosion. "Source of the positive potential by the p–n junction is exposure to light during processing" (Homma et al., 2000).
- Plate-out of Cu during CMP of Al(Cu) on Ti liners. Can be eliminated by changing oxidant (Ronay, 2001).
- Delamination at film interfaces: notably at low-ε interlevel dielectrics/cap layers.

6.22.3 Usage and Disposal of Water

CMP requires enormous amounts of water in the polishing slurries and in the cleaning processes. According to information cited by Belongia et al. (1999), approximately 30 to 50 liters of dilute waste slurry may be generated for each 200 mm wafer for each level of planarization. Recycling the DI water eliminates (or at least reduces) the disposal problem and decreases the need for new water. The solids must be separated from slurries in which they are suspended in order to recycle the water. Electrodecantation and electrocoagulation were demonstrated by

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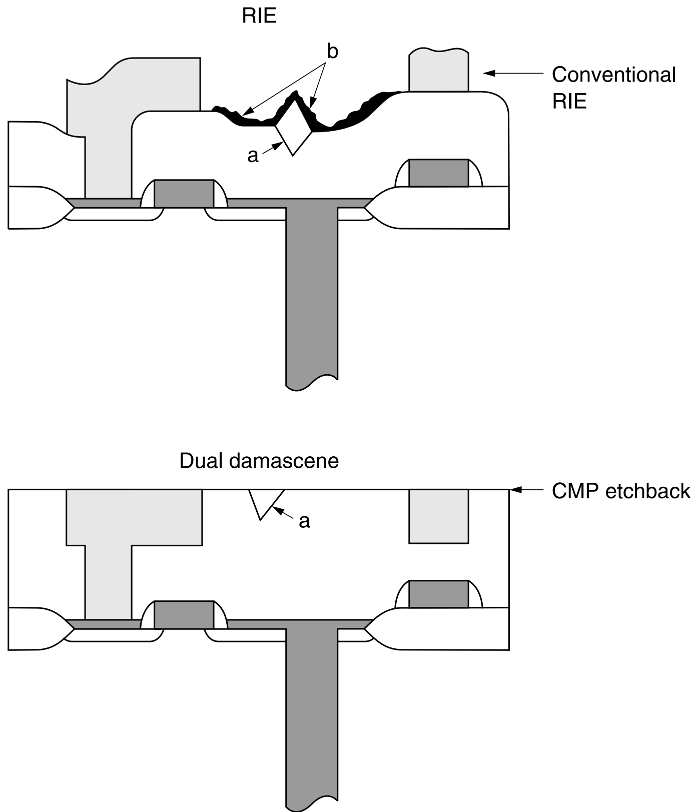

Figure 6.36 Defect reduction using CMP. Top: after RIE, tip of embedded defect (a) protrudes from surface; residual metal (b) on surface. After CMP (bottom) both kinds of residue removed by polishing. (Reprinted from Kaanta, C., S.G. Bombardier, W.J. Cote, W.R. Hill, G. Kerszykowski, H.S. Landis, D.J. Poindexter, C.W. Pollard, G.H. Ross, J.G. Ryan, S. Wolff, and J.E. Cronin, 1991 VMIC, 144, 1991. With permission.)

Belongia et al. (1999) to be effective in sedimenting the particles from suspension. Recycling of waste slurries was also mentioned as a possibility.

6.23 IMPACT OF CMP

Although CMP can create defects (see above) it can reduce or eliminate some (see Figure 6.36). Since the best planarity is achieved when the features are approximately the same size, there is a serious attempt to reduce the range of feature sizes. The use of larger numbers of vertical interconnects and narrow pitches is now possible, however. The approach to global planarity minimizes variations in film thickness (e.g., variations in capacitance) minimizes overetch and reduces or even eliminates depth-of-focus variability.

CMP is a low-temperature process unlike, for example, high-temperature sputtering or flowage of metals. A single kind of equipment is used for both dielectric and metal polishing. It is less expensive than RIE and ion milling. CMP of metal, an essential step in the dual damascene process, has made possible the fabrication of rectangular conductors, previously not considered feasible because of difficulty in patterning. The need for complete selectivity in CVD and plating is eliminated. The earlier doubts about the compatibility of the dirty process with cleanrooms and

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cleanroom practices have been laid to rest and CMP has become an accepted manufacturing procedure. There are now many suppliers of various kinds of polishing equipment, as well as of slurries and pads.

6.24 CONCLUSIONS ON TOPOGRAPHY

Many techniques discussed in this chapter can fill gaps extremely well and are planarizing as well, but the planarization is only local. The techniques, however, are often prerequisites for CMP and so continue to be useful. CMP produces the best planarization, the widest global range. CMP has been accepted into the chip manufacturing environment. Processes are constantly being developed, many have matured. Process monitoring and control have improved significantly. CMP is now an accepted step in the process flow in the fabrication of many kinds of chips.

6.25 REMAINING ISSUES FOR CHIP INTEGRATION

6.25.1 Overview

The detailed analyses of the individual process elements and their advantages and concerns were covered in Section 6.2 through Section 6.24. The elements were discussed from the point of view of the specific requirements they satisfy in building multilevel interconnection structures. A single process or material, however, cannot be selected for inclusion in a process sequence without consideration of the mutual interactions with other processes or materials. It is important to remember that the overall manufacturability and quality of the completed device depend on the successful execution of all elements. The last decade has seen significant changes propelled by the need to lower the RC delay in the interconnection wiring to reap the benefits of the smaller, faster-switching devices (in the silicon) and the increased number of circuits (and their density) on the chip, made possible by the advances in lithography and etching. This was accomplished by using lower resistivity metal, more metal levels, and smaller features (of the order of 100 nm and less), which allow increases in the wiring density, and insulators that have a lower ε compared with SiO_2. There have been many changes in the processes, equipment, and integration proposals. It is, therefore, very important that the different elements be brought together successfully. These mutual interaction issues can be grouped broadly as: (1) conflict between the choice of a process and the required structure, (2) process (in) compatibility, (3) reliability (defects), and (4) manufacturability (yield, productivity).

As noted above, there have been many significant changes in the BEOL interconnections. Some of these are the extensive use of Cu and associated processes (liners, plating, and CMP) and the migration to dielectric materials having a value of ε lower than that of SiO_2 but with significantly different (usually poorer) chemical and mechanical properties compared with SiO_2. The first of these films was FSG followed by, for example, SiLK, then SiCOH (and many others), and then versions of these films with pores that would have been classified as “process defects” in the past.

The number of wiring levels has increased and continues to increase to about ten and the line widths to decrease to about 90 nm. Thus the control of the defect density becomes even more exacting. Both chip and wafer sizes are increasing. The insulating layers are now being used not only as interlevel dielectric but also as etch stops and polish stops. This requires many steps of insulator deposition. Also, integrated into the overall structure are stacks consisting of layers of different materials with different chemical and mechanical properties. Successful integration has to include not only adhesion issues, but also differences in the coefficient of expansion, in-plane and in the normal directions, as well as any other possibly anisotropic properties. With respect to the metals,

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the need for liners to promote Cu adhesion to and prevent diffusion into the sidewalls of the insulator has been recognized and is now common (essential). However, the continued decrease in feature size requires new processes for depositing extremely thin but conformal and continuous liners. An example of a new process is atomic layer deposition (ALD) in which organometallic precursors are decomposed on a surface to form very thin layers. The push to migrate to 300 mm wafer facilities to improve productivity implies a target of the same or better yield. The newer equipment must be designed for greater uniformity over a larger surface than needed before. All these changes have made the issues of integration very critical to the successful outcome of wafer manufacturing.

6.26 PROCESS/STRUCTURE CHOICE CONFLICTS

Many of these issues have been discussed in the individual chapters, but are repeated here to put them into an overall perspective. The ITRS roadmap (2003) describes the challenges in the coming years as finding (1) low-ε materials with a pore shield barrier, which together with Cu can survive the harsh processes, such as CMP and etching, and (2) low-resistivity barriers to minimize the increase in resistance due to impact of electron scattering at the interfaces. Beyond 2010 one might need still newer materials to provide the improved chip performance being projected.

The parts of the interconnection processes, the materials and structure are closely interrelated. The choice of one invariably will affect the others. Some of these scenarios are discussed here, but the reader should remember that there are likely to be many others.

As mentioned above, the faster devices/circuits require minimum propagation (RC) delay in the interconnection wiring and the denser circuits require high wireability, i.e., the ability to wire a large number of circuits in a given area. These requirements drive the interconnection technology toward use of several wiring planes (known as multilevel metallization, MLM, or multilevel interconnects, MICs) (Berndlmaier, 1980; Fried et al., 1982; Sasaki et al., 1983), low-ε dielectrics for intra- and interlevel insulation, and high-conductivity metals for wiring. The advantages gained thereby are illustrated in Figure 6.37 which shows the decrease in cycle time as the number of wiring levels is increased, as well as the reduction due to both lower ε (e.g., using a fluorinated polymer (FP) in

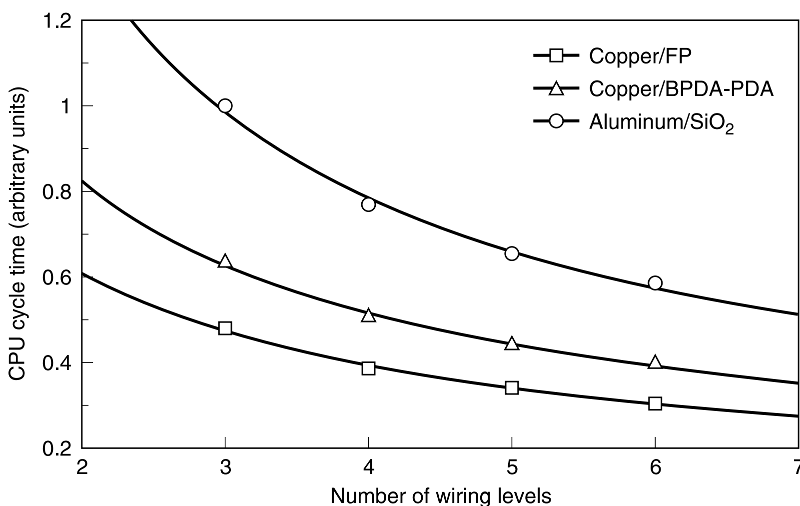

Figure 6.37 CPU cycle time vs. number of wiring levels for Al/SiO_2 (top), Cu/BPDA:PDA (middle), Cu/FP (fluorinated polymer) (bottom). (Reprinted from Paraszczak, J., D. Edelstein, S. Cohen, E. Babich, and J. Hummel, IEDM, 93, 261, 1993. With permission. Copyright 2004, IEEE.)

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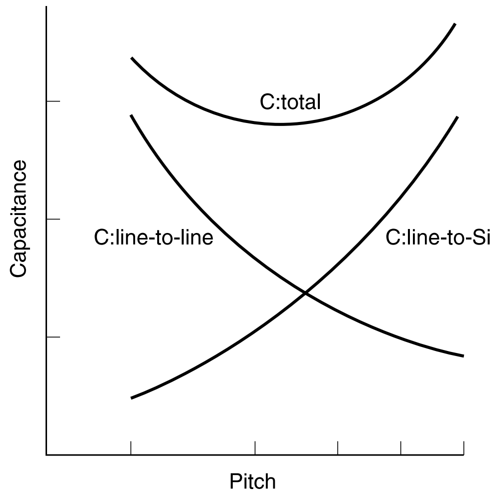

Figure 6.38 Capacitance vs. pitch (line width + space between adjacent lines): line-to-line, line-to-Si, total capacitance.

place of BPDA-PDA PI) and ε (although some of the delay is due to the higher ε of SiO_2 as well as the higher ρ of Al).

The relative chip size also decreases as the number of levels is increased; thus it is seen that the use of MLM increases the wiring efficiency and decreases chip size. According to the ITRS (2003) projections, the number of wiring levels will increase from the present 9 to 12 levels. In comparison to the sloped via/sputtered AlCu/RIE technology, these 9 to 12 levels represent approximately twice as many mask levels, etch, and metallization process steps. One way of increasing density is to decrease the wiring pitch. However, as seen in Figure 6.38, although decreasing the pitch reduces the capacitance to silicon it increases the line-to-line capacitance, so that eventually the overall capacitance and hence the delay is increased.

Increasing the line-to-line spacing lowers the intralevel capacitance but increases chip size. Increased chip size requires increased wiring length, resulting in longer delay because both resistance and capacitance to the silicon are increased, and, as noted above, the use of several wiring planes has long been an accepted solution to these problems. Once the choices of insulator and metal are made, the horizontal geometry of conductor features and separations are optimized for wireability and minimum propagation delays by modeling and simulation. The use of several wiring planes introduces the need to keep the capacitance between successive metal levels as low as possible. Thus, thicker insulators might be preferred for reducing both interlevel capacitance and interlevel shorts. However, thicker insulators are difficult to etch, anisotropically, and the etched holes have a high AR; etching is complicated, still further, by RIE lag which requires significant overetching.

To maintain acceptable wiring pitches at higher wiring levels, thicker insulators necessitate the use of vertical interconnects (studs/plugs) instead of tapered vias to be filled when depositing the next level of metal. However, it is difficult to fill a high-AR hole by most metallization processes. Vertical studs introduce another interface, require more process steps (e.g., an extra deposition step), as well as other process complexities, and therefore add to the cost of processing.

A process that utilizes single metal deposition cycles with integral wire–stud interfaces, the so-called dual damascene process, was proposed by Kaanta et al. (1991); it avoids some of the problems mentioned.

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When feature dimensions decreased to 130 nm, the device fabrication industry adopted this process, shifting the demand from RIE of metals and gap-fill by insulators to RIE of insulators, forming liners, and void-free filling the high-AR openings with metal. Complete cleaning of the bottom of a deep hole etched in the insulator, to prepare it for subsequent metal deposition, is vital. Many of the low-ε dielectrics are incompatible with the cleaning processes used for SiO_2 and new processes (e.g., Ar/N_2 aerosols, H_2/He plasmas) and new cleaning liquids (e.g., CO_2-based fluids) are being introduced. Exposure of porous films to N_2 must be avoided because of poisoning of DUV photoresists. Extreme care must be taken to dry the wafers completely without damage.

The wide adaptation of the dual damascene process and electroplated Cu have minimized the number of nonlithography process steps, but bring their own complexity to the integration.

Sloped vias, if any, are used only at the uppermost of the multilevel wiring levels. The ITRS (2003) projections of metal 1 pitch and interconnect failure rate objectives are shown in Figure 6.39 for a three-year technology cycle. By this projection, the metal wires are expected to be about 50 nm, half of the current 90 nm dimension. It is likely that some of the current processes may not be extendable. At the same time, with the increase in wiring levels and density, the total wiring length continues to increase, and the interconnect wire failure rate objectives per unit length becoming more stringent.

Since AlCu metallurgy is still widely used with devices below 130 nm, the following discussions continue to be relevant. To increase conductivity without sacrificing wiring pitch or changing the metallurgy, tall narrow lines can be used. RIE of such metal features presents difficulties related to RIE lag (the decrease in etch rate as the AR of the feature increases) similar to that encountered in etching high-AR holes in insulators. This also means that the insulator deposition process needs to fill high-AR spaces between the conductors. Biased high-density plasma PECVD, SACVD, and a dep/etch PECVD process have all been used for improved gap-fill. Alternatively insulating materials with good gap-fill properties such SOGs or spin-on organic films can be used. Each of these processes brings with it issues, either new materials or new process conditions. For example, a biased high-density plasma PECVD process can result in sputter etching of the underlying metal lines; to avoid this, one has to start the deposition using a lower bias. SACVD insulators have been known to have a low density and high water (OH) content. Dep/etch processing is more expensive than simple deposition.

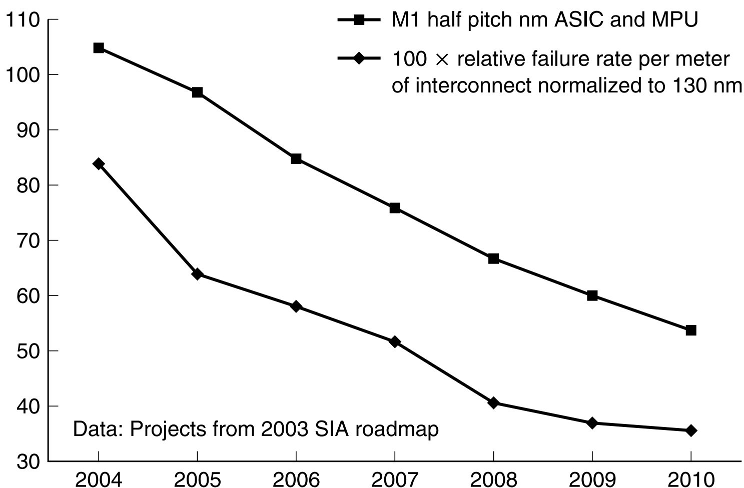

Figure 6.39 SIA 2003 trend projection of M1 half pitch and metal failure rate objectives.

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If organic insulators or SOGs are used for their improved gap-filling properties, one has to be concerned with their thermal stability and with moisture absorption which increases the dielectric constant of the film (Harada et al., 1990). Many of the available low dielectric constant insulators are organic or highly fluorinated inorganic oxides. These materials also suffer from thermal degradation and moisture absorption that may lead to delamination of subsequent metal or insulator layers. For example, FSGs become unstable when the F-content is too high. Even at levels of F acceptable for stability, the F in the FSG can migrate to Al wires and can cause corrosion, necessitating the use of insulating F-barriers such as SiO_2 and SiN (Cooney et al., 2000), thereby increasing the effective ε. Porous insulators are being developed to lower ε still further but porosity introduces its own problems.

The molecular structure of some organic insulators such as PIs are different in and out of the plane of the film; this has been shown to result in orientation-dependent mechanical and electrical properties, such as the coefficient of thermal expansion and leakage. Thus, minimum thickness specification needs to take into account the difference in properties due to orientation. In structures made using PECVD TEOS-based oxide, the line-to-line capacitance was higher than expected from the value of ε determined on a blanket film. The capacitance of similar structures, using SiH_4-based or sputtered oxide. An instance of a difference in a film property depending on its position in a structure is that of dep/etch SiO_2, using PECVD TEOS-based oxide (Schwartz and Johns, 1992). The material in the gap etched more rapidly in BHF than did the oxide on the top surface and an unidentified filament-like structure was also seen near the sidewalls, except when O_2 was substituted for Ar in the etch cycle.

Finally, the planarization process may determine the choice of insulators. For example, in CMP, a material such as silicon nitride is hard to polish and can act as a polish stop, and may be used despite its high ε. Organic insulators tend to scratch easily when polished and may, therefore, be unsuitable to be used with CMP.

A high-conductivity metal such as Cu can be used; but issues such as adhesion, oxidation, and diffusion through insulators, discussed in Chapter 5, will require the use of glue layers and barrier layers which reduce the effective conductivity, as shown in Figure 6.40 (Edelstein et al., 1995).

Since Cu, unlike Al and its alloys, is not easily patterned by RIE, the choice of Cu restricts the patterning options. The current choice is the dual damascene process but that introduces new steps. To protect Cu from oxidation as well to improve adhesion of SiO_2, a layer of SiN is deposited after the Cu CMP step (Hu et al., 1989).

An underlying requirement for advances in semiconductor integration is the continued evolution of lithography process for printing smaller and smaller features. Optical exposure systems now use deep-UV radiation (245 nm) with 197 nm projection systems being used for critical levels and liquid immersion systems might be the next stop. Phase shift masks and optical proximity corrections have become common. The shorter wavelength, together with associated improvements in lenses, makes possible printing of images that are significantly smaller than 250 nm. Printing these fine features exacts a price; at every exposure level, the exposure field has a tight planarity requirement, i.e., a small depth of focus (DOF) over the field of exposure. However, to maintain productivity, the goal is to keep the exposure field area the same in future exposure systems, i.e., 30 mm $\times$ 20 mm. As the feature size resolved decreases, the topography requirement over the filed of exposure becomes tighter, less than about 0.1 μm for good focus. This requires excellent planarization at every level. This has made CMP (which is described earlier in this chapter) the process of choice.

As stated at the start of this chapter, there is both an upper and lower limit to the thickness of the resist used to transfer the mask image to the material to be etched. An upper limit exists since the smallest thickness of resist provides the best resolution. However, a resist cannot be too thin; that limit is determined by the ability to spin-on continuous films without pinholes. RIE, used to etch anisotropically, in order to produce vertical features and control process bias, consumes resist masks at a finite rate. If thick films must be etched, then processes that have high selectivity to resist

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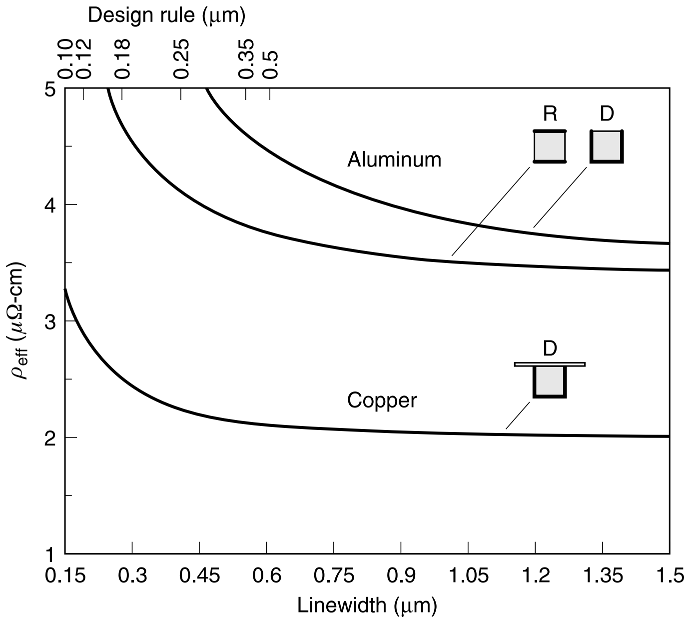

Figure 6.40 Effective resistance of encapsulated metal conductor vs. linewidth. (Reprinted from Edelstein, D.C., G.A. Sai-Halasz, and Y.J. Mii, *IBM J. Res. Develop.*, 39, 384, 1995. With permission.)

must be developed or else complicated multilayer resist schemes must be used to decouple etch masking and lithographic print requirements (Bushnell et al., 1986).

When the semiconductor devices and circuits require mixed feature sizes, the differential between the RIE rates of small and large features, RIE lag (Lee and Zhou, 1991), will increase the need to overetch. To compensate for large wafer size and RIE lag etch nonuniformity, etch-stop layers came into use; this introduced the need for improvements in adhesion.

Increasingly, passive devices (capacitors, inductors) are being fabricated on the chip for analog and mixed signal applications. The MIM capacitors and metal inductors are formed in the interconnection layers. The inductors do not require additional wiring level but also may require an increase in the line thickness to make fat inductors or overlays of two or more levels (see, e.g., Burghartz et al., 2000). The capacitors, however, add at least one extra process step, to define the top or bottom electrode or the capacitor dielectric. Since the capacitor dielectric is thin compared to stud insulator thickness, an extra level of wiring is added to the process.

Since most of the chips are wirebonded, the pad surface metallurgy is preferably Al. Copper is difficult to wirebond to. In integrating an Al pad layer with the Cu interconnection, the tendency for rapid reaction of Cu–Al has to be taken into account and suitable metallic barriers between the two have to be used.

6.27 PROCESSES

Compatibility of later process steps and materials with earlier ones is essential. Plasma processes, especially deposition at high rates using high bias, can increase the wafer temperature well above acceptable temperatures for Al wiring, unless adequate heat transfer equipment is used which complicates the design and operation of the plasma systems. As discussed in the reliability

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chapter (Chapter 7), thermal stresses are a major source of failure for thin conducting film. Laser and thermal reflow and CVD W deposition for stud levels can increase temperatures substantially and may cause problems in underlying metals. Many of the low-ε materials used as gap fillers or as primary insulators can undergo irreversible changes or degradation at temperatures in the 500°C range. Outgassing of adsorbed moisture from SOGs and other dielectrics during subsequent process steps can result in blistered metal (Hirashita et al., 1990) and high via resistance (so-called "poisoned vias") (e.g., Romero et al., 1991; Hamanaka et al., 1994). Desorption can have other effects as well. For example, it takes very little absorbed moisture outgassing to scatter metal atoms in vacuum and cause tapered studs, which appear black in an optical microscope (Schwartz, 1991). Too much outgassing can prevent metal deposition within the via, since the outgassing molecules can create high local pressure and scatter the arriving molecules.

If the deposition of insulators requires oxidizing ambients, the metal surfaces can be oxidized, increasing the resistance of the contact. Reflow or densification of BPSG or PSG for planarization or improving oxide contours requires high temperatures, in excess of 700°C. Depending on the exact temperature, devices and gate electrodes or local silicide/poly-silicon wiring can degrade. Film stresses can affect adhesion and cracking of underlying layers.

The patterning of any layer must be compatible with underlying layers. Exposure to an O_2 plasma during plasma stripping of resist can result in cracking of some SOGs and degrade many low-ε materials so that H_2/He plasmas have been used instead. Etch selectivity is essential since overetching is required to accommodate process nonuniformity. If corrosive gases are used in etching a conductor, then the underlying insulator should be impervious. However, organic insulators can absorb the chlorine species used in RIE of an Al alloy; these can be released subsequently, leading to corrosion. Even a small amount of residual chlorine is known to cause corrosion in different metal systems (Parekh and Price, 1990).

Liners, seed layers, and electroplating processes must be mutually compatible. Any defects in the liner and seed layers can easily mushroom into an unacceptable metal fill. The possibility of poisoning devices by contamination of the wafers by Cu (even in the ppb range) was a serious issue in the development of plating hardware; the equipment must be built so that the back and edges of the wafer never come in contact with the Cu plating bath. Cu poisoning is also an issue in designing the Cu CMP process. Cleaning after CMP has become critical to ensure that there are no residues. Scrubbing and use of HF-based solutions, surfactants, and adjustment of the pH to control the forces between the particles and substrate are among the treatments that have been used. Complete drying is also important. The insulators must not absorb species that may degrade their quality from either the processing ambient or the manufacturing environment. Examples of the deleterious effect of absorption of moisture from the environment on some deposited oxides are increases in the dielectric constant and stress hysteresis. Dilute HF-based solutions, isopropyl alcohol, and phosphoric-chromic cleaning mixtures are commonly used many times during the fabrication of the multilevel interconnection and both conductors and insulators used should be inert to these chemicals. This problem will only become more severe with the plan to use porous insulators which provide additional sites for entrapments of chemical and ionic metal impurities. Cryogenic cleaning using inert gases can be potentially attractive as the cleaning interaction is more mechanical/thermal and less chemical.

A necessary element of manufacturing is resist rework to correct any misprint or misdevelopment. The usual process involves wet stripping followed by ashing (O_2 plasma). In the case of inorganic insulators or Al metallurgy, these steps are not harmful. In the case of low-ε insulators one may have to add additional barrier layers between resist layers and insulators to allow resist rework.

6.28 RELIABILITY

Chapter 7 provides an in-depth discussion of reliability. It is touched upon only briefly here.

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6.28.1 Defects

Defects invariably cause early failures in use; these can be distinguished from the statistically distributed wear-out failures during extended use. The choice of interconnect materials and their thicknesses and specific processes used can also lead to reduced wear-out lifetimes. A defect can be defined as an unwanted feature created by missing material such as pinholes in insulators, voids or notches in the metal conductor, or by the presence of extraneous particulates, metallic or insulating. The effect of the defect is to alter the line/space dimension to a value below the minimum design value, outside of the usual distribution. In the extreme case, the defect can lead to an electrical short or an open circuit. The defects can be created by a variety processes, masks, and equipment. Here, we are mostly concerned with how the choice of a deposition or patterning process can lead to a defect at a later or earlier level. Deposition processes, equipment, and cleanroom ambient can all add particulates to the surface. A metallic particle on an insulator surface can become a potential path for shorting between conductors at a subsequent level as shown in Figure 6.41. Upon planarization, the metallic particle simply becomes an extraneous stud which shorts conducting lines above it; however, this effect of the extraneous particle can be reduced by the deposition of a redundant insulating layer after the planarization step. Similarly a defect in the insulator, such as a hole or a depression, can lead to traps for unwanted metal films in a subsequent damascene process, which can lead to metal shorts between two levels as shown in Figure 6.42.

Sometimes the choice of the process can make the structure more immune to the defect, as illustrated in Figure 6.36. Damascene CMP is sensitive to pinholes and voids in the insulator. In

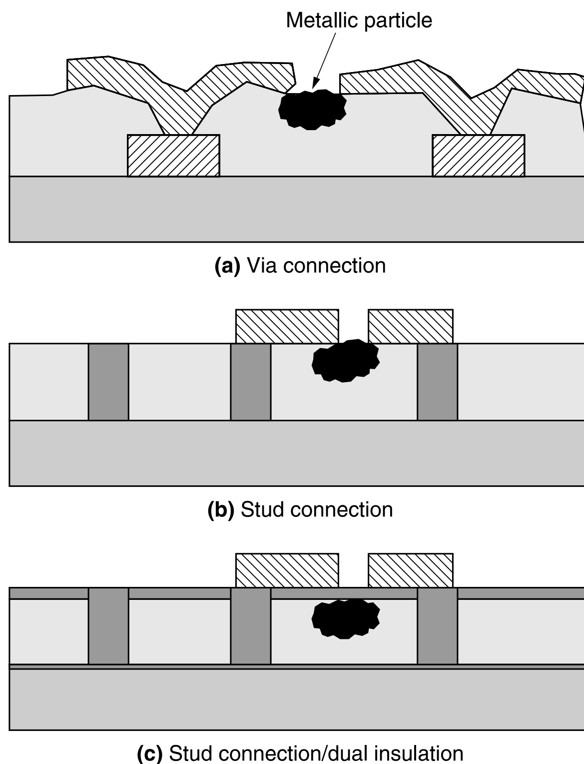

Figure 6.41 Schematic representation of the effect of metallic defects causing shorts: (a) a via interconnection; (b) a stud interconnection; (c) the benefit of a dual insulator on a stud interconnection.

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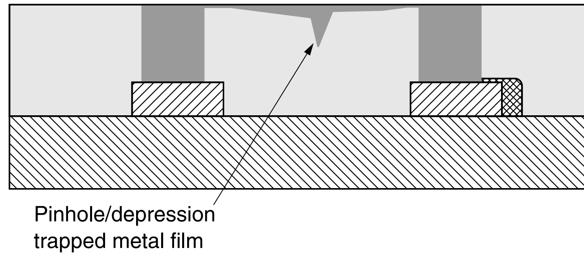

Figure 6.42 Schematic representation of the effect of a defect in an insulator, in a damascene process; metal trapped in pinholes or depressions (e.g., scratches) causing shorts.

etchback planarization, defects (a pinhole or hard particle) in the planarizing layer can be translated into defects in the insulator (a pinhole or a bump). These defects are not created if the insulator is not planarized or if an additive process is used for forming the stud or wiring. Similarly, if the chosen insulator tends to absorb moisture and release it during the hot metal deposition step, this can prevent the nucleation and growth of the metal leading to voids or porous metal films. Sputtering processes and equipment can add particles. Some sources are impurities in the processing gases and delivery systems, transport and clamping/unclamping of wafers within the reactor, spalling of poor-quality material deposited on the chamber walls, and metals sputtered from the walls themselves. Load locks, soft pumping, and frequent *in situ* or *ex situ* chamber wall cleaning as well as better design of mechanical parts are often used to minimize some of the problems. Another source of particulate contamination arises in the plasma due to gas-phase nucleation and growth by condensation of species generated in the plasma (Selwyn et al., 1989; Weiss et al., 1995). Highly stressed metallic films, such as CVD W can delaminate locally and be transported to regions where they are unwanted. The delamination problem is aggravated if the adhesion and nucleation layer such as TiN is inadequate. Residues from RIE (e.g., inadequate overetch, deposited polymer, or unetchable impurities in the film) are a problem; cleanup processes/chemicals used after the etch process can lead to attack of the exposed metal or insulator. Post-RIE corrosion of Al (alloys) by residual Cl can be controlled but require the use of extra plasma or wet chemical treatments (Mayumi et al., 1990).

Defects in resist layers and masks can result in defective patterns; if the defect occurs in a sensitive area it may result in yield loss or compromised reliability. Point of use filtering with extremely fine filters is increasingly preferred with spin-on layers, to remove gels and other extraneous particles. In the same vein, some materials are more prone to create or be affected by defects. Incorporating refractory metals into AlCu conductors by layering or cladding has been preferred since defects and voids in the AlCu film have less effect on the total structure. Aluminum forms a good passivating oxide but incorporation of large amounts of Cu make the film more susceptible to corrosion. Copper does not have a passivating oxide and is more susceptible to oxidative damage. Copper and Al are scratched easily during CMP. CVD metal growth is a heterogeneous process and any impurity in the surface of the seed film can lead to voids or other defects in the grown film.

6.28.2 Insulator Reliability

A direct short or a leaky path in the insulator, even a momentary breakdown, can result in circuit malfunction. The intrinsic quality of the insulator material can affect its breakdown characteristics. For example, an organic-based insulator or a F-doped SiO_2 film, used because of its low dielectric constant, may have a lower breakdown strength, as illustrated in Figure 4.8 and Figure 4.20.

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With the continued shrinking of the insulator thickness and metal to metal spacing and the use of different layers of insulators, the interfaces are likely to dominate as the source of failures. Interfaces of different materials such as SiN, SiO_2, and SiC have different molecular structures which can potentially lead to open structures at the interfaces, along which metallic impurities (or any ionic species) can migrate from one conductor to an adjacent conductor, increasing line to line leakage. This problem can continue to build up over time causing failures during use, a reliability issue. This phenomenon can be a function of the nature of the interface, impurities introduced during processing, and the temperature during use. The many sources of interface leakage would make it difficult to model this failure phenomenon and predict failure rates.

The choice of material and process can affect the adhesion of the insulators to each other and to the metal. For example, stacks of various insulators are often used to meet certain process requirements and adhesion failures between them can occur. Loss of adhesion can result in local delamination and thus hot spots and early failures can develop.

6.28.3 Metallization Reliability

The major concerns about thin-film metallization are corrosion, electromigration, and stress-induced failures such as voids, extrusion, and cracking; each of the problems can aggravate the other. The choice of insulators, the geometrical structure of the interconnect, and finally the choice of metal and deposition process which determine its microstructure, all influence and affect the extent of the reliability failures. These issues are discussed in detail in Chapter 7.

The choice of the insulator can expose the wiring to corrosion. Defect-free inorganic insulators afford excellent protection. Organic insulators, however, usually absorb moisture which can permeate readily to reach the thin metal film, leading to corrosion, especially since the thin film (wiring) is likely to be electrically biased. Another example can be found in the poor adhesion of PI to metal, coupled with its tendency to absorb moisture, makes possible the formation of a monolayer of film of water, said to be necessary for the initiation of corrosion of Al-based conductors.

It may be necessary to use AlCu layered with or capped by refractory metal to improve electromigration performance, although this increases the line resistance. Another issue needing consideration is whether the choice of metal and its method of deposition and/or patterning has any adverse effect. Metal solubility, migration in the insulators, and reaction with and adhesion to the insulators are some areas of concern. For example, polyamic acid is known to dissolve Cu from the interface and clusters of copper redeposited within the polyimide body (LeGoues et al., 1988; Kim et al., 1990). Copper diffusivity necessitates the use of barriers, at the cost of higher resistance. Forming adequate liners is exceedingly difficult when the AR of the feature is high. This problem is aggravated when porous insulators are used; the inevitable sidewall roughness adds to the difficulty in forming adequate liners. Thus failures may occur during use due to Cu migration. Voids and seams can be produced in a plating process, particularly when the features have a high AR. This can lead to high contact resistance and even open circuits during operation.

Passivating films play a role in determining electromigration lifetime; this is covered in Chapter 7.

6.28.4 Device Reliability

By and large, the devices formed in the silicon remain unaffected by MIC materials and processes except for the introduction of ionic impurities such as Na^+, plasma damage, moisture evolution, and impurities that emit alpha particles.

Ionic impurities are usually introduced as trace impurities from wet processing using chemicals such as alcohols and acids, resist processing, including developers and polishing slurries used in

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planarization by CMP. In all cases, it is essential to devise methods for eliminating these impurities, by purity specification or other targeted actions. The choice of the insulator, especially adjacent to device layers, should be one that is an effective diffusion barrier to ionic impurities and/or moisture (such as silicon nitride) or one that actively getters the ionic impurities such as PSG.

Plasma damage to gate oxides can occur in both etching and deposition. The damage has been said to be due to plasma nonuniformity leading to a local imbalance between electron and ion currents from the plasma, resulting in gate charging and subsequent gate oxide degradation (Fang and McVittie, 1992). The damage becomes more serious as the thickness of the gate dielectric is decreased. In an ECR plasma, it was shown that the charging occurred at the time the discharge was turned off (Samukawa, 1990); to reduce damage, the power can be ramped down at the end of processing. Modification of the magnets in an ECR reactor was shown to improve the magnetic flux and current densities at the wafer surface, thus reducing charge damage (Nakahira et al., 1996). Other kinds of RIE damage occur during etching contact holes which exposes the Si surface. Some of these effects are surface residues (e.g., polymer films), loss of dopant or dopant activity, impurity penetration (particularly hydrogen), lattice damage, and heavy metal contamination. This subject has been discussed more completely by Oehrlein (1989, 1990). Deposition of SiO_2 by sputtering has been shown to cause threshold shifts in gate oxides (Larsen, 1980). The damage is probably caused by production of x-rays in the gate, generated by secondary electrons produced at the target (Grosewald et al., 1971); reducing their energy (Logan, 1977) or placing a DC-biased mesh between target and substrate (Hazuki and Moriya, 1987) reduces the damage. Flat-band shifts have been attributed to high-energy (VUV) photons in plasmas.

Outgassing of moisture from insulators can cause n-channel field inversion (Yamaha et al., 1993) and hot-carrier degradation (Doki et al., 1994).

Alpha-particle radiation can affect storage states in memory devices; many of the metals used in the interconnection and cleaning solutions used in processing can introduce trace amounts of thorium and other radioactive impurities that can cause unacceptable failure rates, often requiring the use of error-correction circuits or radiation-hardened device designs.

The use of compressive insulating films has been found to delay the onset of emitter current gain (beta) degradation in bipolar devices (Zalar, 1981; Hemmert et al., 1982). Most of the above concerns and considerations are unchanged by the use of Cu and low-ε materials, as long as Cu is kept away from the devices using insulating and metallic barriers and avoiding any process-induced contamination.

6.29 MANUFACTURABILITY

When selecting the materials and processes, issues of manufacturing and volume production should be kept in mind. Two key issues are yield and productivity and both affect the cost of products. Yield is improved if the materials and processes are compatible and the individual processes have large process windows. Clustering of reactor chambers and processes, *in situ* cleaning, and real-time process monitoring all should help in achieving better process control and high throughput. The process/application requirement is often tempered by the availability of process controls and equipment capable of high throughput and low defect levels. New SOG materials that seem to be more crack-resistant and less prone to absorb/desorb moisture increase their use as gap-fill dielectrics. With the increased use of studs in place of vias, CVD W, and, more recently CVD Al and Cu, have become more commonly used, since these processes provide good fill behavior. Deposition processes for Al–Cu or Al–Si are being modified to improve hole-filling capabilities; among them are elevated temperature and directional sputtering. Another path for enhanced hole-filling is the use of substrate-biased high-density plasma systems for metal and PECVD oxide deposition. Improved RIE reactors, using high-density plasmas, have been introduced to meet the need

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for etching vertical, high-AR features; process modifications have been designed to minimize pattern-factor effects. For the 130 nm and smaller featured MPU and ASIC devices, however, some of these improvements in materials and processes are less important due to the migration to dual-damascene processing, electroplating of Cu, and new low-ε materials. CMP for planarization has clearly the conceptual advantage of providing excellent local and global planarity, but its increase in use is fueled equally by the wide choice of commercially available polishers, pads, and slurry materials, alternative cleaning methods, and finally tool modifications and controls that lead to better uniformity and process monitoring.

However, the improvements obtained by using the advanced equipment and processes must be cost-effective.

6.30 WAFER SIZE

Fundamentally, integration issues do not depend on the wafer size directly, although many of the integration issues tend to become aggravated as the industry migrates from one wafer size to a larger one. The new equipment and a general degradation in uniformity will often necessitate modifications of the process and its control. Fortunately, the migration to 300 mm and the associated learning has started with years of planning. Extensive use of standard tool interfaces, real-time monitoring to control processes at the individual wafer level, and analysis and monitoring of the data have been used to climb a steep learning curve.

One of the early goals of the 300 mm manufacturing facilities (fabs) was to automate as much of the wafer handling through use of standardized containers (FOUPS, front opening unified pods). The development of equipment for processing 300 mm wafers has been guided by CIM and SEMI standards. Some of the benefits are the industry-standard software functionality, equipment front-end load modules, number of load ports at every work station, facility for FOUP docking, carrier ID verification, recipe downloading, and so on. Data collection and analysis diagnostics has improved. From the point of view of foreign material (FM)-caused defects, there is greater isolation of the wafer within the processing chamber from the external facility. This has reduced the need to emphasize cleanroom class and garments, thus making it more comfortable for the operators. However, the feature driven need for reducing the impurities in the wafer processing environment has continued to be demanding. The focus has moved to manage process-induced particulate generation, purity of gases and chemicals and more effective ways to clean wafers during processing, low or no outgas wafer carrying plastics, and also the quality of in-between process steps. Most of the 300 mm fabs have open-space architecture with islands of operating equipment and sophisticated wafer container movement system. The wafer containers are moved along tracks in two directions and lowered to individual stations. It is amazing to think that the industry is already starting to plan and lay the foundation for wafers that can be as large as 450 mm in diameter, even though it is (thankfully) several years away.

6.31 CONCLUDING REMARKS ON COMPATIBILITY OF MATERIALS AND PROCESSING

The starting point for choosing conducting and insulating films as well as the processes for use in multilevel interconnection, in order to achieve the best performance from the device or chip, is often determined by modeling and simulation. With new materials the risks of running into major problems are high. Beyond the risk factor, other issues of integration become important considerations for deciding which processes and materials are feasible. The issues range from compatibility of materials and processes to manufacturability and affordability. Often, the changes are made in small increments to improve predictability of the results and begin the learning process; to recover

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the maximum benefit from the existing infrastructure and minimize new investment. It is often wise to wait for the new processes and equipment to mature. For the same reason, the hardware (most of it) has become a commodity unable to command profit margins required for new investment to solve future needs and invest in productivity. This has led to joint development efforts among companies, sharing the cost, and the creation of industry–university (and some government) consortia (such as Sematech, Nanotech center). The cost of building and equipping new fabs is substantial and is continuing to escalate. This is a dark cloud hanging over the future direction of this industry.

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CHAPTER 7

Reliability

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7.1 INTRODUCTION

The reliability of an interconnect/insulator system in a multilevel integrated circuit structure is complicated. The small dimensions of contemporary integrated circuits (ICs) and the variety of materials employed means that the reliability of literally billions of circuit elements must be evaluated in terms of a multitude of failure mechanisms. The total wiring length in state-of-the-art ICs (microprocessors) is in the neighborhood of kilometers arranged in up to ten levels of wiring with hundreds of millions of interlevel connections. The reliability is further complicated by the presence of process-induced defects.

Although there is no stated industry standard, competitive reliability targets of chip failure rates have been on the order of one per thousand throughout the anticipated lifetime in the field. The demands on each of the components, i.e., on the fine wiring lines, on each contact, etc., are enormous. As an example, if all elements in the chip are critical, that is, if the failure of any single element will cause the failure of the chip, the probability of the chip with n components surviving, $P_s(n)$, is

$$P_s(n) = (1 - P_f)^n \tag{7.1}$$

where P_f is the probability of failure of a single element which is assumed to be the same for each element. In order to obtain the desired reliability of 0.1% cumulative failure probability, the probability of failure would have to be on the order of 1 part per trillion (10^{-12}) for a high-performance microprocessor as described above. This is a number that is hard to imagine.

As device and interconnect dimensions are further reduced, the complexity of ICs increases concurrently, meaning that either the reliability must suffer if the circuit element reliability remains constant, or the reliability of the circuit elements must increase if chip-level reliability is to be maintained. Since the customer is only sensitive to the latter, the challenge is on.

This capability of producing even more complex wiring with equivalent or better reliability at the chip level can only be achieved by understanding potential failure mechanisms and using this understanding to select appropriate materials, optimize process procedures and controls, and apply design limitations. Because burn-in is routinely and increasingly used to weed out early fail defects, field failures are dominated by wear-out processes that are relatively well understood and, therefore, amenable to modeling and prediction. This chapter reviews interconnect reliability, dominated by two critical wear-out mechanisms, electromigration (EM) and mechanical stress-induced voiding (SV). The subjects of corrosion and intra- and interlevel dielectric reliability are also briefly discussed.

7.2 THIN-FILM INTERCONNECT RELIABILITY

7.2.1 Overview

Although there are similarities between the reliability of Al and Al alloy conductors and Cu, the conductor of choice for state-of-the-art high-performance ICs, they are treated quite differently.

In the earliest ICs, at the beginning of the age of microelectronics (about 40 years ago), pure Al thin-film wiring was used as the interconnect metal. Soon, however, it was found to be lacking in

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current-carrying capability due to its susceptibility to electromigration-induced failure. Al was also found to be prone to stress voiding and hillock formation. It comes as no surprise that these three failure mechanisms are related since they are all diffusion dependent. The thin Al-based conductors initially used were very fine grained and, at the temperatures of use (50 to 100°C), grain boundary diffusion was extremely rapid. The key to improving the reliability was to slow down grain boundary diffusion, which could be achieved by proper alloying. An effective reduction in hillock formation coupled with enhanced electromigration performance was indeed achieved by using Al alloys (Ames et al., 1970; d'Heurle et al., 1972) and multilayered structures of Al (or Al alloys) with a layer (or layers) of a refractory metal (Finetti et al.,1986; Gardner et al., 1985; Howard et al., 1977, 1978; Rodbell et al., 1991; Wada et al., 1986). Although other materials have been found to work, such as creep- and corrosion-resistant Al alloys like Al–Pd or Al–Sc (Onuki et al., 1990; Rodbell et al., 1993), Al–Cu alloys have remained the workhorse for Al-based technologies to the present day.

Electrodeposited Cu has recently become the conductor of choice due to its lower resistivity, as compared to Al, and its capability for increased electromigration resistance (Edelstein et al., 1997). However, care must be taken when implementing Cu metallization to realize the advantages over Al (Lloyd and Clement, 1995). Unlike Al, Cu does not form a tough, adherent oxide that effectively shuts off the film surface as a diffusion pathway. The Cu surface, and the many interfaces associated with passivation and liner materials, may permit faster diffusion than the dominant Al grain boundary mass transport pathway.

7.2.2 Thin-Film Wear-Out

7.2.2.1 Diffusion-Induced Failure Mechanisms

Mass transport is the response of diffusing material to a variety of driving forces, all acting in unison, some together and others in opposition. The direction and the strength of the driving forces according to various boundary conditions determine the mechanism that will ultimately be responsible for failure. It is this interaction of multiple driving forces according to a variety of boundary conditions that creates a complex environment that must be understood in order that failure can be predicted and avoided by proper design practices.

Diffusion is described by the Einstein relation

$$J = \frac{DC}{kT}\left(\sum_i F_i\right) \tag{7.2}$$

where J is the mass flux, D the diffusion coefficient, C concentration of diffusing atoms, kT the average thermal energy, and F_i the driving forces. For thin-film conductors the major operating driving forces are electromigration, and stress, thermal, and concentration gradients.

7.2.2.1.1 Driving Forces for Diffusion

7.2.2.1.1.1 Electromigration The electromigration driving force arises from the momentum transfer that results from the collision of conducting electrons with diffusing metal atoms. Since any diffusing atom must have a vacancy associated with it, regardless of the diffusion mechanism, electromigration has often been described as the diffusion of vacancies.

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The electromigration driving force is traditionally expressed as

$$F_e = z^* e \rho j \tag{7.2a}$$

where z^* is a quantity known as the effective charge or the effective valence. This nomenclature comes from a traditional treatment of the mass transport, but in reality it is neither a charge nor a valence. z^* is, in fact, a term representing the sign and the magnitude of the aforementioned momentum exchange, e is the electronic charge, ρ is the resistivity, and j is the current density. Strictly, F and j are vectors, but in the interest of simplicity they will be treated here as scalars with little loss of insight.

The majority of metals are n-type conductors and, therefore, z^* is negative, meaning that the mass transport is in the direction of electron flow, or opposite to current flow if one agrees with Benjamin Franklin's convention. (Franklin, America's first internationally acclaimed scientist, was responsible for the convention that current flows from the positive to the negative terminals in a circuit. In fact, electrons, the particles that effectively cause the current flow in metals, go in the opposite direction. It is not recorded whether Franklin was a successful gambler, but the implication here is that he was not.)

The numerical value of z^* can be from near unity to the order of 10. This fact was instrumental in the history of electromigration in that this represents a clear indicator that z^* could not have been purely charge related.

Electromigration has traditionally been the failure mode of greatest interest in metallization reliability. Tremendous effort is expended understanding, measuring and controlling it. The elimination of electromigration is often the principle reason that currents are limited in the design of integrated circuits, and in many cases define the limits to performance. If electromigration resistance can be improved, higher currents can be permitted so that higher performance can be achieved.

7.2.2.1.1.2 Temperature Gradient Temperature gradients give rise to the Soret effect, or thermomigration, which is defined as mass transport that responds directly to a temperature gradient. This driving force is expressed as

$$F_T = \frac{Q^*}{T}\frac{\partial T}{\partial x} \tag{7.2b}$$

where Q^* is a quantity known as the heat of transport and can be either positive or negative. Theory shows that Q^* and the electromigration z^* are closely related (Huntington, 1966). The physical process giving rise to the Soret effect is the momentum exchange between thermally excited electrons and diffusing metal atoms, implying that if a metal is susceptible to electromigration, it should also be correspondingly susceptible to thermomigration.

This correspondence between electromigration and thermomigration is most prominent in solder materials. In these materials, because of peculiarities of the electronic structure, both z^* and Q^* are quite large and with the high diffusivity at low temperatures (solder materials such as Pb and Sn are metals with very low melting points), thermomigration can become a real reliability problem (Hua et al., 2003). It is generally not very important in conductor materials like Al and Cu.

Thermomigration is not to be confused with temperature gradient-induced electromigration failure which is an entirely different matter.

7.2.2.1.1.3 Stress Gradient A gradient in mechanical stress is a powerful driving force for mass transport. It is responsible for creep failure in high-strength materials and for the phenomena

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known in the microelectronics industry as stress migration. It is also responsible for many of the features we observe in electromigration behavior.

It is important to note that the driving force is not due to the stress level directly, but due to the gradient. If the stress is high, but there is no difference in the level of stress from one location to another, there is no driving force. Only if the stress is lower somewhere will there be a driving force for material to move there.

The driving force due to a stress gradient is given by

$$F_\sigma = \Omega \frac{\partial \sigma}{\partial x} \tag{7.2c}$$

where Ω is the activation volume and σ is the hydrostatic component of the stress.

7.2.2.1.1.4 Concentration Gradient

The last important driving force is due to the concentration gradient. This can also be interpreted as an entropy gradient, expressed as

$$F_\mathrm{S} = kT \frac{1}{C} \frac{\partial C}{\partial x} = kT \frac{\partial \ln C}{\partial x} \tag{7.2d}$$

In the absence of all other driving forces, this is the major reason for diffusion and is responsible for the traditional Fick's law diffusion that must be considered at all times.

7.2.2.1.1.5 Bringing It All Together

It is the interaction of all these driving forces, acting together according to the boundary conditions imposed by geometry and composition, that are responsible for essentially all that we observe in wear-out failure. None of the individual driving forces act alone and all must be considered in unison to understand how the system actually works in real situations.

It is instructive and helps in developing intuition into the failure processes to see the driving forces explicitly expressed:

$$F = \sum_i F_i = F_\mathrm{e} + F_\sigma + F_\mathrm{T} + F_\mathrm{S} = z^* e\rho j + \Omega \frac{\partial \sigma}{\partial x} + \frac{Q^*}{T} \frac{\partial T}{\partial x} + \frac{kT}{C} \frac{\partial C}{\partial x} \tag{7.2e}$$

In any failure model, all of these driving forces must be considered, and therefore it is the comprehensive Equation 7.2e that must be used to describe the behavior of the materials. Failure can only be understood by considering the subtle interactions of these driving forces acting together in unison and/or in opposition.

Combining Equation 7.2 and Equation 7.2e we obtain an expression for the mass flux:

$$J = \frac{DC}{kT} \left\{ z^* e\rho j + \frac{Q^*}{T} \frac{\partial T}{\partial x} + \Omega \frac{\partial \sigma}{\partial x} + kT \frac{1}{C} \frac{\partial C}{\partial x} \right\} \tag{7.2f}$$

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where D is the diffusion coefficient of diffusing atoms and is characteristic of the major mass transport pathway, i.e., interfaces, grain boundaries, or the lattice. D is thermally activated:

$$D = D_0 \exp \frac{E_a}{kT} \tag{7.3}$$

and highly sensitive to temperature. D_0 is a temperature-independent coefficient characteristic of the diffusion pathway and E_a is the activation energy of the diffusion mechanism operating in that pathway. The activation energy is a major defining quantity for electromigration and a very important quantity to be determined experimentally. The activation energy allows the use of accelerated conditions by enabling the extrapolation of high-temperature data to lower use conditions. It is also characteristic of the operative diffusion mechanism, identifying where work may be done to improve reliability.

7.2.2.1.2 Electromigration-Induced Failure

Electromigration is perhaps the most important of the wear-out failure mechanisms. Since the faster one can move electrons from one place to another, the faster the circuit can operate, high performance implies high current density. The current density will be limited by the susceptibility to electromigration.

The two major conductors used in the microelectronics industry are sputter-deposited Al alloys and electroplated Cu. There are many similarities in the behavior of these two materials and a number of important fundamental differences.

When a wire of any conductor is carrying a high current density, the conducting electrons induce a mass flux of the material that is directly proportional to the current. In the absence of mass flux divergences, there would be no electromigration failure. As the conductor material is transported along with the electron flow, and if as much material enters a region as leaves it, no damage can result. If, however, there are divergences, where the net mass flow is not constant, damage can result in the form of voids or extrusions that can cause electrical open or short circuits, respectively.

Let us consider what happens in a conductor undergoing electromigration-induced mass transport. In any real circuit, there must be a contact to the semiconductor or else there is no functionality. Conductor mass transport will then come to a halt at this location at what can be classified as a blocking boundary. In the absence of a temperature gradient, Equation 7.2f becomes

$$J = \frac{DC}{kT} \left\{ z^* e\rho j + \Omega \frac{\partial \sigma}{\partial x} + kT \frac{1}{C} \frac{\partial C}{\partial x} \right\} \tag{7.2g}$$

In a single component material, such as Cu or pure Al, changes in the concentration of the diffusing species are not supported when there is a free exchange between atoms and vacancies. It has been demonstrated that this atom–vacancy exchange is reflected in the creation of a mechanical stress (Blech and Herring, 1976; Korhonen et al., 1993). Therefore, Equation 7.2g in the presence of a perfectly blocking boundary ($J = 0$) such as that which exists at contacts or most vias (see Section 7.4) becomes

$$0 = z^* e\rho j + \Omega \frac{\partial \sigma}{\partial x} \tag{7.4}$$

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implying that a stress gradient will be generated by the electromigration mass flow. Equation 7.4 expresses the eventual state of the conductor everywhere at steady state. Therefore, if there is a blocking boundary, at the steady-state condition there is no net electromigration mass flow. The electromigration driving force is exactly opposed by the driving force from the induced stress gradient. This can, of course, only be possible if the maximum stress does not exceed the strength of the conductor. This strength is not the classical yield strength, but is a complex function of the material and the surrounding medium. However, in any case there will be a length of conductor from the blocking boundary condition where the strength, whatever it is, will be exceeded. If the conductor is shorter than this, electromigration immortality can be achieved; if longer it cannot. This length is commonly known as the Blech length (l_B) and is obtained by an integration of Equation 7.4:

$$\sigma_{\max} - \sigma_0 = \int_0^{l_B} \frac{Z^* e\rho j(x) dx}{\Omega} \tag{7.4a}$$

where σ_{max} is the maximum stress that can be accommodated by the system and σ_0 is the initial stress state. For a constant current density, Equation (7.4a) produces a product of the current density and the length that is a constant for a given technology (set of design rules and materials). It is this interaction between the electromigration and stress gradient driving forces that determines the features of electromigration failure, in particular, the so-called Black's law that relates time to failure with current density and temperature (Black, 1969a):

$$t_{50} = \frac{A}{j^2} \exp\left(\frac{E_a}{kT}\right) \tag{7.5}$$

The current exponent, 2, is the consequence of the time it takes for stress to build up to the point of failure, whereupon a void will form and failure follows soon afterward. This is referred to as nucleation-dominated failure. In many cases, however, the current density exponent in Equation 7.5 is not observed to be 2, but some other value, either higher or lower. In these cases the time to failure is more generally expressed by the generalized Black equation:

$$t_{50} = \frac{A}{j^n} \exp\left(\frac{E_a}{kT}\right) \tag{7.5a}$$

If $n \neq 2$, failure is not nucleation dominated and Equation 7.5a does not accurately reflect the behavior. If $n > 2$, the failure process can be either dominated by temperature gradients or by the Blech length effect described above and the actual relationship is much more complicated. If $n < 2$, failure is growth dominated, where the time elapsed following nucleation for damage in the form of voids or hillocks to grow to the point of disaster is a significant portion of the time to failure. The lower the measured current exponent, the more the failure time is dominated by growth. If $n = 1$, this implies either that the nucleation time vanishes, or there was pre-existing damage in the structure.

In reality, for growth-dominated failure, the failure time should actually be expressed as the sum of a nucleation and a growth term, but this is seldom done (Lloyd, 1992). It can be shown, however, that the errors induced by using Equation 7.5a are conservative in nature and not overly severe, as long as temperature gradient effects do not dominate. Therefore, the use of Equation 7.5a is a prudent method for predicting failure due to electromigration.

Electromigration failure is influenced both by macrostructural factors such as test structure geometry (Rathore et al., 1994), materials selection (d'Heurle and Ho, 1978), layering sequence,

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patterning dimensions, topography, and interlayer connection methodology (Scorzoni et al., 1991; Hu et al., 1995), and by microstructural factors such as the metal grain size and grain size distribution (Oates, 1990; Vaidya et al., 1980; Vaidya and Sinha, 1981), crystallographic grain orientation (texture) (Knorr, 1993), alloy solute distribution and precipitation (Colgan and Rodbell, 1994), dislocation densities (Livesay et al., 1992), and the number and quality of interfaces.

7.2.3 Electromigration Testing Techniques

There are many experimental techniques available for measuring atomic transport in thin films; these can generally be divided into three categories: (1) measurements of compositional or structural variations, (2) direct determination of the ion flux, and (3) time to failure measurements.

Compositional variations can be obtained, for example, by *in situ* scanning electron microscopy (SEM), transmission electron microscopy (TEM) techniques or by radiography. This is most useful in determining the basic physical parameter of electromigration, the effective charge, or valence, z^*. For instance, the value of z^* for a number of solutes has been measured by passing current for extended periods of time and measuring the composition as a function of position in the sample. This is especially valuable in investigating the behavior of interstitial solutes since the diffusion of interstitials is so rapid that the steady-state profile can be achieved before there is appreciable diffusion of the solvent. From Equation 7.2f and neglecting the effect of stress and temperature we see the solution for blocking boundary conditions is

$$0 = z^* e\rho j + kT \frac{1}{C} \frac{\partial C}{\partial x} \tag{7.6}$$

This is the only way that z^* can be unambiguously determined. However, this may be of arcane interest to materials scientists and solid-state physicists as it has little use in reliability engineering.

Direct mass transport measurements utilize marker or edge motion techniques to determine the direction of transport, the diffusion coefficient (D), and the effective charge (z^*). Drift velocity (V_D) can be directly measured by depositing a conductor onto a material with much lower atomic mobility, such as a refractory metal or conductive compound like TiN. The conductor of interest is deposited as an island on a thin film of the refractory material and current applied. The upstream end of the island will move at the drift velocity:

$$\nu_D = \frac{Dz^* e\rho j}{kT} \tag{7.7}$$

Since the refractory metal will be either very thin and of higher resistivity, the drift velocity can be easily measured by recording the increase in resistance of the composite conductor as a function of time. This is a simple and fast technique, although the relative roles of interface and surface diffusion may need to be accounted for, especially in narrow lines.

The most common technique and the one that is most relevant to engineering is that of accelerated lifetime testing of test structures. In these tests, a current (corresponding to high current density) is passed through the conductor at an elevated temperature and the time to form either an open circuit or a predetermined resistance increase is recorded. Constant current testing is most commonly used, but there is no reason why constant voltage testing cannot be used if the resistance increase that defines failure is not too high. For instance, if the definition of failure is only a 2% increase in resistance, this would be only a 2% reduction in current density and that only for a short time near failure.

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The problem here is that lifetime measurements can be critically dependent on relatively subtle features of geometry, and, more importantly, the test results must be capable of being related to the operation of real devices under realistic use conditions. Therefore, test structure design is critical. One important feature of a test structure is that the flux divergences that will be a feature in product chips must be duplicated or approximated in the test structure, but accelerated testing must also be possible. There must be absolute flux divergences, such as contacts or vias on the test structures. The major flaw in early test structures and in the NIST or NBS structure was that there were no extreme flux divergences and as a result the times to failure obtained from these structures were always dangerously optimistic. Failure can be in the form of voids, an open circuit, high resistance, or as extrusions. To detect this latter failure mode, extrusion monitors need to be incorporated into the design.

To project wear-out lifetimes accurately, test structures must have lines and stud chains that are comparable to the minimum or worst case conditions in the product and try to simulate conditions of topography and insulator thicknesses similar to those in the product (Figure 7.1) since all of these factors have been found to be important in affecting electromigration lifetime. Figure 7.1a shows a top view of a line test site, where extrusion monitoring lines are placed adjacent to the test structure to detect extrusion fails. A cross-section of a via chain test structure is shown in Figure 7.1b, which shows two levels of layered Ti/Al–Cu connected by a tungsten stud. Extrusion monitors are usually used in one or both wiring levels (not shown in the cross-sectional figure). In the case of copper wiring, the structure built using a dual damascene process would have a non-Cu liner (Ta, TaN, etc.) interposed between M1 and Via 1, but no liner between Via 1 and M2. Techniques that compare the integrity of the film, such as lifetests and resistivity studies, are routinely used to compare the rates of atomic transport between different sets of films.

The results of lifetime experiments are almost always expressed as the median time-to-failure (MTF, t_{50}) and the standard deviation (σ) of a lognormal distribution of failure times of nominally identical samples. The relationship of this time-to-failure at accelerated conditions (higher temperature and current density) is expressed in Equation 7.5a, commonly known as Black's law.

Some engineers have used a Weibull distribution, but there is no physical justification for its use. Although a pure lognormal distribution has conceptual problems, there is theoretical justification for a lognormal type of distribution (Lloyd and Kitchin, 1991). Unfortunately, the failure distribution is often not a single mode, but may be bimodal or even multimodal (Ogawa et al., 2001; Fischer et al., 2001; Liu et al., 2004). The problem is that the extrapolation to small probabilities, necessary when relating test structure results to real product chips (scaling), becomes highly unreliable. If the calculated sigma is high (of the order of or exceeding 0.7), it is likely that the distribution is indeed bimodal, with an early failure population that may or may not have the same failure kinetics as a later mainstream failure mode. If a single failure mode is assumed, the erroneously high sigma will extrapolate to a very pessimistic time-to-failure at small failure percentages, which is grossly unrealistic. The danger here is that using this extrapolation will unrealistically limit design rules which will, in turn, adversely affect device performance using the materials and feature sizes being investigated.

Kinetic studies must be performed to determine the terms in Equation 7.5a that must be used to relate the failure times to operational conditions. Usually t_{50} is measured at constant current density as a function of temperature in order to determine E_a. Correspondingly, t_{50} measured at different current densities at constant temperature is used to determine the current exponent (n). In practice a large number of identically prepared thin-film interconnects are tested at elevated temperature and current density until failure (in most cases both open and short circuit failures are recorded). Due to the statistical nature of electromigration, a range of failure times occurs at a given temperature and current density (see Figure 7.2). Typically, a number of test structures are stressed under accelerated temperature and current density conditions. A test specimen is considered to have failed if a preset criteria is met; e.g., the criterion can be a change in resistance or an electrical short

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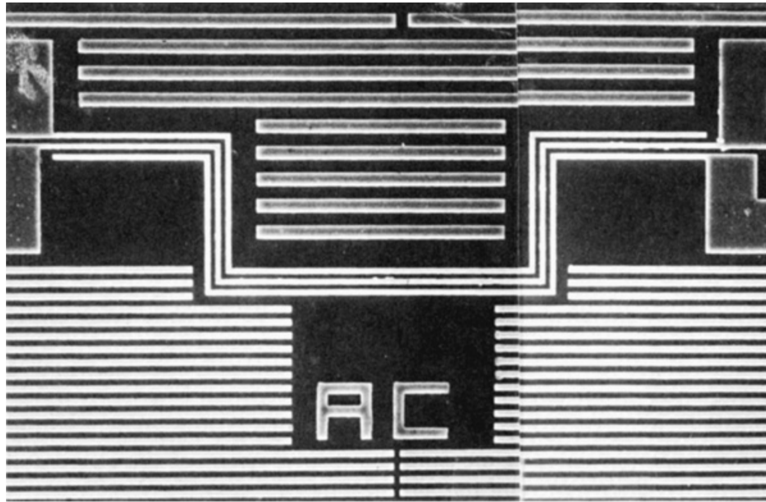
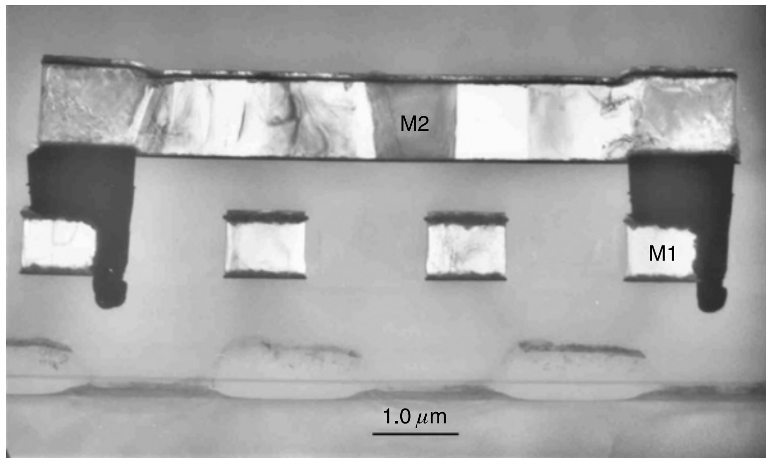


(a)



(b)

Figure 7.1 Electromigration testing structures: (a) single level (SEM top view) (Courtesy K.P. Rodbell); (b) multiple level (cross-sectional SEM). (Courtesy L. Gignac, IBM.)

to the adjacent monitor. The fail time (log life) is plotted against cumulative fraction failed to determine a t_{50} and a sigma for the test population. Usually t_{50} is measured at constant current density as a function of temperature from which E_a is determined; t_{50} determined from tests at different current densities at the same temperature is used to determine current exponent (n). Furthermore, the activation energy determined is an aggregate activation energy since it effectively averages over a large group of samples, which can have a variety of failure modes. Even though it offers little insight into either the atomic diffusion mechanism(s) involved or the details of possible failure mechanisms, it is a useful tool to get estimates of design guidelines and failure rates in use conditions.

The life-testing variables considered important are (1) geometric (such as shape, line length and width, multilevel vias and studs, and the type of passivation), (2) solute concentration(s), (3) temperature, and (4) current density (DC, AC, pulsed DC). The lognormal, Weibull, and Gamma life

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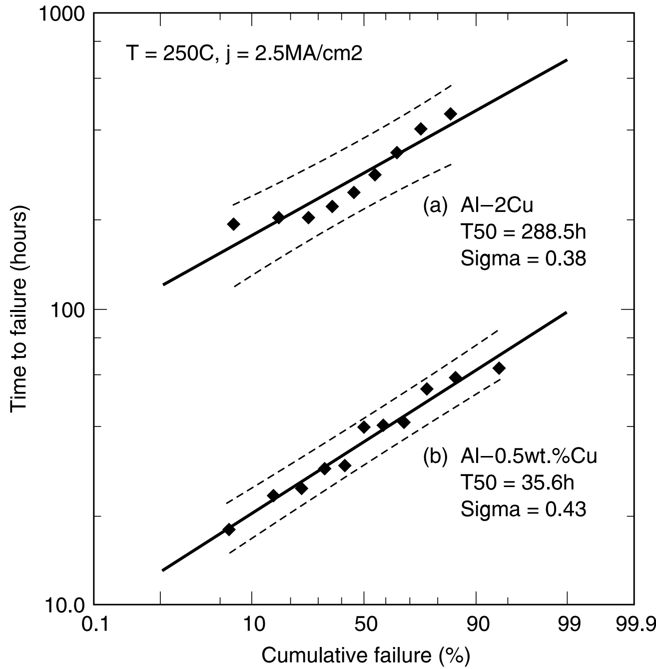

Figure 7.2 Example of lognormal electromigration failure plot.

distribution are usually sufficient to plot the data, from which the shape parameter (sigma = $\ln(t_{50}/t_{16})$, for a lognormal distribution) is calculated. A sigma > 2 implies a high early failure rate, while sigma < 0.5 implies a wear-out type failure rate. Care must be taken in the kinetic studies to avoid overstress, meaning that one not use temperatures so high that transport mechanisms are excited that would not normally dominate at use temperatures. Secondly, one should avoid current densities that induce extreme temperature gradients which can promote failure modes not seen at use conditions.

Once the acceleration parameters have been determined the acceleration factor (AF) can be calculated. If we use Equation 7.5a with $n = 2$:

$$\mathrm{AF} = \left(\frac{j_2}{j_1}\right)^2 \exp\left[\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right] \tag{7.8}$$

The projected use t_{50} ($t_{50\ \mathrm{use}}$) is calculated as

$$t_{50\ \mathrm{use}} = \mathrm{AF} \times t_{50\ \mathrm{accelerated}} \tag{7.9}$$

In this analysis it is assumed that σ at both the use condition and use population are equal to that in the field, and that the failure mechanisms are identical in both the test (laboratory) and use (field) conditions. As illustrated in Figure 7.3, small variations in the measured t_{50} can lead to big difference in activation energy, which in turn can lead to large difference in the calculated lifetimes under use conditions.

The customer has little interest in t_{50}. He or she will be more than upset by the time half the product has failed. In reality, the designer is interested in the time when only a small portion of the

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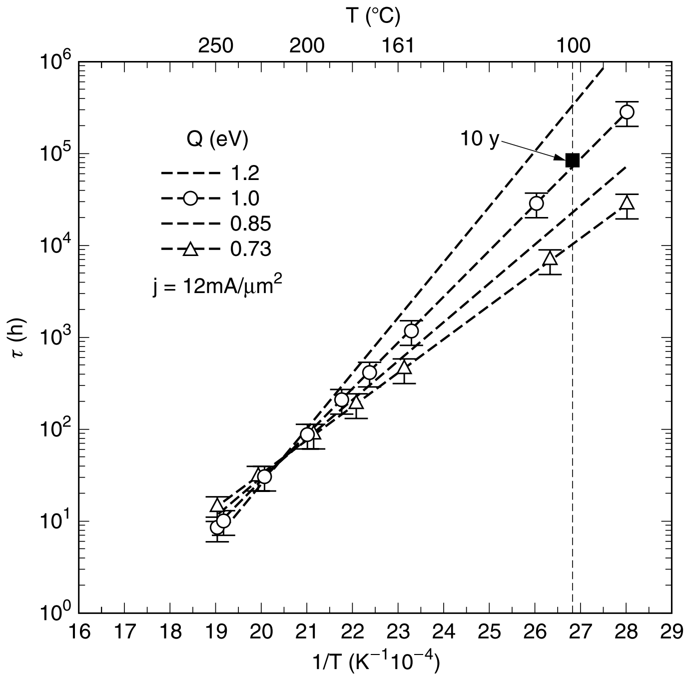

Figure 7.3 Effect of extrapolation to use conditions from experimental conditions. Small differences in experiment get magnified.

samples have failed, typically 0.1% of the population or less. Errors in the determination of sigma can exaggerate estimates of field failure rates by projecting too low or too high a value. This can have unfortunate consequences in either case, either unduly restricting designs or allowing too high a field failure rate.

The present methods for determining interconnect reliability are both costly and time consuming. For example, the use of refractory metals as discrete layers in Al and Cu metallization has produced samples that can withstand more than 5000 hours of accelerated lifetime testing at high oven temperatures (typically greater than 200°C) and high current densities (e.g., $>10^6$ A/cm^2). Higher temperatures and current densities cannot be used lest the failure modes become irrelevant. Therefore, faster techniques have been proposed; including SWEAT (Standard Wafer-Level-Electromigration Accelerated Test; Root and Turner, 1985), BEM (Breakdown Energy of Metal; Hong and Crook, 1985), WIJET (Wafer-Level Isothermal Joule Heated Electromigration Test; Jones and Smith, 1987), TRACE (Temperature Ramp Resistance Analysis; Pasco and Schwarz, 1983), assorted pulsed-current techniques (see, e.g., Scorzoni et al., 1991), and noise measurements (Chen et al., 1985a; Koch et al., 1985).

In all of these tests it is doubtful that the results can be used to estimate reliability at use conditions. In fact, a review of the literature will reveal contradictory conclusions and disputes that have gone on for decades (Lloyd, 1992). However, if actual failure times are not required, kinetic parameters, such as the activation energy, can sometimes be obtained in relatively short times.

In the $1/f$ noise technique, the noise spectrum, $S(f)$, of a thin metal film may be described as a sum of its thermal and current (excess) noise components (Vossen, 1973):

$$S(f) = 4kTR + KV^2/f\alpha \tag{7.10}$$

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where R is the resistance of the film, K is a constant dependent on film microstructure, V is the voltage across the film, f is the frequency of measurement, and α is a constant which describes the frequency dependence of the excess noise term. When the DC biasing current is small and/or the film temperature is low, the measured noise spectra exhibit a $1/f$ frequency dependence. However, at high film temperatures and current densities, a noise component that depends on $1/f^2$ can dominate the spectrum and may compromise the conclusions. Measuring the temperature dependence of the $1/f$ noise can produce an activation energy that is identical to that measured for grain boundary diffusion and electromigration. The experiments can be accomplished in only a few hours, making this technique attractive.

7.2.3.1 Thermal (Stress) Voiding

Metallization processing can expose an integrated circuit to temperatures of more than 500°C. Since the metal conductors are confined in dielectrics that have substantially different coefficients of thermal expansion (CTE), these temperature excursions can produce thermal stresses that are extremely high. The thermal stress (σ) induced in the conductor will be

$$\sigma = E\Delta\alpha\Delta T \tag{7.11}$$

where $\Delta\alpha$ is the difference in CTE between the metal and the passivation and ΔT is the difference between the passivation deposition and the measurement temperature. E is an appropriate modulus of elasticity.

Numerically, thermal stresses are far in excess of the yield strength. The reason this is possible is that the system is constrained in three dimensions. In order to accommodate the thermal strain, the stresses are primarily hydrostatic with the maximum deviatoric component being the yield stress. Hydrostatic stresses cannot be relieved without a volume change. At use conditions, the stress is tensile and the relief of tensile stresses can only be accomplished by the nucleation and growth of voids. This is obviously not a good thing.

Thermal voiding can be a major problem in passivated Al metallization, especially with stiff dielectrics such as sputtered SiO_2 or SiN_x and has also been observed in Cu metallization.

7.2.3.2 Effect of Thermal Stresses on Electromigration Failure

Since it has become pretty well established that electromigration-induced void failure occurs when the stress of a conductor reaches a critical level, if the stress in the conductor is increased by thermal history prior to the test, the failure time will be correspondingly affected. If the stress is tensile, as it almost always is, the critical stress for damage nucleation will be reached with either a smaller stress gradient in a given time implying a lower current density, or in a shorter time at a given current density. In addition, when a void is formed, the surface of the void must be stress free, so that when this happens, there will be a momentary stress gradient that will enable the electromigration-induced stress to be dumped into the void, resulting in rapid void growth immediately following void nucleation (Lloyd, 1999b).

This inflationary growth stage of the void is responsible for the $1/j^2$ dependence on electromigration failure whenever there is no redundant conductor layer beneath the conductor line. When there is no opportunity for the barrier layer to conduct electricity, the rapidly formed void will produce an open circuit without waiting for any appreciable void growth. If the redundant conductor can delay this catastrophic immediate failure, it may take some time to form the void and the time to failure will incorporate void growth and consequently a lower current density exponent will be observed. Not only will the voids form more easily with thermal tensile stresses present, but the

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eventual void size will be larger. Conditions that may not result in resistance increases that would promote failure in the absence of thermal stresses may be found to be a problem when they are present. Thermal stresses can also negate any advantage from the Blech length effect (Lloyd, 1999b).

7.2.3.3 Thermal (Stress) Voiding Testing Techniques

Traditionally, thermal voiding is studied by annealing samples at temperatures where diffusion is reasonably rapid and the stress in the film is high enough to provide a driving force for void nucleation and growth. Since atomic mobility is thermally activated, e.g., very sensitive to temperature (faster at higher temperatures), and the driving force is reduced as temperature is increased, the temperature-dependent behavior is quite different from other diffusion-related phenomena (Lloyd and Arzt, 1992). In contrast to electromigration that is always faster as temperature is increased, for the case of thermal voiding there is an intermediate temperature where the effect peaks. Beyond this optimum temperature the severity of voiding does not increase. Even though the mobility is greater, the driving force can be reduced to the point where voids will not nucleate. At room temperature, the driving force is extremely high, promoting void nucleation, but the void growth rate very slow. Finding the optimum temperature and understanding the damage kinetics are critically important in interpreting test results and relating them to use conditions.

One method to test for stress voiding is to hold the samples at an intermediate temperature and carefully monitor the resistance. The problem with this method is that there is very little resistance change with damage until very near failure. Additionally, there can be considerable voiding with no measurable resistance change and these voids can later be important in reducing the EM lifetime.

Another common method is to cycle the temperature between room temperature and some elevated temperature, but it is questionable whether this promotes damage more than holding at the optimum temperature and, in fact, it can be convincingly argued that cycling the temperature is not as severe a test as an isothermal hold.

Decelerating the results to use condition requires an appropriate model. Since the driving forces in thermal stress voiding are a function of temperature, the activation energy that is measured must be calculated carefully. Stress voiding is a diffusion-related failure mechanism and in some way will follow the Einstein relation (Equation 7.2). The driving force for void damage is proportional to the difference between the temperature where the system is stress-free, presumably somewhere between the temperature at which the passivation was applied and the measurement temperature. The stress will be tensile, so that the vacancy concentration will be elevated with respect to a stress-free material by an amount determined by the chemical potential (μ_{th}):

$$\mu_{\text{th}} = \sigma\Omega = \frac{\Omega E \Delta\alpha (T_{\text{e}} - T)}{(1 - \nu)} \tag{7.11a}$$

where $\Delta\alpha$ is difference in the thermal coefficients of expansion between the metal and the passivation, E is Young's modulus of the passivation layer, ν is Poisson's ratio, T_e is the temperature at which the metal is in a stress free state, T is the measurement temperature, and Ω is the activation volume.

If the failures occur long before all the thermal stress is relieved, the time-to-failure can be approximated as proportional to the product of the mobility and the chemical potential. Thus, the correct method to decelerate stress voiding failure times is to modify the Arrhenius relation as follows:

$$\text{AF}_{\text{SV}} = \left(\frac{T_{\text{e}} - T_1}{T_{\text{e}} - T_2}\right)\left(\frac{T_2}{T_1}\right)\exp\left[\frac{E_{\text{a}}}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right] \tag{7.12}$$

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This is different from a pure Arrhenius treatment. In fact using a pure Arrhenius relationship will result in optimistic predictions of the stress voiding performance. The problem here is that T_e is not directly obtained by experiment and must be inferred from the data. It can be expected, however, that T_e will be near the temperature at which the passivation was applied. If this approximation for T_e is used, one will see that a typical error of about 25% in the time-to-failure would have resulted had we neglected this.

7.3 BEHAVIOR OF THIN-FILM CONDUCTORS IN STRESS VOIDING AND ELECTROMIGRATION TESTING

7.3.1 Al Alloys/Layered Structures

Many factors are known to influence the electromigration lifetimes of Al films such as alloying, film geometry, and microstructure. An effective reduction in hillock formation and enhanced reliability is obtained by alloying Al, e.g., Al–Cu (d'Heurle et al., 1972), and multilayered structures of Al (or Al alloys) with a layer (or layers) of a refractory metal (Howard et al., 1978; Gardner et al., 1985). In Al–Cu alloys the electromigration lifetime is a function of Cu concentration, increasing as the Cu content increases from 0 to 4 wt% Cu (Ames et al., 1970). The role of Cu in increasing the electromigration lifetimes in Al–Cu alloys has never been unambiguously determined. It has been proposed that Cu atoms in solid solution preferentially migrate before Al in an electric field, thereby improving the electromigration behavior; e.g., Al atoms will not electromigrate until the Cu is depleted (Rosenberg, 1972). Another proposal is that θ-phase (Al_2Cu) precipitates at Al grain boundaries inhibit void growth and limit vacancy migration and stabilizes the Al grain boundaries (Frear et al., 1990). Furthermore, annealing conditions affect the shape and distribution of precipitates in AlCu alloys (Frear et al., 1991; Colgan and Rodbell, 1994) which controls the resultant film stress and grain size and has a strong influence on electromigration behavior.

In pure Al (Knorr et al., 1991; Knorr and Rodbell, 1996) and AlCu (Rodbell et al., 1992) film texture was shown to affect the EM reliability of single level structures without interlevel vias or studs. The role of local grain misorientaion in Al electromigration (Hurd et al., 1994; Longworth and Thompson, 1991) and stress voiding (Kordic et al., 1993) shows that local flux divergences are often seen at, or near, damage sites. These data imply that one may want to control the local film texture by suitable control of the film deposition process.

High creep strength aluminum alloys, such as Al–Pd, have been found to have excellent electromigration and stress-induced migration resistance as well as being less susceptible to corrosion compared to AlCu films (Onuki et al., 1990; Rodbell et al., 1993). However, the benefit of highly textured lines is overshadowed by the significant degradation of lifetimes (Estabil et al., 1991) measured for multilevel structures with W vias. Joule heating, solute diffusion, electromigration, and flux divergences at via/conductor interfaces must be considered (Filippi et al., 1996; Korhonen et al., 1993).

Where Al alloys are still employed, sputtered Al–low Cu (~0.5 wt% Cu) is in common use. It generally consists of either a Ti or a TiN underlay, although Ti 10%W is also often used. The AlCu conductor is usually ~0.5 μm thick and capped by a TiN layer, approximately 30 nm thick. These films are patterned by reactive ion etching, and show both a low susceptibility to corrosion and a low resistivity. The electromigration behavior of single level lines in SiO_2 is good (e.g., Rodbell et al., 1991), but this is illusory. In a multilevel stack with W vias, the lifetime is reduced significantly. The reduced lifetime is due to the presence of an absolute flux divergence at the W stud/Cu interface, where Cu is transported away from the via and cannot be replaced since diffusion through W is essentially nonexistent. Cu becomes depleted at the W/Cu interface, and, as the Cu moves away from the interface, rapid Al diffusion occurs in the Cu-depleted region. This induces a stress

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gradient that eventually produces the threshold failure stress at the interface (Lloyd and Clement, 1996). This failure mechanism is not seen in single level samples without vias because there are, generally, few abrupt flux divergence sites in single level structures. This is the main reason that any test structure used for a qualification must include vias or contacts.

Table 7.1 contains electromigration T_{50} data for several Al conductor systems reported in the literature.

The role of the TiN underlay in improving electromigration lifetime is a curious one. The most important effect is that the TiN under the Al alloy acts as a redundant conductor so that the generation of a small void will not result in an open circuit. The damage must grow to the point where the resistance becomes so high that the circuit fails. This results in a time to failure that is less dependent on nucleation and in many cases is dominated by the growth of voids to fatal size. When this occurs, the dependence on current density of the failure time becomes more growth dominated ($n = 1$) than nucleation dominated ($n = 2$).

Another benefit of Ti underlayers is the improved crystallographic texture of the subsequently deposited Al alloy films. By relating grain boundary angle to diffusivity both along grain boundaries and on grain surfaces one may be able to determine the optimum microstructure required to minimize mass transport in fine lines. A tight (111) texture in Al means that most grains have (111) planes parallel to the substrate. Viewed in the direction normal to the film plane, most grains differ from each other only by a rotation, which would produce (111) tilt grain boundaries perpendicular to the film plane. For low-angle misorientations (less than 15°), these boundaries are composed of a vertical array of parallel edge dislocations. Since in this situation the direction of fastest diffusion (along dislocation cores) is orthogonal to the film plane, grain boundary diffusion is expected to be slower than in a film with poorer texture (e.g., a wider range of misorientations). High-angle misorientations generally produce faster diffusivity paths (except for a limited number of special boundaries, known as coincident site lattices (CSL), which behave like low-angle boundaries).

For electromigration and stress voiding, damage tends to occur heterogeneously at grain boundaries, suggesting that the important aspect of texture is its influence on the distribution of grain

Table 7.1 Survey of Electromigration Lifetimes for Al Metallization

Alloy	Resistivity (μΩ-cm) 1 h, 400°C Forming Gas	$t_{(50\%)}$ (h) at 250°C, 2.5 MA/cm^2
Al–0.5% Cu [a]	3.5	9000
Al–0.5% Cu [b]	3.4	12000
Evap [c]	3.7	400–500
Evap [d]	3.8	400–500
Cr/Al–4% Cu	3.0	400
Al	2.8	15
Al–0.5% Cu	2.9	50
Al–1.2% Si–0.15% Ti	3.1	23
Al–1.2% Si [e]	2.9	156 [f]
Al–1% Ti	6.6	2
Al–Si/Ti [g]	3.1	300 [f]

[a] Sputtered 4250 Å A10.5% Cu/1500 Å $TiAl_3$/4250 Å A10.5% Cu; annealed in forming gas at 400°C.
[b] Sputtered 700 Å $TiAl_3$/8500 Å A10.5% Cu/700 Å $TiAl_3$/250 Å A10.5% Cu and annealed in forming gas at 400°C.
[c] Evaporated 4250 Å A10.5% Cu/1500 Å $TiAl_3$/4250 Å A10.5% Cu and annealed in forming gas at 400°C.
[d] Evaporated 700 Å $TiAl_3$/8500 Å A10.5% Cu/700 Å $TiAl_3$/250 Å A10.5% Cu and annealed in forming gas at 400°C.
[e] *Source*: From Fisher, F., Siemens Forsch-U. Entwickl-Dec. 13, 21 (1984).
[f] 150°C, 1 MA/cm^2, unpassivated. Ibid.
[g] *Source*: From Gardner. D. S., T. L. Michalka, P. A. Flinn, T. W. Barbee Jr., K. C. Saraswat, and J. D. Meindl, Proc. 2nd IEEE VMIC, 1985, pp. 102–113.

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boundary misorientation angles. In electromigration, damage occurs at flux divergence sites where material flow into and away from a damage region is not balanced. This can be due to aspects of the film microstructure, including grain size, precipitates, and crystallographic texture, or to physical constraints such as the presence of blocking boundaries (e.g., W vias). Table 7.2 summarizes the activation energy determined from electromigration studies on aluminum with different grain sizes and structures. From a crystallographic texture viewpoint one would like to have fewer number of off-(111) grains since flux divergences will form at all off-(111) grains in an otherwise (111) textured film. In stress voiding, however, one may want a uniform grain structure with regions of off-(111) oriented grains to serve as locations for strain relief. In a perfect fiber texture one can expect a small uniform strain in all grains; therefore a local nonuniformity in strain may result in rapid void formation in nearby grains or grain boundaries. In a weakly textured film, however, many sites exist to absorb strain making an individual grain boundary or grain less susceptible to void nucleation and growth. The reaction between thin films of Al, AlCu, and Ti has been extensively investigated: see Colgan (1990) for a comprehensive review. In most reports the initial phase formed was found to be $TiAl_3$ (see Table 7.3); however, Howard et al. (1976) observed Ti_9Al_{23} (in addition to $TiAl_3$) in evaporated films, annealed between 325 and 440°C. The Ti_9Al_{23} subsequently transformed to $TiAl_3$ at 440°C. A cubic metastable phase of $TiAl_3$ has also been reported by Hong et al. (1988). This phase was found in bi- and multilayered, evaporated and coevaporated, samples which had been annealed at 350°C. At 400°C the metastable phase was found to transform to the equilibrium tetragonal phase.

7.3.2 Copper

In the latest high-performance integrated circuit technologies, copper has become the conductor of choice (Edelstein et al., 1997; Hau-Rige, 2004). This choice as a replacement for Al–Cu is not only for its lower resistivity, but also its higher melting point which implies better potential electromigration resistance. However, we have found that the potential of improved elecromigration performance of copper can be achieved only with a critical control of film microstructure and purity.

Table 7.2 Electromigration Activation Energy for Aluminum Thin Films

Activation Energy (Q) (eV)	Grain Size (μm)	Method
0.74 ± 0.08	4	Transported volume
0.51 ± 0.10	2	Life test
0.73 ± 0.05	8	Life test
0.48	1.2	Life test
0.84	8	Life test
0.3–1.2 [a]	—	Life test
0.55	—	Life test
0.51 ± 0.10	—	Life test
0.34	~1	Life test
0.46	~5	Life test
0.41	~1	Life test
0.70 ± 0.20	0.5–several	Transported volume
0.63	—	Transported volume
0.70	—	Transported volume
1.22	Single crystal	Transported volume
0.5–0.6	—	Resistance
0.5–0.6	—	Resistance

[a] Thickness dependent.
Source: From Learn, A. J., *J. Electrochem. Soc.*, 123, 6, 1976. With permission.

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Table 7.3 Thin-Film Ti–Al(Cu) Intermetallic Formation

Film(s)	Phases Formed/$\Delta + H$ (eV)[a]	Range(°C)	Reference
Evap. Al/Ti/Si	$TiAl_3$/1.9(Al), Ti_7–$Si_{12}Al_5$	350–475	Bower (1973)
Evap. Al/Ti	$TiAl_3$, Ti_9Al_{23}(< 440°C)	325–475	Howard (1976)
Evap. Al/Ti	$TiAl_3$, Ti_8Al_{24}	580–640	van-Loo (1973)
Evap. AlCu/Ti	$TiAl_3$/1.6(Al), 2.1 (1% Cu)	375–450	Wittmer (1985)
Evap. AlCu/Ti	$TiAl_3$/1.7(Al), 2.2 (0.25 at % Cu)	350–500	Tardy (1985)
Evap. AlCu/Ti	$TiAl_3$/1.8(Al), 2.4 (3 at % Cu)	300–500	Krafcsik (1983)
Evap. Al/Ti	$TiAl_3$/1.9–2.0 (Al)	460–515	Zhao (1988)
Evap. Al/Ti	$TiAl_3$	400–550	Thuillard (1988)
Sput. Ti/Al/Si	$TiAl_3$, Ti_8Al_{24}, unknown[b]	380	Han (1985)
Sput. AlCu/Ti	$TiAl_3$/1.7(Al), 2.1(4% Cu), Ti_9Al_{23}	320–550	Ball (1987)
Evap. Al/Ti	$TiAl_2$(>350°C), Ti_9Al_{23}(>500°C)	300–500	Fujimura (1989)
Evap. Al/Ti	Cubic metastable $TiAl_3$, $TiAl_3$	350–400	Hong (1988)
Evap. AlCu/Ti	$TiAl_3$	400–425	Slusser (1989)
Sput. Al/Ti	$TiAl_3$	300–520	Ben-Tzur (1990)
Sput. Al/Ti	$TiAl_3$1.8(Al), 2.2(2% Si)	400–500	Nahar (1988)

[a] Activation energy for reaction (from Arrhenius plots).
[b] Tetragonal ($a = b = 5.782$ Å, $c = 6.713$ Å).

Table 7.4 Survey of Electromigration Activation Energies for Cu Thin Films

Film	Technique	Activation Energy (eV)	Reference
Cu/W	Drift velocity	0.66	Hu (1992)
Cu–TiW	Electromigration	0.54	Kang (1993)
Cu (large grain)	Electromigration	1.25	Nitta (1995)
Cu (small grain)	Electromigration	0.86	Nitta (1995)
Cu	1/*f* noise	1.1	Rodbell (1991)
Cu–Sn, Zr	Drift velocity	1.1–1.3	Hu (1995)
Cu	Drift velocity	0.75	Hu (1995)
Cu Wire/W stud	Electromigration	0.83–1.05	Yokogawa (2001)
Cu/SiN_x cap/low-e dielectrics	Electromigration	0.8–1; dielectric layer no effect	Lee (2004)
Cu	1/*f* noise	0.8–0.95	Emelianov (2003)
Cu	Highly accelerated lifetime; 425°C	Bimodal; one modal 0.81	Aubel (2003)
Cu capped with CoWP, Ta/TaN SiN_x, SiCNH	Electromigration	CoWP cap, 2; Ta/TaN cap, 1.4; SiN, 0.85–1.1	Hu (2004)

The data for copper in Table 7.4 have been expanded to include some recent results. There are too many reports to include all of them here, but the activation energy values of various studies seem to be in a narrow band of 0.8 to 1 eV, and conclusions on the effect of capping films, low-dielectric insulators are also generally similar.

In terms of electromigration, the major materials difference is in the way the surface oxidizes. Al forms a tough, very adherent oxide that is nearly impossible to reduce. It is also a highly refractory material, making it an excellent diffusion barrier. Because of its highly adherent nature, diffusion along the Al/oxide interface is also extremely sluggish. Thus, Al and Al alloys are limited to grain boundary or lattice diffusion. Cu, in contrast, does not form a stable oxide layer. This makes

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for both a less effective diffusion barrier and, correspondingly, a more active diffusion pathway along the metal/oxide interface as compared to Al alloys. Therefore, the increase in melting point from Al to Cu does not necessarily mean that the diffusion activation energy will correspondingly increase. The major diffusion pathway in Al alloys is the grain boundary, whereas in Cu it is the Cu/oxide interface. As it turns out, metal/oxide interface diffusion in Cu is comparable to grain boundary diffusion in Al alloy grain boundaries.

Another consequence of the lower oxidation potential of Cu with respect to Al is that the diffusion of Cu through dielectrics is much faster than Al. Since the heat of formation for Al oxide is so great, Al atoms have great difficulty diffusing through oxide dielectrics without being captured by an oxygen atom and forming an oxide. Cu does not react so readily and, therefore, diffuses without this restriction. To make matters worse, in an electric field, Cu will diffuse as an ion instead of as a neutral atom. The diameter of a Cu^{+} or Cu^{2+} ion is much smaller than that of the neutral atom and, therefore, diffusion through dielectrics is correspondingly faster. As a result, Cu interconnections require a liner to ensure that there will be no appreciable Cu penetration into the dielectric.

7.3.2.1 Interfacial Electromigration

The most commonly used liner material is Ta. The adhesion between Ta and Cu is quite good as long as the surface is not oxidized, and it has recently been determined that interfaces that exhibit exceptional adhesion also show very sluggish diffusion (Lloyd and Clement, 1995; Lane et al., 2003). Therefore, with Ta liners, the interface is shut off for diffusion in a fashion similar to that of the Al/oxide interface. The choice of liner is critical for the electromigration resistance of Cu metallization.

Frankovic and Bernstein (1995) measured the electromigration lifetime of a 50 μm long 82 nm thick evaporated Cu conductor deposited onto 8 nm of Ti as a liner. At a current density of 5×10^7 A/cm^2, they found no fails at 100 hours. From this performance, they estimated the MTF of evaporated Cu with a Ti liner is at least 2 to 4 orders of magnitude better than Al–Cu.

Rodbell et al. (1991) used a two-frequency AC bridge to measure the $1/f$ noise in Cu films with a Ta liner as a function of temperature. $1/f$ noise has been shown to be related to electromigration and, correspondingly, self-diffusion (Koch et al., 1985). The activation energy determined was 1.1 eV which attests to the sluggish nature of diffusion along the Ta/Cu interface. Hu et al. (1992) used drift velocity measurements on 0.4 μm sputtered Cu/W structures, and determined that the activation energy for drift velocity was 0.66 eV. Cu and W neither intermix nor form intermetallic compounds, and consequently the adhesion is poor. Therefore, this result is not surprising and points to the importance of choosing a proper liner for electromigration reliability.

Kang et al. (1993) studied CVD copper in a variety of structural forms: Cu/TiW, Cu/SiO_2, TiW/Cu/TiW, W/Cu/TiW, SiO_2/Cu/TiW, and a buried Cu/TiW. As-deposited Cu grains were in the 0.1 to 0.2 μm range and grew to 0.2 to 0.4 μm range on annealing at 350°C. The EM activation energy for Cu/TiW was 0.54 eV and the sandwich structures showed an activation energy ranging from 0.32 to 0.41 eV. These low activation energies clearly suggest that some kind of surface diffusion was operating and that none of the interfaces studied were of much value.

Unfortunately, the fine geometry of high-performance integrated circuits necessitates processing schemes, such as CMP and damascene patterning, that do not allow a liner on the top surface of a conductor. Therefore, mass transport and electromigration will be dominated by the properties of this top interface (Hu et al., 1999). It has been shown that the effectiveness of this interface as a diffusion pathway is determined by how well the two components of the interface adhere to each other (Lane et al., 2003). The activation energy for diffusion is directly dependent on the energy required to separate the interface. Thus, the reliability of a conductor is greatly enhanced by the choice of an adherent capping layer.

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Recent experiments have shown that the best results are obtained when an adherent metallic layer, such as electroless CoWP, is applied to the surface before deposition of the interlevel dielectric. In such a case, a very thin (~10 nm) layer is completely sufficient to entirely stop all interfacial diffusion. This is especially valuable in narrow lines, where bamboo Cu grain structures exhibited bulk like activation energies for failure, which makes this system essentially immortal with respect to electromigration failure (Hu et al., 2003).

Because the Cu interfaces are such an easy pathway for diffusion, one of the important properties of a capping layer is that it must be a good diffusion barrier to oxygen. Any oxygen that is allowed to diffuse to the Cu surface will degrade the adhesion leading to an increase in diffusion and a reduction in electromigration lifetime (Hayashi et al., 2003; Chen et al., 1999; Wang et al., 1999). Poor cleaning practices prior to the application of a cap layer have also been found to degrade the Cu EM lifetime (von Glasow et al., 2003).

7.3.2.2 Deposition Method and Electromigration

Aside from these effects, the most important contributor to electromigration resistance in Cu conductors was, surprisingly, found to be in the method of deposition. Evaporated, sputtered, and CVD Cu films were all found to be inferior to electrodeposited Cu films.

Not all of the studies were easy to understand. Nitta et al. (1993) studied electromigration and grain growth using ion bombardment and thermal anneals in 1 μm thick Cu(111) and Cu(100) films. The film resistivity in all films was ~1.76 μΩ cm, close to that of bulk Cu. The test structures were very wide, 4 to 5 μm, 80 μm long and were cycled between 0 and 10^7 A/cm^2 with active cooling of the test specimen. The maximum temperature from Joule heating was estimated to be between 100 and 200°C. For large grain copper they found the activation energy for electromigration to be 1.25 eV; for as-deposited fine-grained films the activation energy was 0.86 eV. Since the activation energy for grain boundary diffusion for Cu is on the order of 1.2 eV, this result is quite puzzling. Hu et al. (1995) used drift velocity measurements on both evaporated and CVD deposited copper films and found the activation energy in both cases to be 0.75 eV, suggesting that the interface or the surface is the primary diffusion pathway and that grain boundary diffusion is unimportant.

The addition of Ma to Cu degraded the electromigration lifetime, which was attributed to its inhibiting effect on grain growth. Small additions of Sn and Zr to Cu films increased the activation energy of Cu films (from drift velocity) from 0.75 to 1.1–1.3 eV, in this case suggesting that the alloying elements somehow shut off the surfaces to diffusion. Since both metals are effective oxide formers, the formation of an oxide layer of the alloying component may be the likely reason.

7.3.3 Role of Passivating Films

There is general agreement that a rigid, defect-free dielectric overcoat increases the electromigration lifetime, at least in Al alloy conductors. Since the conductors at every level of a MLM structure must be isolated by such dielectrics, this is fortunate.

Increased lifetime due to overcoating Al and Al alloy conductors was discovered early in the study of electromigration (Black, 1969b). Anodization of Al led to increased lifetime and this was attributed to a naïve concept of vacancy supply (Learn and Sheperd, 1971). Grain growth observed during the deposition of glass passivation was held responsible for increasing electromigration lifetimes (Blair et al., 1970) in one particular case, but the principle reason for the increased lifetime was proposed by Ainslie et al. (1972) who stated that it was the mechanical constraint exerted by a coating that was important in increasing lifetimes. The benefit was due to the effect of pressure

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gradients (backflow) on reducing the driving force for mass flow as well as providing a compressive stress that would reduce the mobility. Therefore, to reduce electromigration damage, the coating must have good mechanical properties and should be defect-free (Lloyd et al., 1982). Stated somewhat differently, a restraining (strong) passivation layer would permit accommodation of higher stresses, which are built up in the conductor during the passage of current (Blech and Herring, 1976) and in this way reduce diffusivity of metal atoms (Lloyd and Smith, 1983). It has been shown that a more rigid passivation, which should resist the formation of the local hillocks and voids formed during electromigration, did improve electromigration lifetime (Schafft et al., 1984). Thicker rigid films were more effective (Lloyd and Smith, 1983); with thick passivation, the failure mode is more likely to be extrusions, causing short circuits to adjacent or overlying conductors. If there are defects in the passivating film, the metal film stress will be relieved at those sites, providing flux divergences and inducing void and extrusion formation.

The stress state of the insulating film in one case was found to be unimportant (Felton et al., 1985; Yau et al., 1985). However, Schlacter et al. (1970) found that the lifetime of a conductor was diminished when passivated by a tensile CVD SiO_2; when the oxides were P-doped, the tensile stress was reduced and lifetimes of the PSG-coated conductors were longer than those of the unpassivated ones. In contrast, tensile PECVD SiN was found to increase the lifetime by about an order of magnitude over that of uncapped films (Levy et al., 1985). It is clear that the quality of the passivation is more important than the stress state. Defects in the passivation or in the conductor itself will provide stress gradient-induced flux divergences that can promote early failure (Oates and Lloyd, 1994).

Improved lifetimes and reduced drift velocity were found when the films were encased in sputtered SiO_2, but the extent of improvement depended on the deposition conditions (Grabe and Schreiber, 1983). Planarization of the dielectric overcoat was said to reinforce the sidewalls and suppress crack formation and in this way increased the electromigration resistance of the underlying conductor (Isobe et al., 1989). The lack of damage in an M1 layer in a two-level structure, in which the identical upper layer was unpassivated and failed catastrophically, was attributed to the encapsulation of the first level metal in a thick layer of (uncharacterized) deposited oxide (Martin and McPherson, 1989; May, 1991). Pramanik et al. (1994) reported that the failure mode depended on the mechanical restraint imposed by the overcoat but the kinetics of mass accumulation and depletion were unchanged. A thick rigid overcoat (in this case PECVD oxide) prevents relief of the stresses generated during EM, so they build up to the point of dielectric cracking and the metal extrudes. With a thinner, more flexible overcoat (in this case SOG plus a thinner oxide), stress relief can occur and the line resistance increases due to void growth.

Any benefit of a yielding film, such as polyimide, was attributed to its ability to supply H_2 to the grain boundaries of the metal film (Lloyd and Stegall, 1986) which had been shown to reduce grain boundary diffusion (Shih and Ficalora, 1979). However, it is not clear that hydrogen is responsible for the improvement since photoresist coating, which should have a similar effect, was found to be ineffective (Yau et al.,1985).

Nishimura et al. (1995) reported that thick (PECVD SiN/PSG) passivation on a tapered via was responsible for a decreased lifetime. They correlated the degradation resulting from increased thickness with increased thermal tensile stress which increases the diffusivity of the Al atoms. The role of tensile stress in the passivated lines was also invoked by Witrouw et al. (1995) to explain the shorter lifetimes of AlCuSi lines passivated with PETEOS SiO_2 when compared to unpassivated lines. It is not clear, however, how the stress state in the passivation, by itself, can contribute to the stress in the underlying metal film.

They also pointed out, as did Lloyd (1995) and Clement et al. (1995), the role of tensile thermal stresses in lowering the threshold for damage nucleation and the need to take into account the increased stress at lower temperatures in extrapolating from accelerated test conditions to use conditions.

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7.3.4 Influence of Low-*k* Interlevel Dielectrics

In addition to using low-resistivity Cu, advanced integrated circuits require the use of low dielectric constant materials to ensure high performance. Unfortunately, the dielectric constant is proportional to the mechanical properties, which is counterproductive for reliability, since, for low-*k* materials, such as FSG, where the interlevel dielectric is still relatively strong and stiff, there is little impact on reliability, but for the organic ultralow-*k* dielectrics and porous dielectrics, the mechanical and thermal properties of the interlevel dielectric may be a problem. For one, the low mechanical strength will not offer as much restraint as the silica-based interlevel dielectric and therefore will not allow as much advantage from an opposing stress gradient (Lee et al., 2003).

Another problem with low-*k* dielectrics is that poor thermal conductivity is also correlated with low values of the dielectric constant (Tsai et al., 2001). This will be even more of a problem when porous dielectrics come into common use and worse again when air gap structures are finally developed.

One potential failure mode observed with Cu and low-*k* interlevel dielectrics that is not present with Al or with silica based dielectrics is that time dependent dielectric breakdown (TDDB) can be a problem with interlevel dielectrics, where this was never a problem previously. With silica, TDDB is not a problem unless the fields are near the intrinsic breakdown on the order of 10 MV/cm, which is much higher than any experienced in other than in gate oxides. In the low-*k* dielectrics, fields much lower than this will produce failures in dangerously short times (Noguchi et al., 2001). In one study, it was found that the failure kinetics did not correspond to either the “E” nor the “1/E” models for TDDB and it was suggested that the kinetics are primarily dominated by statistical arguments rather than the precise physical mechanism of breakdown (Lloyd et al., 2004). At the time of writing there is very little in the published literature concerning this problem, but suffice to say this will be a topic of intense interest in the near future.

7.4 ELECTROMIGRATION BEHAVIOR OF VIA CHAINS

7.4.1 Overview of Interlevel Connectors

There are two basic types of interlevel connectors linking sequential metal levels through the interlevel dielectric layer. These have been termed “conventional” and “stud” vias at the time that the now more prevalent latter configuration was introduced. This historical nomenclature is similar to that in early aviation, where the now nearly ubiquitous tricycle landing gear was not considered conventional as was the tail wheel.

Figure 7.4 shows the tapered via structure, into which a metal is evaporated or sputtered to directly contact the underlying metal at the via opening, but the hole is not completely filled. The stud (plug) structure is shown in Figure 7.5; the walls are vertical and the holes filled by one of two processes. The stud vias are more desirable since they use less real estate. In Al alloy technologies CVD W-filled studs are almost exclusively employed. Other schemes such as CVD Al and pressure-filled vias were tried, but are not widely used.

A third scheme that has come into common practice in the finest geometries is the dual-damascene method. Here, with the use of chemical mechanical polishing (CMP) vias are made by electrodepositing the via material at the same time as the trenches and polishing off the remainder.

The disadvantage of the W-filled vias is that the via/conductor interface represents an absolute mass flux divergence. Therefore, the via is a preferred location for failure, both in the form of voids or extrusions. Conceivably, the Blech length effect could be used to preclude electromigration failure, but the high W via resistance makes this unworkable.

In the dual damascene process the metal is deposited into the vertical (via) and horizontal (trench) interconnections in one step, so that no interfacial film forms between them. In principle,

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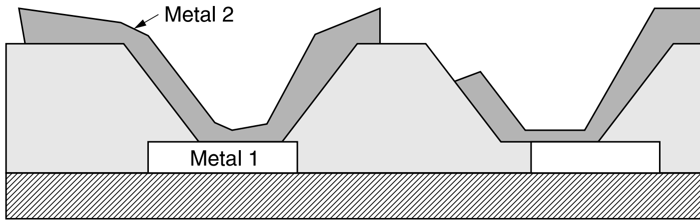

Figure 7.4 Schematic of a tapered via structure.

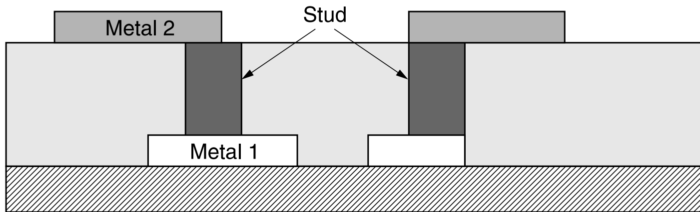

Figure 7.5 Schematic of a vertical stud interconnect between two wiring levels.

the absolute flux divergence should be eliminated. However, practice has shown that this is not the case. The presence of capping material on the lower metal layers and process-induced modifications of the surface have preserved the via as a preferred failure location.

Two kinds of test structures have been used: the Kelvin or four-point test structure which probes a single via, and via (stud) chains containing different numbers of vias (studs) and intervia (stud) spacing. The upper level may or may not be passivated.

7.4.2 Vias with No Barrier Layer in M2 Metal

Although, in principle, it is possible to create a divergence-free conventional via in practice this is seldom achieved. Contaminants such as a native oxide or other process-induced contaminants on the Al surface at the interface between the first (M1) and second (M2) metals can cause degradation due to electromigration similar to the effect of a W via or a contact to Si.

A source of trouble in conventional vias is also in the sidewalls. The step coverage in the via is never 100% and the thinning increases as the via becomes more vertical. The problem arises when the current density becomes so large that Joule heating becomes significant and produces hot spots. This, in turn, can increase diffusion locally and produce flux divergences and early failure. As the aspect ratio of the via is increased, the cross-sectional metal area at the base of the via can eventually become smaller than in the step region and thus shift the current density peak to that region. By increasing the thickness (and thus reducing the current density) of the upper metal, the current density peaks and thus the hot spots in the via can be reduced. The vulnerable regions are, therefore, the sidewall of the via and the interface between the metal levels and the via.

The effect of step coverage by the second metal (M2) has been investigated experimentally. In the absence of any barrier layer, poor step coverage has sometimes been found to be responsible for the degradation of electromigration resistance (Rathore, 1982; Matsuoka et al., 1990). Rathore (1982) used *in situ* sputter cleaning of the vias to insure the absence of a barrier (resistive) layer (Bauer, 1980, 1990) and therefore attributed high via resistance to poor step coverage. They correlated high initial via chain resistance to low electromigration lifetimes. They showed SEMs of the microcracks in M2 at the top rim of the via which confirmed the failure mechanism.

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However, according to Yamaha et al. (1992), in the range of 8 to 22% step coverage of the M2 metal, the lifetime of via chains was independent of M2 coverage. They also showed that there was an optimum sputter-clean time for lifetime improvement and attributed the degradation after that time to deposition on the interface of a thin insulating film consisting of material sputtered from the dielectric sidewall.

Kisselgof et al. (1991) showed that steps degrade electromigration lifetime more than would be predicted based only on the current density in the thinner region. Thinning that resulted in 40% step coverage would suggest a lifetime of about 20% of that of a conductor without steps based on $n = 2$ kinetics, but the observed lifetime was reduced to approximately 10%. The results were consistent across several lots.

7.4.3 Vias with a Barrier Layer in M2

The barrier layers used in conjunction with Al alloys in vias are Ti, TiN, TiW, and WSi.

There is a flux divergence at the interface between M1 and M2 due to the presence of the barrier. When electrons flow from M2 to M1, void formation at M1 can be expected since the electron flow results in metal transport away from the interface with no means of replenishing it. Conversely, metal accumulates at M2. Similarly, when the electrons flow from M1 to M2, metal accumulates at the interface at M1 (Martin and McPherson, 1989).

7.4.3.1 Tungsten Vias

The presence of a W via produces the unfortunate feature of an absolute flux divergence. The W via itself is extremely resistant to electromigration since the diffusion of W is vanishingly small at any reasonable use temperature. Therefore, the statement that we have a via failure is really that the conductor line in contact with the via fails, not the via itself. Therefore the current density in the via is unimportant except for how it determines the current density in the adjoining conductor lines.

The flux divergence at the AlCu/W interface is the main factor responsible for electromigration failure. Voids form at or close to the via interface (e.g., Kwok et al., 1990; Hu et al., 1993; Korhonen et al., 1995). In Al/Cu conductors, Cu is found to be almost completely depleted near the stud after current flow, (Kwok et al., 1990). Depletion of Al at the interface is preceded by an incubation period during which Cu is swept past a threshold distance. The kinetic process is controlled by electromigration of Cu along the grain boundaries and not by dissolution of precipitates (Hu et al., 1993). Failure occurs when the failure stress is reached at the Al–Cu/W interface in the depleted region by electromigration of Al. Current crowding at the stud–line interface has also been cited as a contributor, even though local heating calculations show that the temperature rise is insignificant (Kwok et al., 1987b; Tu et al. 2000); however, the idea that current crowding alone will contribute to lower lifetime has been challenged on theoretical grounds (Lloyd, 2001).

Estabil et al. (1991) found that the mode of failure, void-open or extrusion-short, depended on the current density in M1; as the current density decreased at constant M1 thickness, there was an increased tendency for failure by extrusion shorts.

Therefore, although the W-stud structure (e.g., Figure 7.6) satisfies many of the needs of VLSI, the electromigration performance has been disappointing. Several suggestions have been made for improving it. Grass et al. (1994) reported that using a layered structure conductor, in which the Al alloy was capped with Ti/TiN, improved the lifetime of the stud structure (as it does with stripe lifetime) and eliminated the differences due to the direction of current flow. Ting et al. (1991) reported that a conformal coating of the via hole by CVD TiN ensured a good barrier between the W plug and M1 and thus improved the lifetime.

Because of the existence of a critical current length Blech effect threshold below which no metal transport occurs during current stressing, the interstud (via) spacing would be expected to influence

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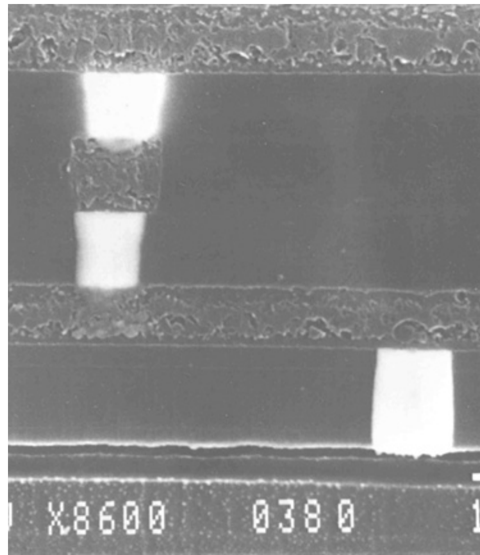

Figure 7.6 SEM cross-sectional view of the schematic of Figure 7.5. A W stud interconnects two levels of Al–Cu wiring.

the electromigration performance of a given stud (or via) chain. This effect has been demonstrated by Filippi et al. (1993) and by Aoki et al. (1994) where it was found that for interstud distances below a critical value there were no failures. The practical problem with this approach is that a price in resistance must be paid for using W studs. This price has precluded the use of this scheme for increasing electromigration lifetime.

7.5 CORROSION

7.5.1 Introduction

Basic discussions on corrosion can be found in many sources (Uhlig, 1966; Evans, 1960). Therefore, the discussions here will be limited to the corrosion of thin films used in microelectronics and their characterization.

Corrosion in thin-film wiring can be described as the (unintended) loss of conducting metal by dissolution in an electrolyte or conversion to a nonconducting form in response to an external stress, which is primarily chemical or electrochemical in nature. The external stress is usually made of a combination of the following:

1. Impurities external to the film, such as moisture or corrosive gases
2. Temperature
3. Applied voltages
4. Mechanical stresses including that caused by coatings

Corrosion reactions require the generation of an electrolytic cell having two electrodes and an electrolyte. We are most familiar with the aqueous electrolytes, but just about any material that can support the diffusion of ions can serve as an electrolyte. A metal in equilibrium with its ions in an electrolyte (half-cell) can be written as a reaction, with a characteristic free energy of

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reaction and a corresponding electrical potential. Corrosion cell potentials (electromotive forces) of many metals have been measured with respect to a hydrogen half-cell (0.0 V reference potential), and the list of values are known as the galvanic series. Corrosion cell reactions are broadly classified as:

1. Galvanic, where elements with dissimilar emfs form a cell
2. Concentration, where the differential local ionic concentration creates sites of different potentials or emfs
3. Externally impressed potential (emfs) on electrodes

Electrodes or metals with large positive values of emf are usually active in a corrosive reaction (anodic), whereas the ones that have negative emfs tend to be passive (cathodic). However, the corrosion kinetics even in a simple corrosion cell can be changed by passivity, which is when the element forms a passive surface layer, or by polarization when the local ionic concentration adjacent to the electrode is changed. Thin-film metallization used in interconnection suffers from the presence of all of the above mechanisms contributing to corrosion cell formation and to corrosion. For example, the corrosion susceptibility of thin-film conductors are influenced by the choice of metal (passivating, galvanic potential); the presence of dissimilar metallurgical junctions caused by layers or phases, and compositional inhomogeneities; the presence of electrolytes in contact with the film surface are required for the onset and continuation of corrosion. Externally impressed voltages on the conductors (biases) can accelerate the corrosion reaction.

Corrosion in thin films can be caused during processing and between process steps when residual impurities can react with films surfaces: this is known as in-process corrosion. In-process corrosion can lead to yield losses or cause reliability failures prematurely. When a functional device at the end of all processing cycles fails in use or storage due to corrosion of an interconnect, then it becomes a reliability failure.

7.5.2 Reliability Measurements/Temperature and Humidity Stressing

Unlike corrosion studies of bulk materials using metal blanks or coupons, thin films used in interconnections are usually studied using a comb-serpentine structure (Figure 7.7a), or a double maze structure of parallel meandering lines (Figure 7.7b), or maze structures separated by an insulating layer (Figure 7.7c). The maze lines can be built to the same design rules of the circuit using similar processes and structures. In addition, the adjacent lines can be electrically biased with respect to each other. The structure is usually terminated in a bond pad and mounted on a substrate. Wire bonding or other techniques are used to complete electrical connections between the substrate and the bond pad. The test chip is usually encapsulated in an organic or inorganic material and test structures on the chip are electrical biased, while the chip is under a high temperature and humidity (THV) environment. The leakage current between adjacent lines (corrosion current) is sometimes monitored and, alternatively, the test is interrupted periodically and the resistivity of the corroding lines is measured. The leakage current is a measure of the corrosion reaction rate whereas the change in resistivity is an indirect measure of the extent of corrosion. The test sample is examined using analytical tools to determine corrosive products and the extent and location of corrosion. Temperature and humidity testing is usually performed on packaged chips and is designed to test the integrity of the hermetic seal for preventing moisture diffusion and thus corrosion of the interconnects. The test conditions that are most widely used are 85°C, 85% relative humidity, with a voltage bias. Although this is a rather simple engineering test, it is very useful in assessing the corrosive potential of the test structure in the context of the integrity of the encapsulant. Sometimes high-pressure and high-temperature tests (pressure cooker) are used to accelerate corrosion failures

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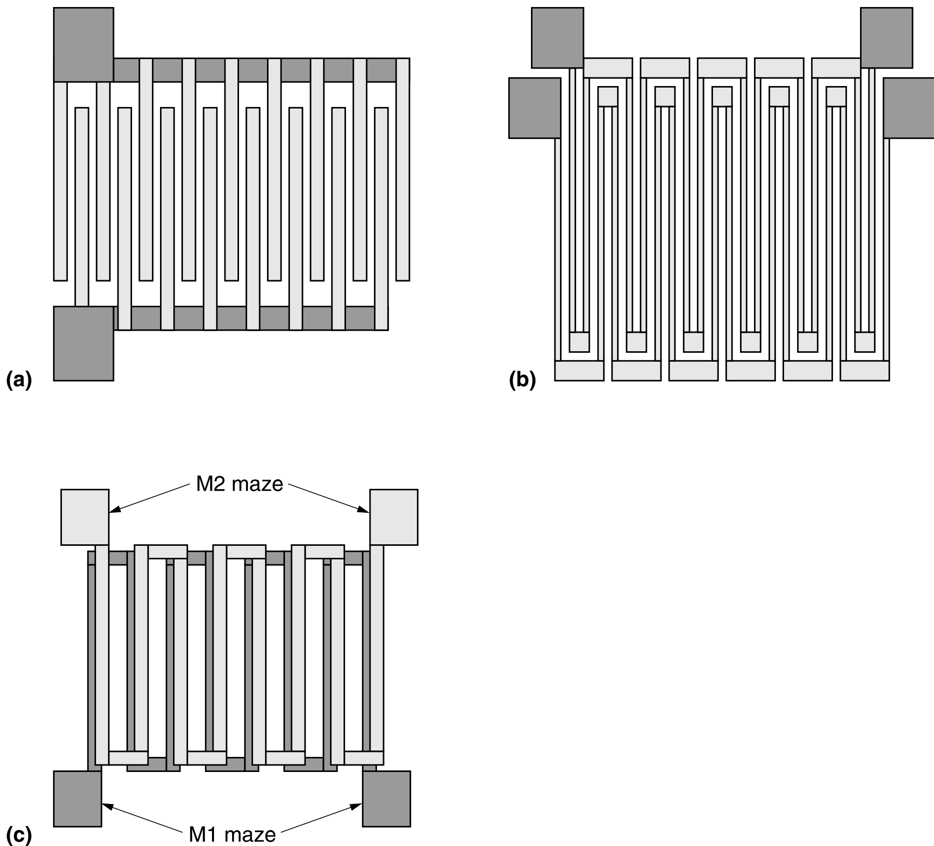

Figure 7.7 Schematic of top view of structures used in THV corrosion studies.

(Gunn et al., 1981). Typical corrosion models express fail time or lifetime, as an Arrhenius equation having an activation energy and field factors:

$$t = A\exp(-B/T)f(\mathrm{RH}, V)$$

where t is the time for failure of a percent of a test population where failure is defined as exceeding a critical resistance change or leakage current, B is the activation energy of the corrosion rate-limiting process, $f(\mathrm{RH}, V)$ is some function of the RH (relative humidity), and V is the applied bias voltage. A is the pre-exponential value in the rate equation. Since the primary purpose of these equations is to determine the acceleration factors between stress and use conditions, the primary variables used are temperature, RH, and bias voltage. The sensitivity of each variable can be determined individually and a total acceleration factor calculated.

In an encapsulated test structure, there are many steps in the corrosive failure sequence: absorption of moisture; migration of water to the film location; corrosive reaction at the metal/electrolyte interface; transport of ions under the electric field, etc. In most studies of structures that have insulator coatings, the diffusion of moisture determines the corrosion rate. Under this assumption, the activation energy is the energy for diffusion or permeation of water through the insulator. In most electronic applications, the semiconductor wires are usually well insulated and most often it is the packaging elements and exposed pads that experience corrosion failures (especially if they are not adequately encapsulated or the structures are exposed to aggressive environments).

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7.5.3 Corrosion Behavior of Al–Cu Conductors

Although Cu-based technologies are gaining ground in the high-performance arena, the most commonly used conductor for semiconductor interconnection is still Al based. Often the Al is alloyed with Cu or Si and occurs with layers of Ti, TiN, or TiW. In the context of the multilevel interconnection, even in the absence of externally impressed voltages, the lines are connected to silicon regions of different impurities and conductivities which make them susceptible for corrosion. Paulson and Kirk (1992) studied the corrosion of Al test structures coated with P-doped glass. In their study the corrosion rate of Al under electrical bias and humidity increased with the amount of P in the glass, presumably due to an increase in absorbed moisture from higher P_2O_5. Humidity had the strongest effect on corrosion rate. The corrosion product was $Al(OH)_3$. Wada et al. (1986) studied aluminum corrosion using a double layer metallization, where two mazes separated by an interlayer dielectric were stressed under a voltage bias and humidity. The vertical electrolytic current between the two mazes was monitored. The corrosion was always on the cathode, with an activation energy of 0.9 eV, irrespective of which maze, top or bottom, was biased as the cathode. When the top insulator and/or the interlayer are SiN, the corrosion diminished considerably indicating that SiN was an excellent barrier to moisture. P-doped oxide, undoped silicon dioxide, and PECVD SiN were compared for their passivation effectiveness over sputter deposited and patterned Al–2% Si in a THV stress test (Wada et al., 1989). It was found that electrolytic leakage and cathodic corrosion occurred for both doped and undoped oxide passivated samples. The corrosion was negligible in the case of SiN. The study also showed that applied bias had a strong effect on the corrosion current and the current leakage was primarily at the plastic resin and passivating layer interface. Will et al. (1987) studied *in situ* corrosion of aluminum metallization using a polymer passivation layer with pinholes. They found that the electrolyte in the gap has a resistivity 100 times lower than distilled water, which they attributed to the leaching of ionizable impurities from the polymer coating.

Intergranular corrosion in Al–4.5% Cu, called "missing Al," was seen when theta particles are overaged and enlarged (Totta, 1976). Kawal et al. (1996) studied the *in situ* corrosion behavior of age-hardened Al–Cu alloys in aqueous (dilute) hydrochloric acid and found extensive pit formation in the vicinity of second-phase particles; the dissolved Al redeposits as hydrated oxide at the local cathode. The main cathodic reaction, however, becomes hydrogen evolution rather than Al deposition. Mayumi et al. (1990) observed a high occurrence of corrosion-induced contact failure in double-level Al–Si–Cu metallization, which they attributed to the formation of large precipitates in the via holes, which served as a cathode, and promoted the dissolution of adjacent Al (anode). Corrosion susceptibility of Al–Cu and Al–Cu–Si was studied by Lawrence et al. (1990) using unpassivated metal structures. The test structures consisted of an Al alloy overlaying a Ti–W barrier layer. The Cu and Si contents were varied from 0 to 2% and 0 to 1%, respectively. A controlled concentration of NH_4Cl was used to effect corrosion. The study found that corrosion sensitivity is greatly increased when the Cu content is increased to between 1 and 2%. Addition of 1% Si to Al–2% Cu resulted in delaying the onset of corrosion, consistent with improved native oxide formation protecting the film. Weston et al. (1990) similarly observed that adding Si to Al–2% Cu reduced corrosion. This study also attributed localized surface corrosion to the galvanic action due to the presence of theta phase particles. Koelmans (1974) studied the corrosion of Al metallization in plastic-encapsulated ICs and concluded that a film of water absorbed at high relative humidity led to passivation or destructive corrosion depending on the ionic impurities present. The presence of Cl^- ions leads to poor-quality oxide at the anode, whereas Na^+ moves to the cathode and increases the pH, thereby promoting cathodic corrosion. Parekh and Price (1990) studied the effect of residual Cl levels on the corrosion of Al–Si metallization with Cu addition and TiW layering. They found that in the range of Cl contamination studied the corrosion rate was strongly influenced by the amount of residual Cl, and the galvanic cell effects of Cu and TiW were less significant.

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Rotel et al. (1991) using potentiodynamic polarization measurements compared Al–Cu lines and Al–Cu lines containing Ti and Hf layers patterned by wet and reactive ion etching (RIE) processes. The observations were: a decrease in copper reduced the corrosion rate, reactive ion-etched Al–Cu showed more corrosion compared with wet-etched Al–Cu, and Ti- and Hf-layered structures had lower corrosion resistance compared to Al–Cu alone.

7.5.4 Corrosion Behavior of Copper Conductors

Copper is increasingly being employed as an alternative interconnect material in place of Al–Cu due to its lower resistivity and electromigration resistance. Even though published accounts of corrosion studies with thin copper films in integrated circuits are limited, extensive observations exist on corrosion of thick films and bulk copper. Copper has an emf of 0.521 V in the galvanic series which makes it passive. Copper forms cuprous oxide (Cu_2O) cathodically in slightly acidic solutions and cupric oxide (CuO) anodically in alkaline solutions. Cupric oxide dissolves in dilute acids and ammonia. Cupric hydroxide is sometimes formed. Copper forms numerous complexes such as copper (of valency one) with Cl^-, CN^-, NH_3, $S_2O_3^{2-}$, which are colorless. In chlorine solutions, complexes between Cu^+ and Cl^- can lead to appreciable dissolution of copper. A summary of liquid solutions and gases that react with copper can be found in Uhlig and Revie (1985). Copper is also known to corrode in oxidizing acids and aerated solutions. In seawater and fresh water, the presence of copper oxide films determines the corrosion rate (i.e., diffusion of oxygen). The corrosion rate of copper in aerated chloride solutions is roughly an order of magnitude higher than nonaerated chloride solutions (Bjorndahl and Noble, 1984). This study, using cyclic voltammetry with disc electrodes, concluded that, in the presence of oxygen, much higher concentrations of $CuCl^{2-}$ ions are in equilibrium with Cu, which increased the Cu corrosion rates in oxygenated solutions. Rice et al. (1981) studied the atmospheric corrosion of copper and silver using coupons in a controlled ambient chamber with predetermined trace impurities of different gases such as sulfur dioxide, nitrogen dioxide, hydrogen sulfide, chlorine, hydrogen chloride, ammonia, and ozone. Copper corroded in SO_2, H_2S, Cl_2, HCl, and O_3, but the corrosion rate was very sensitive to the relative humidity and substantially increased at high humidity. The effect of organic inhibiting molecules on copper such as benzotriazole (Poling, 1970) and N-heterocyclics (Thierry and Leygraf, 1985) have been studied for passivating against corrosion. These and other similar studies are not discussed here, but interested readers can consult relevant articles since they may suggest means for protecting thin copper lines in multilevel structures.

7.6 INSULATOR RELIABILITY

7.6.1 General Remarks

Insulators for interconnect application are primarily used in a passive mode, to insulate and isolate conductors from adjacent ones and underlying silicon where so desired; and further act as a passivant to hermetically seal the conductor and devices from impurities such as water or ions that can cause corrosion of the conductors, or device instabilities. Current leakage and breakdown with use (time-dependent dielectric breakdown, TDDB) are two important reliability or quality concerns for an insulator. For a good passivating film, the insulator should be a barrier to moisture with few pinholes or defects. If the insulator is used adjacent to silicon, it is desirable that it be a barrier or a scavenger of alkaline ions. Forms of silicon dioxide are the most widely used insulators for interconnect applications and silicon nitride is used to a much lesser extent usually in conjunction with an oxide. Organic insulators such as polyimide have been used as scratch coatings and as final passivants. Increasingly, the very small features and spaces in the silicon devices are necessitating the

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use of organics, spin-on glass and other materials as gap fillers. Most breakdown fields are orders of magnitude higher than the average field experienced by insulating films used in interconnect applications. However, TDDB studies are likely to explain how defect locations start conducting and cause insulator breakdown.

7.6.2 Electrical Conduction/Leakage

A good-quality insulator without impurities or defects easily satisfies the leakage requirement of less than 1 μA typically specified for interconnect applications, as it has a large band gap and it takes very large fields to excite electrons across the gap. However, insulator properties are usually degraded by contact with electrodes, which modify the energy barriers, and by the presence of traps, ionic impurities, and charges from compositional deficiencies. Manufacturing defects lead to thinning of insulators. Poor control of deposition processes can produce off-stoichiometry films which can result in conducting islands interspersed with insulating regions. Electrical conduction mechanisms in insulators (Sze, 1981) are grouped as follows: (1) Schottky emission, the thermionic emission of electrons across the electrode-insulator interface; (2) Poole–Frenkel, the field enhanced thermally excited trapped electrons or holes into the conduction band; (3) Fowler–Nordheim, the tunneling of electrons from the metal Fermi level into the insulator conduction band; (4) injection of charge without a compensating charge across a space-charge region; (5) ionic, the migration of ions under temperature and electrical field; and (6) ohmic. All of these mechanisms are present in some combination at the temperature and electrical field used. Studies on thin oxide film suggest that at device temperatures, electron injection (Fowler–Nordheim) dominates and there is negligible hole or electron conduction. The electrode material has some effect, presumably due to the influence on electron injection. Postmetallization anneals reduce leakage. For the thickness of insulators employed for interconnection, it would be accurate to say that any measurable current is caused by defects.

Conduction in thin silicon nitride has been proposed to be caused by the Poole–Frenkel mechanism (Sze, 1967) and by trapped holes. The current is bulk controlled and shows a weak electrode and a strong temperature effect. Both silicon nitride and aluminum oxide have higher conduction at low and moderate fields compared to silicon dioxide. Most circuit applications can withstand leakage that does not contribute to unintended device switching or unacceptable voltage drops. The primary concern is leakage in the insulator, since it usually leads to breakdown within a very short period.

7.6.3 Time-Dependent Dielectric Breakdown (TDDB)

7.6.3.1 General Remarks

Dielectric breakdown has been a major concern for applications involving thin dielectrics such as gate or storage capacitors. Recently, with the advent of the low-*k* interlevel dielectrics and tighter spacing it has become an important if unanswered question as to whether it may be a real problem here as well. In the past, with the use of robust dielectric materials such as SiO_2 with breakdown fields of the order of 10 MV/cm and inter- or intralevel spacings typically ~1 μm, TDDB was simply not a reliability issue except in the gate.

One of the problems with the evaluation of TDDB data is the uncertainty in the physics of the failure process and the correct model to be used to extrapolate to use conditions from the accelerated test. For many years there has been the (in)famous E vs. $1/E$ controversy with each side making strong arguments for their particular belief system, but these all have been eclipsed in recent times by a percolation model that offers a different approach (Stathis, 2001). In the percolation model, defects are presumed injected into the dielectric with failure arriving when there are enough to produce a continuous conduction pathway.

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7.6.3.2 Test Methodology/Results

TDDB is studied using a capacitor structure which has the desired insulator sandwiched between a bottom electrode (usually silicon) and a top electrode which is usually aluminum, i.e., MOS or MIM test structures. Commonly used test sites are built on a degeneratively doped silicon substrate with the backside metallized. The top electrode usually has varying areas (dots) which is most often aluminum unless the effect of the electrode is also being studied. The most commonly used test subjects the capacitors to a constant electrical voltage (field) at different temperatures; the failure behavior with time is observed and analyzed. The breakdown population is divided into two groups, intrinsic breakdown and extrinsic breakdown. Oxides of different thickness have been studied and in one of the models, the logarithmic failure rate has been found to be proportional to the applied field where the activation energy is also affected by the electrical field (Crook, 1979; Berman, 1981). The corresponding physical model describes breakdown as the activated process. Another commonly subscribed to model predicts the failure rates to depend on the reciprocal of the field. In this 1/E model (Chen et al., 1985b; Lee et al., 1988; Moazzami et al., 1989), holes are created by electron injection and impact ionization, and the trapped holes increase the electric field at the cathode interface leading to increase in electron injection, which lead to local breakdown. In another method, the breakdowns were treated as a stochastic process (Shatzkes and AvRon, 1981); the test structures were ramped from zero to breakdown voltage at different ramp rates and at different temperatures. The fails in SiO_2 stressed under different temperatures, electrical fields, and voltage ramp rates were analyzed using a single plot of $R\ln(1 - F_{fail})$ versus F_c(cathode field). F_c is the applied field E, corrected for electron capture and release, as a function of ramp rate. Other methods of stressing without an electrode are corona discharge, laser breakdown, and e-beam-EBIC mode. Internal photoemission is used to determine barrier inhomogeneities. Prendergast et al. (1995) studied the breakdown of thermally grown oxide in the temperature range 175 to 400°C at constant fields ranging from 7 to 11 MV/cm. The breakdown data showed a bimodal distribution at moderate fields and temperatures and concluded that intrinsic breakdown data exhibited a direct E dependence and the extrinsic fail population exhibited a reciprocal E dependence. Breakdown results with defects vary widely. Shatzkes et al. (1980) studied the variability of the Si–SiO_2 interface and identified regions of low barrier heights as defects. As much as agreement on models are important for failure rate projections, there is wide variation in the breakdown results obtained from insulators with different thicknesses. Ting et al. (1991) reported that oxidizing Si in N_2O resulted in lower oxide growth and the resulting oxide showed some pile up of nitrogen at the interface similar to nitrided silicon dioxide films. This film showed superior TDDB under hot electron stressing. Kim et al. (1994) studied nitriding native oxide in ammonia followed by depositing nitride from silane–ammonia mixtures and reported that these films had higher breakdown and lower leakage compared to ONO films. The degradation of TDDB of stacked ONO films and the role of nitride deposition temperature was studied by Tanaka et al., who concluded that lower temperature deposited Si_3N_4 films had improved TDDB due to reduced film roughness. Clearly, the TDDB behavior of thin dielectrics of composite films is strongly affected by the structure and atomic distribution in the thin insulating layers. In thicker composite layers, bulk defects and inhomogeneities add to the complexities of the conduction and breakdown behavior.

7.6.3.3 Is TDDB a Reliability Issue for Thick Insulators?

The average electrical field experienced by the insulator in the interconnection is quite small compared to that experienced at the gate. For silicon oxide-based interlevel dielectrics TDDB is simply not an issue and only severe defects in the insulator can produce a reliability problem. In fact, a ramp breakdown stress test for thick insulators at low fields, to highlight defects, is sufficient to ensure reliability. Voltage ramp tests are common in semiconductor manufacturing to quantify

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the defect levels by ramping a capacitor test structure with electrodes formed from two levels of interconnection, with the dielectric sandwiched between to look for interlevel defects or with an interdigitated comb structure to look for intralevel defects.

Two types of defects tend to affect the reliability: environmentally caused defects such as particulates and those caused by processes or designs. The general trends of how these affect the breakdown are known. For example, Fe impurities reduced the breakdown voltage with an increase in metallic concentration (Henley et al., 1993). The understanding of how these defects affect acceleration factors and projection of failure rates from accelerated to use conditions is unknown. The most powerful approach is to use redundant insulating layers (Gati et al., 1986; Joseph and Wong, 1986) and create a composite layer structure to reduce the overall defects. Equally important is to prescribe design rules for given process tolerances to guarantee some minimum insulator thickness between wiring.

The use of Cu conductors, especially with future dielectrics with lower dielectric constants may be more of a problem. Cu can diffuse readily through interlevel dielectric materials of all kinds and there have been some studies that have characterized the most promising candidates (Loke et al., 1999; Bartha et al., 2002). The best defense against this problem is to use an effective liner as a diffusion barrier. If this problem is obviated, however, it is still not clear that we have a reliable system. The low-*k* interlevel dielectric itself can break down (Lloyd et al., 2004). In addition, stress corrosion cracking has been shown to be a potential problem (Cook and Liniger, 1999) that could contribute to TDDB in real systems.

Most importantly, to answer the question posed at the beginning of this section, we need to understand the physics of the breakdown of these low-*k* dielectrics. At the time of writing, this has not yet been accomplished. An appreciation of the importance of this question can be obtained from the following illustration. If we have data gathered at an accelerated field that will extrapolate to a failure probability at use condition of a few percent using the "E model," use of the "1/E model" predicts lifetimes longer than that of the solar system.

7.7 CONCLUDING REMARKS

Adherence to the self-fulfilling Moore's law has driven fundamental changes in the processing and design of integrated circuits such that new materials are being employed about which our knowledge is very limited. The pressures of the marketplace require that we use these new materials long before they are properly characterized, especially with respect to their reliability related performance.

The metallization reliability (Cu electromigration and stress voiding) is relatively stable and well understood at this point in time. We have learned to make good reproducible Cu conductors and they have been shown to be quite reliable. Furthermore, we have gained considerable understanding of how Cu behaves under real conditions. The story with the low-*k* dielectrics, however, is not so well written. As we search for the ideal interlevel dielectric material (not quite settled upon at the time of writing), we are finding that a myriad of materials are being proposed by suppliers, each with its own peculiar properties and each with a different response to the stresses of everyday life. Therefore, the extrapolation of test results to use conditions is not accurately predictable and will remain so until we have studied these materials in detail. As such, considerable research and development needs to be performed before we will be comfortable with them in critical applications.

The bottom line in any reliability program is to ensure that the failure modes are well understood and that tests are in place where the results from accelerated tests can be confidently applied to use conditions. Purely empirical approaches without understanding are inadequate and, in fact,

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quite dangerous. One cannot extrapolate accelerated test results without some kind of theoretical model that reflects a level of understanding of the materials involved. The principal responsibility of reliability science is in accurately determining these models providing us with the means to make the extrapolations. We have work to do.

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