Computer Architecture

Third Year-Computer Eng. Theoretical : 3 hrs./ week
Control and Systems Eng. Dept.

1- Data Representation :-

- Complements – (r-1)'S complement – (r' S) complement, Sub. Of Unsigned number (Hrs.)
- Fixed-Point, Integer, Arithmetic Addition and Subtraction, Overflow, Floating Point, Error detection codes.

2- Register Transfer and Microoperations:-

- Register transfer language, Register transfer
- Bus and memory transfer (Hrs.)
- Arithmetic and logic Microoperations
- Shift Microoperations
- Arithmetic logic shift unit
- Control function

3- Basic Computer Organization and Design

- Instruction code
- Computer register, computer instructions
- Timing and control
- Memory – reference instruction (Hrs.)
- Input – Output and interrupt
- Complete computer description
- Design of basic computer
- Design of accumulator logic

4- Micro Programmed Control

- Control memory
- Address sequencing (Hrs.)
- Micro program example
- Design of control time

5- Central Processing Unit

- General register, and stack organization
- Instruction formats
- Addressing modes
- Data transfer and manipulation (Hrs.)
- Reduced instruction set computer

6- Memory Management

- Memory hierarchy
- Auxiliary memory
- Main memory
- Associative memory (Hrs.)
- Cache memory
- Virtual memory management
- Memory management hardware

7- Pipeline

- Parallel processing
- Pipelining (Hrs.)

8- Computer Arithmetic

- Addition, Subtraction, Multiplication and Division Algorithm
- Decimal arithmetic operations (Hrs.)

9- Input – Output Organization

- Peripheral Devise
- Asynchronous Data transfer
- Mode of transfer (Hrs.)
- Direct Memory Access (DMA)
- Input – Output Processor (IOP)

References:

1- M. Morris Mano, Computer System architecture.(2^{nd} + 3^{rd} editions)
2- M. Morris Mano, Computer Engineering Hardware Design.

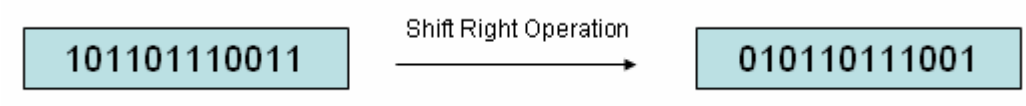
Subject : **Computer Architecture**
معمارية حاسبة

Lecture 1: Data Representation

Lecture 2-3-4-5: Register Transfer and Micro-Operations

L2-1: Register Transfer Language

- Digital System: An interconnection of hardware modules that do a certain task on the information.
- Registers + Operations performed on the data stored in them = Digital Module
- Modules are interconnected with common data and control paths to form a digital computer system
- Micro operations: operations executed on data stored in one or more registers.
- For any function of the computer, a sequence of micro operations is used to describe it
- The result of the operation may be:
  - replace the previous binary information of a register or
  - transferred to another register



- **The internal hardware organization of a digital computer is defined by specifying:**

- **The set of registers it contains and their function**
- **The sequence of micro operations performed on the binary information stored in the registers**
- **The control that initiates the sequence of micro operations**

- **Registers + Micro operations Hardware + Control Functions = Digital Computer**
- **Register Transfer Language (RTL) : a symbolic notation to describe the micro operation transfers among registers**

Next steps:

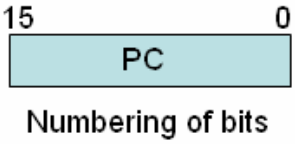
- **Define symbols for various types of micro operations,**
- **Describe the hardware that implements these micro operations**

L2-2: INTER-REGISTER TRANSFER / INTER- REGISTER MICRO-OPERATIONS (Parallel Transfer/ Serial Transfer / Bus transfer/ Memory Transfer)

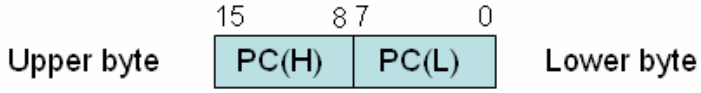
- **Computer registers are designated by capital letters (sometimes followed by numerals) to denote the function of the register**
  - **R1: processor register**
  - **MAR: Memory Address Register (holds an address for a memory unit)**
  - **PC: Program Counter**
  - **IR: Instruction Register**
  - **SR: Status Register**
- **The individual flip-flops in an n-bit register are numbered in sequence from 0 to n-1 (from the right position toward the left position)**

A block diagram of a register

Other ways of drawing the block diagram of a register:



Numbering of bits



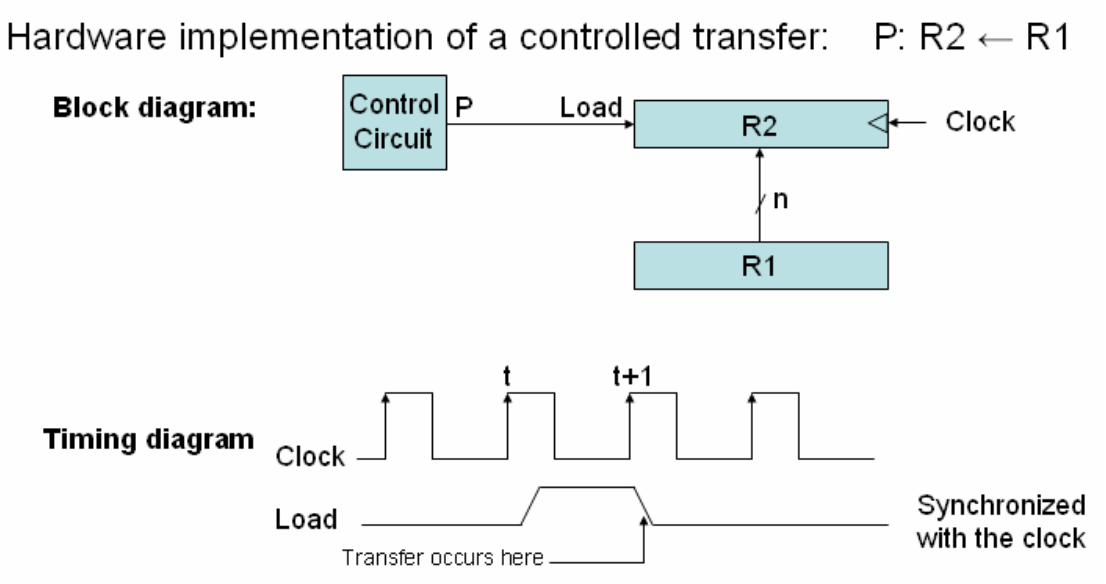
Partitioned into two parts

- **Information transfer from one register to another is described by a *replacement operator:* R2 ← R1**
- **This statement denotes a transfer of the content of register R1 into register R2**
- **The transfer happens in one clock cycle**
- **The content of the R1 (source) does not change**
- **The content of the R2 (destination) will be lost and replaced by the new data transferred from R1**
- **We are assuming that the circuits are available from the outputs of the source register to the inputs of the destination register, and that the destination register has a parallel load capability**
- **Conditional transfer occurs only under a control condition**

- **Representation of a (conditional) transfer**

P: R2 ← R1

- **A binary condition (P equals to 0 or 1) determines when the transfer occurs**
- **The content of R1 is transferred into R2 only if P is 1**



Basic Symbols for Register Transfers		
Symbol	Description	Examples
Letters & numerals	Denotes a register	MAR, R2
Parenthesis ( )	Denotes a part of a register	R2(0-7), R2(L)
Arrow ←	Denotes transfer of information	R2 ← R1
Comma ,	Separates two microoperations	R2 ← R1, R1 ← R2

L2-3: ARITHMETIC MICRO-OPERATIONS

L2-4: LOGIC MICRO-OPERATIONS

- **Logic Micro-Operations**
- **Hardware Implementation**
- **Sample Applications**

L2-5: SHIFT MICRO-OPERATIONS

L2-6: CONTROL FUNCTIONS

- **Timing Sequences**
- **Generation of Control Functions**